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Control of a Single-Star Flying Capacitor Converter Modular Multi-level Cascaded Converter (SSFCC-MMCC) STATCOM for Unbalanced Load Compensation

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Abstract

This paper presents a simulation study into the implementation of the single star flying capacitor converter modular multi-level cascaded converter (SSFCC-MMCC) as a STATCOM for unbalanced load compensation. The paper proposes a new concept of voltage source current control for the reference current tracking of the compensated currents. This control strategy enables the STATCOM system to compensate for both positive sequence reactive and negative sequence currents. Not only compensates for unbalanced load, but also keep the module Dc-link and flying capacitor voltages maintained at their rated values. Simulation results verify the performance of the chosen topology.

1 Introduction

Current imbalance in power distribution systems is due to uneven distribution of single-phase loads, such as commercial facility loads, single-phase electric traction systems, rural electric systems, etc. causing mild voltage unbalance. Larger short-term unbalances can be caused by power system faults. The problem is exacerbated by the recent unprecedented growth of power electronic-based energy-saving schemes such as single-phase adjustable speed drives (ASDs) and switch-mode power supplies, and the trend towards interfacing renewable energy sourced power generators, particularly photovoltaic panels, with the grid phase lines. The adverse effects of load unbalance include low power factor, added line losses and heating effects in power systems.

Voltage Source Converter-based Static Compensators (VSC-STATCOM) have been investigated as an effective mitigation technique for unbalanced operation. They are required to be able to actively compensate unbalanced load and override unbalanced conditions without over-current tripping. Hence in terms of control, these compensators, assuming lossless, need to generate negative sequence current to overcome load unbalance while simultaneously supplying positive sequence reactive current for power factor correction. The connection of a VSC-STATCOM to an unbalanced network causes the appearance of a second harmonic component on the converter's dc side. This, if not eliminated, generates low order harmonic current on the ac side resulting in further deterioration of the power quality [1]. The situation becomes particularly difficult when the unbalance is continually varying as occurs with large industrial loads such as arc furnaces. Various schemes reported have been shown to be effective for compensators based on converters with common dc links such as the two-level full-bridge or classical multilevel converters [1]. The general approach has been extracting, and hence eliminating, negative-sequence components from the load current and cancelling as much as possible the harmonic components on the dc-voltage. There is no issue of converter phase limb voltage imbalance even though they supply unbalanced current.

The Modular Multi-level Cascaded Converter (MMCC) have been investigated as an effective STATCOM device for balanced compensation [2-4]. Contrasting to their two-level converter-based form, the benefits offered by the MMCC are: scalability by using its modular nature to extend to any voltage levels required, thereby dispensing with the need for a multi-winding phase shifted line frequency transformer [5], good waveform performance, and lower switching frequency. Also, the switching and clamping devices in the MMCC are rated at module power levels, enabling the use of low-rated devices and reducing the voltage stresses on them. This allows this topology to offer higher converter efficiency compared to classical multi-level converters. The three phase limbs of an MMCC-based STATCOM can be star or delta connected, named as single-star or single-delta. When using them for unbalanced load compensation a special problem occurs which must be addressed; cancellation of the negative sequence current leads to an undesired non-zero active power flow between phases, but, since the dc-links supplying the stacked modules are galvanically isolated. This, in turn, causes the individual dc-link voltages to drift away from their intended values. Different control methods have been reported in the literature [6-9] to solve this problem for either star or delta configured MMCCs, but these are restricted to modules of full H-bridge topology.

This paper presents a new STATCOM for unbalanced load compensation using a variant of the SSBC-MMCC [10] known as the single star flying capacitor converter MMCC (SSFCC-MMCC). Each module is a basic single phase three-level full bridge flying capacitor converter (3L-FCC) which synthesizes three voltage levels (0, ±0.5VDC, ±VDC) [11]. Comparing to the MMCC using H-bridge cells the main advantage of this topology is having more degrees of freedom in control at the sub-module level, hence it is more flexible for converters

requiring high performance dynamic control. SSFCC-MMCC has been used in the literature for balanced STATCOM application [12, 13], but not yet for unbalanced load compensation. In such a case the challenges, apart from those described above for SSBC-MMCC, also include keeping the module and flying capacitor voltages balanced. This leads to a new concept for a voltage source current control scheme used in tracking the three phase reference currents, and an efficient method for splitting the calculated zero sequence voltage will also be presented.

2 SSFCC-MMCC-based STATCOM and Power System Configuration

The circuit diagram of a SSFCC-MMCC-based STATCOM and the power system used for developing the control scheme are shown in figure 1. The phase limb of the converter comprises a cascade of 3L-FCC's which serve as the basic modules. Each module consists of 8 switch-diode pairs, an outer DC-Bus capacitor $\mathbf{C_{DC1}}$ and two flying capacitors C_a and C_b. The voltage on $\mathbf{C_{DC1}}$ defines the module voltage rating as $\mathbf{V_{DC}}$ and this value together with the capacitance is twice that of the two flying capacitors. This 3L-FCC can synthesize a total of 5 voltage levels ($\mathbf{0, \pm 0.5V_{DC}, \pm V_{DC}}$) using 16 valid switching states. The number of cascaded modules is determined by the voltage of the power network, though in this study only six 3L-FCC modules, two for each of the three phases, are used, hence each phase limb has 9 voltage levels ($\mathbf{0, \pm 0.5V_{DC}, \pm V_{DC}, \pm 1.5V_{DC}, \pm 2V_{DC}}$). Three phases are connected in star configuration with the neutral point floated.

The three phase voltages of the power network studied are balanced and rated at 230V, 10KVA, 50Hz and supplies power to the load through distribution lines with impedance represented as $Z_T = R_T + jX_T$. At the Point of Common Coupling (PCC), two inductive loads are connected, one is balanced and another unbalanced, both rated at the same voltage 230V. These loads draw both reactive and unbalanced current from the source, causing low power factor, low efficiency and poor quality of supplied power. The STATCOM is interfaced to the PCC through a filter inductance L_c to reduce the harmonics generated by the converter switching action. Also, the power losses of the STATCOM are modelled by resistance R_c.

3 DC voltage imbalance in the SSFCC-MMCC

Under balanced operation this SSFCC-MMCC-based STATCOM is able to mitigate the reactive power, but when the load is unbalanced it faces challenging issue. This is because the average active power flowing through the converter is non-zero when load is unbalanced, but the isolated DC sources for the chained modules do not allow circulating current flowing within the converter phase limbs, resulting in module DC voltages imbalance. The non-zero active power can be analysed as follows.

Under unbalanced operation, the PCC voltages and compensation reference currents are written in phasor form as

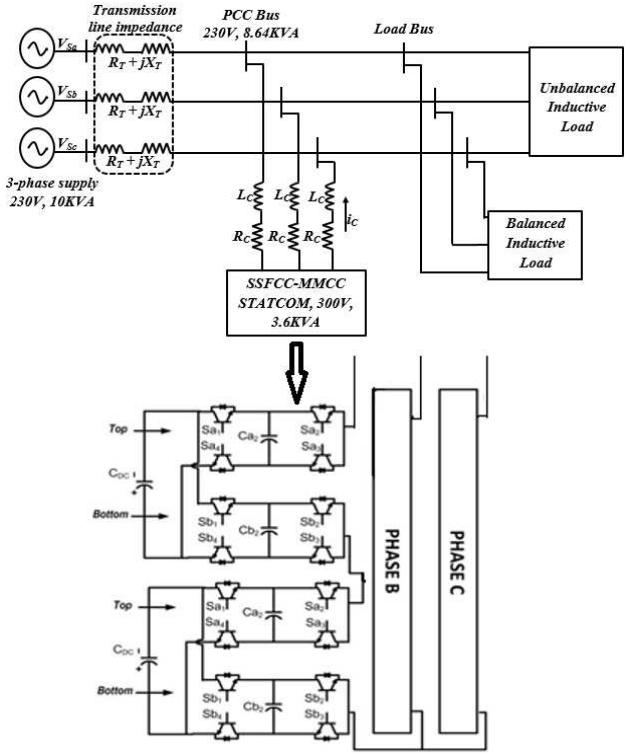

Figure 1: (a) SSFCC-MMCC STATCOM distribution power system diagram, (b) STATCOM circuit diagram

$$\begin{aligned} v_a &= V_P \angle \varphi_{VP} \\ v_b &= V_P \angle (\varphi_{VP} - \frac{2\pi}{3}) \\ v_c &= V_P \angle (\varphi_{VP} + \frac{2\pi}{3}) \end{aligned} \tag{1}$$

$$\begin{aligned} i_{ra}^{*} &= I_P \angle \varphi_{iP} + I_n \angle \varphi_{in} \\ i_{rb}^{*} &= I_P \angle (\varphi_{iP} - \frac{2\pi}{3}) + I_n \angle (\varphi_{in} + \frac{2\pi}{3}) \\ i_{rc}^{*} &= I_P \angle (\varphi_{iP} + \frac{2\pi}{3}) + I_n \angle (\varphi_{in} - \frac{2\pi}{3}) \end{aligned} \tag{2}$$

Thus the total per phase active powers are expressed as

$$\begin{aligned} p_a &= \Re[(V_P \angle \varphi_{VP})(I_P \angle -\varphi_{iP} + I_n \angle -\varphi_{in})] \\ &= V_P I_P \cos(\varphi_{VP} - \varphi_{iP}) + V_P I_n \cos(\varphi_{VP} - \varphi_{in}) \\ p_b &= \Re[(V_P \angle (\varphi_{VP} - \frac{2\pi}{3}))(I_P \angle -(\varphi_{iP} - \frac{2\pi}{3}) + I_n \angle -(\varphi_{in} + \frac{2\pi}{3}))] \\ &= V_P I_P \cos(\varphi_{VP} - \varphi_{iP}) + V_P I_n \cos(\varphi_{VP} - \varphi_{in} + \frac{2\pi}{3}) \\ p_c &= \Re[(V_P \angle (\varphi_{VP} + \frac{2\pi}{3}))(I_P \angle -(\varphi_{iP} + \frac{2\pi}{3}) + I_n \angle -(\varphi_{in} - \frac{2\pi}{3}))] \\ &= V_P I_P \cos(\varphi_{VP} - \varphi_{iP}) + V_P I_n \cos(\varphi_{VP} - \varphi_{in} - \frac{2\pi}{3}) \end{aligned} \tag{3}$$

The first terms on the right-hand-side (RHS) of the above three expressions are the respective positive sequence phase powers which are balanced and hence having a zero sum. This implies that the average three phase power flowing through the STATCOM is zero. However the RHS second terms are cross products of positive sequence voltage and negative sequence current and result in undesired non-zero average active power

flow through individual phases. This causes the DC link and flying capacitor voltages of each module drift away from their nominal values hence preventing the STATCOM to function properly as a reactive power and unbalanced load compensator.

An effective approach to overcoming this problem involves adding a common zero-sequence voltage to each of the three converter-limb voltages. If accurately estimated and applied adequately to each phase limb, this zero-sequence voltage should cancel out the effect of the cross component terms of each phase active power without disturbing the three-phase line-line voltage and current at the network side. Thus the control strategy for the SSFCC-MMCC-based STATCOM must include the followings

- Converter active power/current evaluation
- Zero-sequence voltage estimation
- Converter reference voltage estimation with zero-sequence voltage injection

3.1 Active power/current evaluation

The active power flow across each phase limb ($\mathbf{P_a}$, $\mathbf{P_b}$ and $\mathbf{P_c}$) comprises two elements; the positive sequence active power due to compensating converter losses and negative sequence active power due to unbalanced load.

The first element depends on the active current, I_{d_ref}, required for maintaining the average value of the three phase-limb DC-bus voltages to the nominal level. This current can be evaluated using the well-known DC-bus voltage feedback control scheme as illustrated in figure 2. For SSFCC-MMCC topology obtaining the average value, $\mathbf{V_{DC\_avg}}$, of the three phase-limb DC-link voltages requires calculating per phase limb average DC voltage. This can be done by averaging the measured individual module voltages within the corresponding phase chain, so the DC-link average voltages for each phase are given respectively as

$$V_{DC\_(abc)} = \frac{1}{n_{mp}} \sum_{i=1}^{n_{mp}} V_{DC\_i(abc)} \qquad (4)$$

where $\mathbf{n_{mp}}$ denotes the number of modules per phase and $\mathbf{V_{DC\_avg}}$ can be evaluated as

$$V_{DC\_avg} = \frac{V_{DC\_a} + V_{DC\_b} + V_{DC\_c}}{3} \qquad (5)$$

The positive sequence active current can be evaluated using a feedback P+I controller as shown in figure 2.

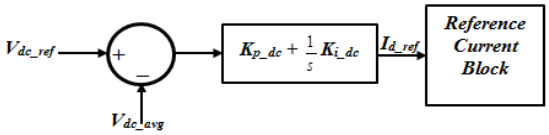

Figure 2: Active current compensation controller

Evaluation of the second element - the negative sequence active power relies on implementing a cluster voltage balancing control scheme since it is this power flowing in and out of each converter phase limb causing the imbalance of the phase limb DC-link voltages. As shown in figure 3 this cluster voltage balancing control consists of three PI regulators respectively for each phase limb. The reference voltage for the three voltage controllers is the same average voltage $\mathbf{V_{DC\_avg}}$ evaluated in (5) and feedback voltages are the respective phase limb average voltages (i.e $\mathbf{V_{DC\_a}}$, $\mathbf{V_{DC\_b}}$ and $\mathbf{V_{DC\_c}}$) as derived by (4). The output of each regulator generates the reference active power for the corresponding phase of the STATCOM converter and will be used to determine the zero sequence voltage.

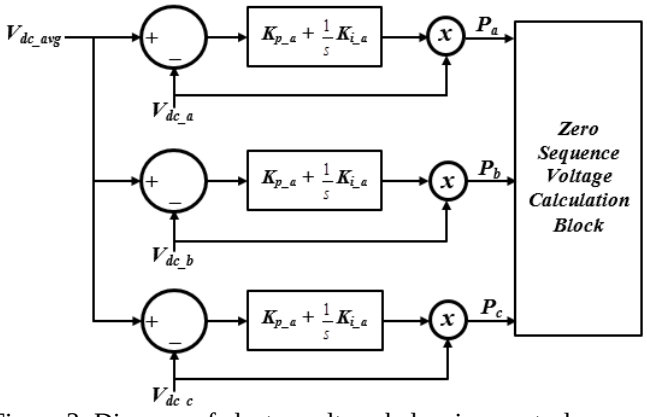

Figure 3: Diagram of cluster voltage balancing control

3.2 Zero-sequence voltage estimation

Having evaluated the active power, $\mathbf{P_a}$, $\mathbf{P_b}$ and $\mathbf{P_c}$, flowing through each phase limb, a zero sequence voltage $\mathbf{v_o}$ can be derived. This follows the principle that the sum of active power caused by the injected zero sequence voltage and that of existing active power expressed in (3) should balance the reference powers. Thus the equations for power across each phase are written as

$$\begin{aligned}
p_a &= \Re[(V_P\angle\varphi_{VP} + V_0\angle\varphi_0)(I_P\angle-\varphi_{iP} + I_n\angle-\varphi_{in})] \\
&= \begin{pmatrix} V_P I_P \cos(\varphi_{VP} - \varphi_{iP}) + V_P I_n \cos(\varphi_{VP} - \varphi_{in}) + \\ V_0 I_P \cos(\varphi_0 - \varphi_{iP}) + V_0 I_n \cos(\varphi_0 - \varphi_{in}) \end{pmatrix} \\
p_b &= \Re[(V_P\angle(\varphi_{VP} - \tfrac{2\pi}{3}) + V_0\angle\varphi_0)(I_P\angle-(\varphi_{iP} - \tfrac{2\pi}{3}) + I_n\angle-(\varphi_{in} + \tfrac{2\pi}{3}))] \\
&= \begin{pmatrix} V_P I_P \cos(\varphi_{VP} - \varphi_{iP}) + V_P I_n \cos(\varphi_{VP} - \varphi_{in} + \tfrac{2\pi}{3}) \\ + V_0 I_P \cos(\varphi_0 - \varphi_{iP} + \tfrac{2\pi}{3}) + V_0 I_n \cos(\varphi_0 - \varphi_{in} - \tfrac{2\pi}{3}) \end{pmatrix} \\
p_c &= \Re[(V_P\angle(\varphi_{VP} + \tfrac{2\pi}{3}) + V_0\angle\varphi_0)(I_P\angle-(\varphi_{iP} + \tfrac{2\pi}{3}) + I_n\angle-(\varphi_{in} - \tfrac{2\pi}{3}))] \\
&= \begin{pmatrix} V_P I_P \cos(\varphi_{VP} - \varphi_{iP}) + V_P I_n \cos(\varphi_{VP} - \varphi_{in} - \tfrac{2\pi}{3}) \\ + V_0 I_P \cos(\varphi_0 - \varphi_{iP} - \tfrac{2\pi}{3}) + V_0 I_n \cos(\varphi_0 - \varphi_{in} + \tfrac{2\pi}{3}) \end{pmatrix}
\end{aligned} \qquad (6)$$

Any two power equations in (6) can be chosen for use in determining the amplitude and phase angle of $\mathbf{v_0}$, assuming the first two are selected they can be written as:

$$\begin{aligned}
&V_0 I_P \cos(\varphi_0 - \varphi_{iP}) + V_0 I_n \cos(\varphi_0 - \varphi_{in}) = \\
&p_a - \left(V_P I_P \cos(\varphi_{VP} - \varphi_{iP}) + V_P I_n \cos(\varphi_{VP} - \varphi_{in})\right) \\
&V_0 I_P \cos(\varphi_0 - \varphi_{iP} + \tfrac{2\pi}{3}) + V_0 I_n \cos(\varphi_0 - \varphi_{in} - \tfrac{2\pi}{3}) = \\
&p_b - \left(V_P I_P \cos(\varphi_{VP} - \varphi_{iP}) + V_P I_n \cos(\varphi_{VP} - \varphi_{in} + \tfrac{2\pi}{3})\right)
\end{aligned} \qquad (7)$$

and their more compact forms are given as

$$X_{a1}V_0\cos\varphi_0 + X_{a2}V_0\sin\varphi_0 = p_a - X_{a3}$$
$$X_{b1}V_0\cos\varphi_0 + X_{b2}V_0\sin\varphi_0 = p_b - X_{b3} \quad (8)$$

where $X_{a1} = I_p\cos\varphi_{ip} + I_n\cos\varphi_{in}$, $X_{a2} = I_p\sin\varphi_{ip} + I_n\sin\varphi_{in}$,

$X_{a3} = V_P I_P\cos(\varphi_{VP} - \varphi_{iP}) + V_P I_n\cos(\varphi_{VP} - \varphi_{in})$,

$X_{b1} = I_p\cos(\varphi_{ip} - \frac{2\pi}{3}) + I_n\cos(\varphi_{in} + \frac{2\pi}{3})$,

$X_{b2} = I_p\sin(\varphi_{ip} - \frac{2\pi}{3}) + I_n\sin(\varphi_{in} + \frac{2\pi}{3})$ and

$X_{b3} = V_P I_P\cos(\varphi_{VP} - \varphi_{iP}) + V_P I_n\cos(\varphi_{VP} - \varphi_{in} + \frac{2\pi}{3})$

From (8) the zero sequence voltage amplitude and phase angle can be derived as

$$V_0 = \frac{(p_a - X_{a3})}{X_{a1}\cos\varphi_0 + X_{a2}\sin\varphi_0} \quad (9)$$

$$\varphi_0 = \arctan\left[\frac{(p_a - X_{a3})X_{b1} - (p_b - X_6)X_{a1}}{(p_b - X_{b3})X_{a2} - (p_a - X_{a3})X_{b2}}\right] \quad (10)$$

and its time domain instantaneous voltage is expressed as

$$v_0 = V_0\sin(\omega t + \varphi_0) \quad (11)$$

where $\theta = \omega t$ is the synchronous rotating angle created by the phase locked loop (PLL).

With the calculated zero sequence voltage applied to each phase, the average active power in all three phases should ideally be zero. In addition, V_0 ensures the capacitor voltages of the individual phase legs do not fluctuate away from their nominal values regardless of the unbalanced load current being compensated. This zero sequence voltage will not affect the external values of voltage and current at the point of common coupling.

3.3 Converter Phase Reference Voltage Calculation

The reference voltage per phase limb of the converter should enable the current flowing to the PCC to compensate for reactive power and current imbalance created by the unbalance load. The current controller can be designed based on

$$v_{c(abc)} = (v_{s(abc)} - L_c\frac{di_{r(abc)}^*}{dt} - Ri_{r(abc)}^*) \quad (12)$$

Where v_{sa}, v_{sb} and v_{sc} are the line to neutral PCC voltages, v_{ca}, v_{cb} and v_{cc} are the converter output voltages, i_{ra}^*, i_{rb}^* and i_{rc}^* are the reference compensated currents. This method ensures the usage of three voltage source current control for three phases of the converter. The voltage source current control is implemented using a predictive deadbeat control as expressed in (13).

$$v_{c(abc)}(k+1) = v_{s\_(abc)}(k) - i_{r(abc)}^*(k)\left[\frac{L_c}{T_s}\right] - i_{c(abc)}(k)\left[R - \frac{L_c}{T_s}\right] \quad (13)$$

The three instantaneous converter line to neutral voltages including the zero sequence voltage (v_{c_a}, v_{c_b} and v_{c_c}) is expressed in (14) as

$$v_{c\_(abc)} = v_{c(abc)} + v_o \quad (14)$$

(14) ensures that the zero sequence component of the converter output voltage v_{co} resulting from the average power across each phase leg not being zero is equated to the counterpart of the calculated supply voltage ($v_o = v_{co}$) through the injection of v_o.

4 Control Scheme for a SSFCC-MMCC STATCOM

Figure 4 shows the schematic diagram of the STATCOM controller. This comprises three parts based on their function, namely: the reference current and zero sequence voltage determination block, the current tracking controller and the modulator controller. Under the reference current and $\mathbf{v_o}$ block, the reference currents to be compensated are determined along with the DC-link voltage control and $\mathbf{v_o}$. The current controller is implemented using the reference currents, PCC voltages, zero sequence voltage and STATCOM current as inputs to generate the converter reference voltage. This current control is actualized using the deadbeat predictive controller. The generated reference voltage s is inputted into the modulator to synthesize gate signals. The phase shifted PWM is employed for this operation as discussed in [12].

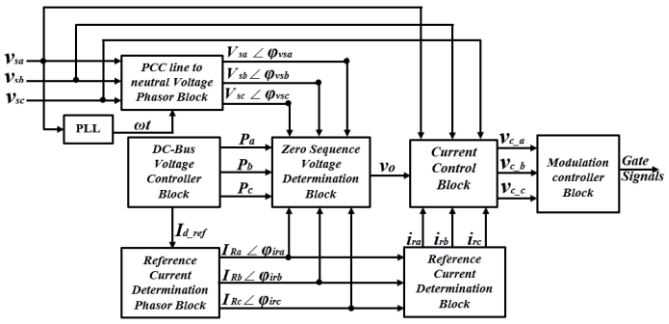

Figure 4: Block diagram of unbalanced load SSFCC-MMCC STATCOM controller

5 Simulation Result

Matlab Simulink has been used to implement the system configuration highlighted in figure 1. $\mathbf{i_L}$, $\mathbf{i_C}$ and $\mathbf{i_S}$ denote the load, STATCOM and source currents respectively. The STATCOM controller is designed to compensate for both positive sequence reactive and negative sequence currents denoted as $\mathbf{i_{Lq}}$ and $\mathbf{i_{Ln}}$ respectively. The operating limit/range of the STATCOM controller is determined by the maximum attainable output voltage on each converter phase legs. This operating range is the ratio of the STATCOM converter DC-link phase voltage $\mathbf{V_{DC\_(abc)}}$ to the line to neutral voltage of the power system $V_{S\_(abc)}$ ($\mathbf{V_{DC\_(abc)}/V_{S\_(abc)}}$). This operating limit determines the degree of unbalanced ($\mathbf{I_n/I_{Cq}}$) compensated current. This implies that the converter voltage rating must be higher than the line to neutral voltage in other to compensate unbalance load current using star configured single star cascaded converters. For this simulated system, the DC-link phase voltage amplitude is $\mathbf{V_{DC}}$=300V and 230V for the line to neutral PCC voltage. The converter operates within its linear modulation region for $\mathbf{I_n/I_{Cq}} \leq \boldsymbol{30.43\%}$. Above this, the converter rides into over modulation region and with extreme high unbalance, the converter operating range becomes invalid. In investigating the effectiveness of this STATCOM controller for SSFCC-MMCC two different scenarios are studied based on the exclusion and inclusion of the zero sequence voltage $\mathbf{v_o}$ in the controller. The parameters of the power system are illustrated in table 1.

parameters	Rating
Rated network line to neutral voltage (peak)	230V
Distribution system resistance R_T	0.5Ω
Distribution system inductance L_T	5mH
Filter resistance R_C	20Ω
Filter inductance L_C	1600µH
Rated converter capacity	10KVA
Number of connected cells in each phase leg **Nmp**	2
Rated DC voltage of each module	150V
Rated DC voltage of module flying capacitor	75V
DC module capacitance rating	260µF
Module flying capacitor capacitance rating	130µF
Switching frequency **fs**	750Hz

Table 1: Power system configuration parameters

At time interval $0.5 \le t \le 1$a balanced inductive load is connected to PCC through the load bus making STATCOM converter compensate for the positive sequence reactive current i_{Lq}=0.5A. At time t=1s, the unbalanced load is tied to the grid resulting in a negative sequence current component i_{Ln}=0.57A and a new i_{Lq}=1.8A. Figure 5 shows the waveforms of the three phase loads, STATCOM and PCC currents. The degree of unbalanced created by the load I_n/I_{Cq}**=0.57/1.84=30.98%** lies within the operating limit of the STATCOM controller. It is observed that the STATCOM totally compensates for the positive sequence reactive and negative sequence currents as illustrated in figures 5(d) and (e) respectively.

With the calculated v_o included in the current controller, the average active power in each phase legs as seen in figure 6(a) are zero. This implies that the DC-link and flying capacitors of each modules are operating within their nominal values as shown in figures 6(b) and (c) respectively.

Figure 7 highlights the effects of the exclusion of v_o on the STATCOM operation. Without v_o, the average active power in each leg does not maintain a zero average power, although the total three phase active power sum up to zero. This results in the DC-link and flying capacitor voltage drifting from their nominal operating voltages as shown in figures 7(b) and (c) respectively. The degree of unbalance determines the severity of drift experienced by these capacitors.

From figure 8, it is observed that if the degree of unbalance is 10% higher than the operating range of the STATCOM controller I_n/I_{Cq}**=0.8/2.02=39.6%**, the DC-link and flying capacitors voltages are still operating at their nominal voltages.

With a further increment on the unbalanced level I_n/I_{Cq}**=1.14/2.2=51.8%**, the reactive component of the load current and negative sequence load current are still compensated for by the STATCOM as shown in figures 9(a) and (b) respectively. This degree of unbalance results in the converter controller working out of its operating range. This can be observed in figures 9(c) and (d) that the converter cannot work effectively resulting to the DC-link and flying capacitors drifting away from their actual rated voltages.

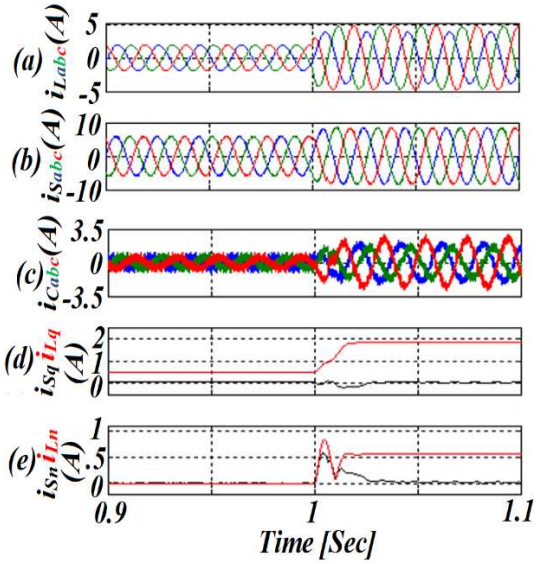

Figure 5: Simulated waveforms having calculated zero sequence voltage with 30.98% of unbalanced. (a) Unbalanced load currents. (b) PCC currents. (c) STATCOM currents. (d) Reactive current component. (e) Negative sequence current component.

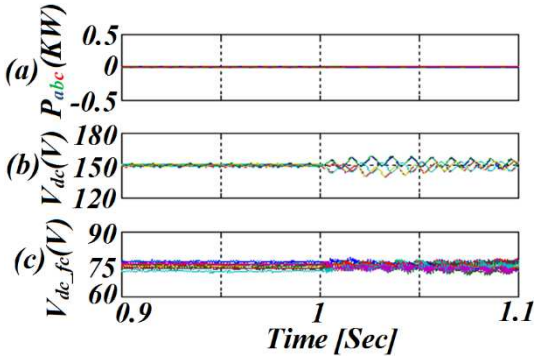

Figure 6: Simulated waveforms having calculated zero sequence voltage with 30.98% of unbalanced. (a) Three phase active power. (b) Module dc-link voltages (c) Module flying capacitor voltages.

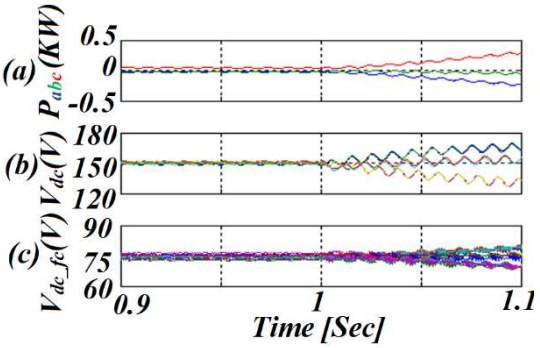

Figure 7: Simulated waveforms highlighting the effects of zero sequence voltage exclusion. (a) Three phase active power. (b) Module dc-link voltages (c) Module flying capacitor voltages.

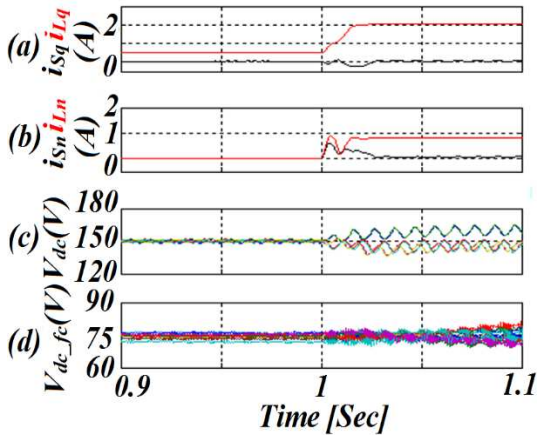

Figure 8: Simulated waveforms with 40% of unbalanced. (a) Reactive current component. (b) Negative sequence current component. (c) Module dc-link voltages (d) Module flying capacitor voltages.

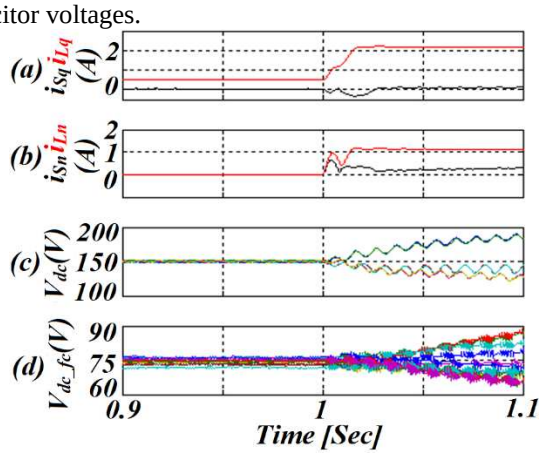

Figure 9: Simulated waveforms with 52% of unbalanced. (a) Reactive current component. (b) Negative sequence current component. (c) Module dc-link voltages (d) Module flying capacitor voltages.

6 Conclusion

This paper has discussed an SSFCC-MMCC based STATCOM operating under unbalanced condition. A Voltage Source Current Control Concept has been used in tracking the reference currents and obtaining the zero average power in each phase. An arm/per phase balancing technique along with a calculated zero sequence voltage $\mathbf{v_o}$ has enable the DC-link and flying capacitor voltages of each module to be operated at their rated values. The operating limit of the STATCOM controller using SSFCC-MMCC is also analysed. This operating limit was found to depend on the maximum output voltage of each phase leg.

7 Reference

[1] Blazic, B. and I. Papic, Improved D-StatCom control for operation with unbalanced currents and voltages. Power Delivery, IEEE Transactions on, 2006. **21**(1): p. 225-233.

[2] Govindaraj, V. and M.K. Elango. Modular multilevel cascade converter based statcom for reactive power compensation. in Circuits, Power and Computing Technologies (ICCPCT), 2013 International Conference on. 2013.

[3] Yang, X., et al. Research on modular multilevel converter based STATCOM. in Industrial Electronics and Applications (ICIEA), 2011 6th IEEE Conference on. 2011. IEEE.

[4] Hagiwara, M., R. Maeda, and H. Akagi, Application of a Modular Multilevel Cascade Converter (MMCC-SDBC) to a STATCOM. IEEJ Transactions on Industry Applications, 2011. **131**: p. 1433-1441.

[5] Sixing, D. and L. Jinjun, A Study on DC Voltage Control for Chopper-Cell-Based Modular Multilevel Converters in D-STATCOM Application. Power Delivery, IEEE Transactions on, 2013. **28**(4): p. 2030-2038.

[6] Maosong, Z. and W. Qunjing. Implementation of a cascade D-STATCOM under unbalanced conditions. in Electronics and Application Conference and Exposition (PEAC), 2014 International. 2014.

[7] Wenhua, L., et al. Research on unbalance load compensation by cascaded STATCOM with star configuration. in IECON 2012 - 38th Annual Conference on IEEE Industrial Electronics Society. 2012.

[8] Qiang, S. and L. Wenhua, Control of a Cascade STATCOM With Star Configuration Under Unbalanced Conditions. Power Electronics, IEEE Transactions on, 2009. **24**(1): p. 45-58.

[9] Betz, R.E., T. Summers, and T. Furney. Symmetry Compensation using a H-Bridge Multilevel STATCOM with Zero Sequence Injection. in Industry Applications Conference, 2006. 41st IAS Annual Meeting. Conference Record of the 2006 IEEE. 2006.

[10] Akagi, H., Classification, Terminology, and Application of the Modular Multilevel Cascade Converter (MMCC). Power Electronics, IEEE Transactions on, 2011. **26**(11): p. 3119-3130.

[11] Efika, I.B., et al. An overlapping multi-hexagon space vector modulation scheme for modular multilevel cascade converters. in Power Electronics and Applications (EPE), 2013 15th European Conference on. 2013.

[12] Efika, I.B., C.J. Nwobu, and L. Zhang. Reactive power compensation by modular multilevel flying capacitor converter-based STATCOM using PS-PWM. in Power Electronics, Machines and Drives (PEMD 2014), 7th IET International Conference on. 2014.

[13] Nwobu, C., et al. A modular multilevel flying capacitor converter-based STATCOM for reactive power control in distribution systems. in Power Electronics and Applications (EPE'15 ECCE-Europe), 2015 17th European Conference on. 2015. IEEE.