Modelling RF interference effects in Integrated Circuits.

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Abstract: The disturbance effects in complex electronic systems, subjected to a High Power Microwave (HPM), Continuous Wave (CW) or Pulse irradiation, show a conversion of the injected High Frequency (HF) out-of-band signal to a Low Frequency (LF) inband signal. In this paper a behavioural model is presented that combines HF and LF subcircuits to predict the effect of Radio Frequency Interference (RFI) on linear integrated circuits. The model is constructed from detailed measurements and manufacturers' data, and can be used to determine the upset mechanism in analogue systems subjected to RFI.

Summary

The electromagnetic (EM) environment in which electronic systems have to operate is becoming increasingly hostile while dependence on electronics is widespread and increasing. The need for assurance that upsets due to the EM environment will *not* occur is fundamental to acceptance of systems as fit for purpose. Design features to impart EM hardness are beginning to be implemented ab initio[1], but hardness verification of major systems still depends on testing prototype hardware late in the development process. This is expensive, and the cost of rectification of any shortfall found can be enormous.

Modern equipment design and evaluation processes are increasingly being carried out using computers. CAD/CAE systems are now being used extensively in industry for design and manufacture in a number of disciplines - aerodynamics, structures, mechanical, and of course, electronic design. The elements exist in principle to treat EM hardness in the same way. This opens the prospect of the hardness (or vulnerability) of a virtual design (CAD files) being amenable to virtual evaluation using modelling and a knowledge base. Virtual *clearance* of the system via the endorsement of the design and evaluation processes, to the satisfaction of a clearance authority, is the ultimate goal. While these may be long term objectives, addressing them now will produce substantial benefits in the short term including problem identification, decomposition of large-scale testing and a better general understanding of the RFI effects on systems.

The elements to allow software evaluation of EM hardness are coupling modelling and circuit emulation. Both of these have a substantial history, but neither has been developed to the stage where it can be used for practical hardness evaluation. A third element - a knowledge base (e.g. reactions of non-microwave semiconductors to microwave frequency inputs and of the practicalities of implementing coupling models) is required if such a process is to become reality. An integrated process has yet to be demonstrated.

Much work has been done to characterise the effects of electromagnetic interference on operational amplifiers and other circuits [1] [2]. Little attention has been given to addressing the problem of a system with more than one element (i.e. op-amp). This paper presents a means of modelling such systems. The model consists of a linear model to represent the interference propagation (HF subsystem) and a non-linear frequency dependent function to generate offset voltages that are injected into the LF part of the model, which can use standard device (macro) models, as illustrated in Figure 1 [3].

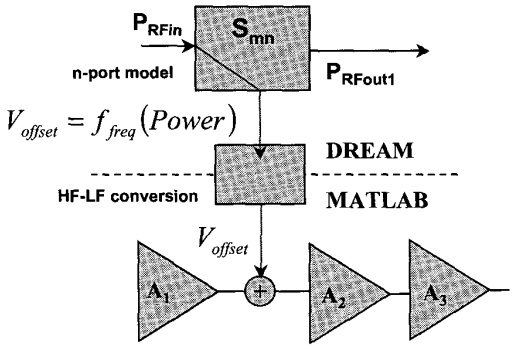

Figure 1 Two-layer model showing coupling between HF and LF layers

To implement this model, according to Figure 1, two different data analysis tools were used; DREAM and Mathworks MATLAB. DREAM is a database with an interface to MATLAB used by EMH&P group DERA to store and process laboratory data. DREAM was used to define the HF n-port model and MATLAB derives the HF-LF conversion to enable the calculation of the voltage offset to RF power levels. This works under the main circuit analysis tool such as PSpice. Other methods of data analysis can be used with the model, which may be to be implemented using any of a wide range of software tools method.

The HF subsystem is characterised by linear s-parameter measurements using an IC test jig and a Network Analyser (NA) [4]. This subsystem can be modelled directly in the frequency domain by a circuit simulator program such as PSpice. Coupling of interference between different pin configurations was modelled and the results compared with measured data. To verify the behavioural model for the comparison of measurements and simulation, an amplifier was set-up as a voltage follower buffer, modelled and compared to the measurements, from 100MHz to 6GHz. In this circuit the RF + dc biasing is fed back into pin 2 of the device in a conventional buffer configuration as illustrated in Figure 2.

The comparison between the measurements and simulation is good up to 2GHz, where some divergence between calculated and measured data is observed as illustrated by Figure 3. Above 2GHz,

[1] Far preferable to "bolt-on fixes" later on

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there are discrepancies between the calculated and the measured data. Some discrepancies at the higher frequencies in all the validation set-ups do show limitations of the model and/or measurements, which must be further, analysed.

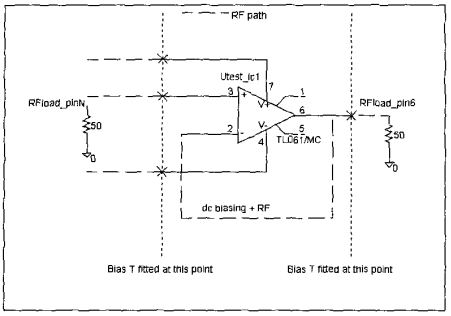

Figure 2 Measurement and simulation of an amplifier configured as a voltage follower gain 1 showing the Bias T fitted to isolate test fixture from Network Analyser

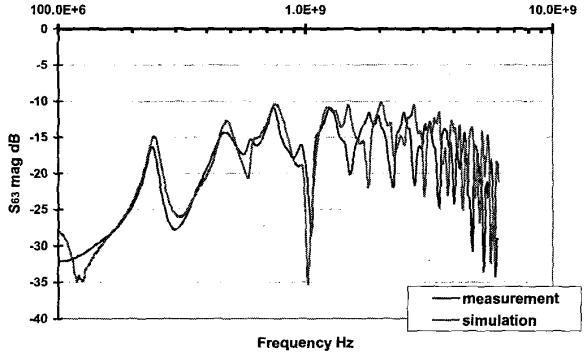

Figure 3 Comparison of S21 measurement and simulation for RF incident into pin 3 and coupling to pin 6 to check model for an amplifier configured as a voltage follower of unity gain

The linear model has been validated by considering more complex circuit configurations and shown to accurately reproduce the behavioural response of a device over the frequency band 100MHz to 6GHz [5]. From the results discussed in the references [5] and [3], it has been shown that:

1. The normalised scattering parameters between two ports of the IC are virtually independent of the operating conditions
2. Under normal power levels, the normalised scattering measurements between two ports change little with incident power, which indicates that the coupling model can be considered linear. The power levels indicated on the Figure 4 relate to the network analyser drive power levels given in Table 1:

Level indicated on graph	Drive level
Low	-10dBm
Med.	0dBm
Mid	8dBm
High	20dBm

Table 1 network analysers drive power levels

It is significant that the measurements carried out on pins 2, 3, 6 and 7 (Figure 4) show no large change in their scattering measurements. However in the case of pin 4 (negative power supply rail) significant changes in its scattering parameters can be seen as the input power is increased (Figure 5). The reason for this change is not known at present. However, the power level for which the change occurs is sufficiently high that this effect can be assumed not to be relevant under expected operating conditions.

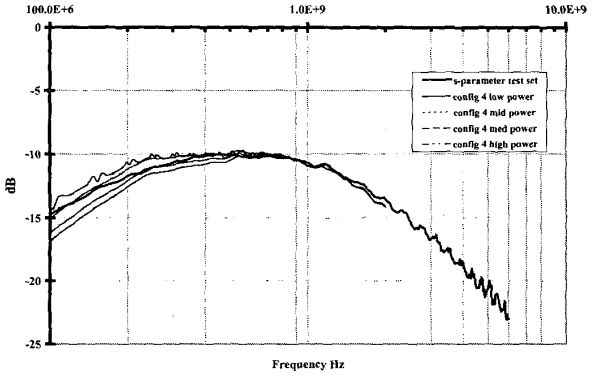

Figure 4 Effect of variation of input power on pin4 S21 -ve supply to pin7 +ve supply

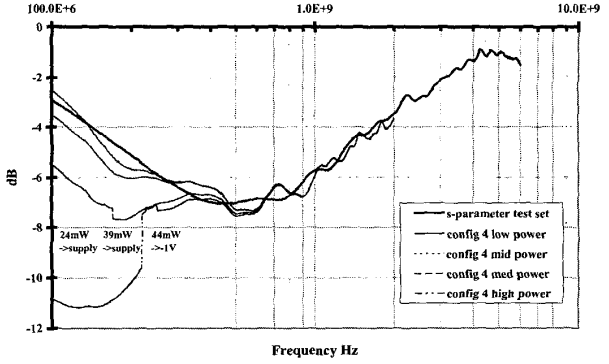

Figure 5 Effect of variation of input power on pin4 S11 -ve supply showing upset at power levels – supply means ± 12V

The results indicate that the RF transmission or propagation is generally due to the device and packaging parasitic. This illustrates an important result since the propagation of RFI through a device seems to be independent of the detail and function of the internal structure of the chip. The results suggest that it may be possible to use circuit analysis programs to predict the effects, in both linear and digital ICs, of RF voltages incident on the pins of the device, without detailed knowledge of the internal structure of the chip. In this paper a model will be illustrated and discussed that will use measurement data to define the transfer functions, between all the pins on the device. This enables the synthesis of a linear model to define the

device propagation characteristics to frequency and time domain RFI waveforms. This is illustrated in Figure 6, and will be used to define the HF model used in this paper.

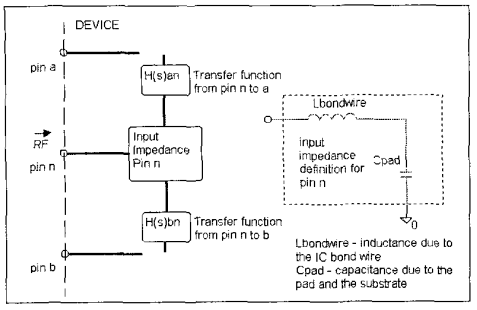

Figure 6 model definition for the transfer function and input impedance between all the pins on the device

Experimental validation of the HF linear model

This part of the paper will define the methodology of the model to evaluate the input impedance and the cross coupling of RFI between the individual pins, according to the model described in Figure 6. To define the input impedance and the coupling or transfer function, measurements were carried out according to [5].

To design a model to define the device transfer function a method has been designed to use a least-mean-squares 'best fit' filter using the measurements. The method is based on a novel application of the Wiener-Hopf equation for signal estimators as described in [8], with the same method described by Levy [9] and used in the Matlab 'Signal processing toolbox' routine 'invfreqs' according to reference [10]. The transfer function of the device can be described as a ratio of polynomials in s, which can be used to determine the time, or frequency response of the device by means of Laplace transforms. The transfer function is of the form

$$H(s)=\frac{b_0+s^1b_1+s^2b_2+\cdots s^{N-2}b_{N-2}+s^{N-1}b_{N-1}+s^Nb_N}{1+s^1a_1+s^2a_2+\cdots s^{N-2}a_{N-2}+s^{N-1}a_{N-1}+s^Na_N} \quad (1)$$

The values a_n and b_n are coefficient multipliers.

The graphs and the pole zero plot indicate the frequency and phase response of the device and will define the transfer function for each pin according to the next set of figures.

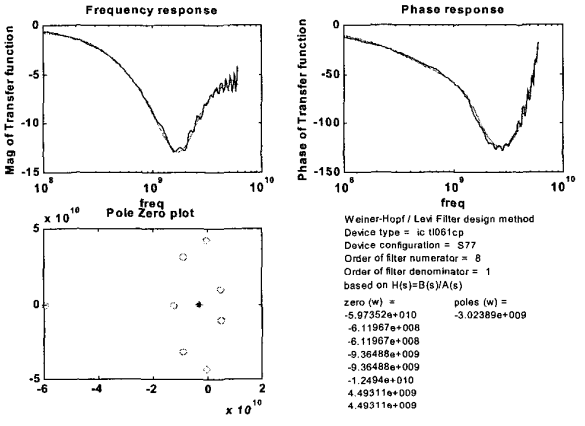

Figure 7 Wiener-Hopf algorithm applied to the device thick line measurement S_{11} for pin 7 with the dotted line the curve fit

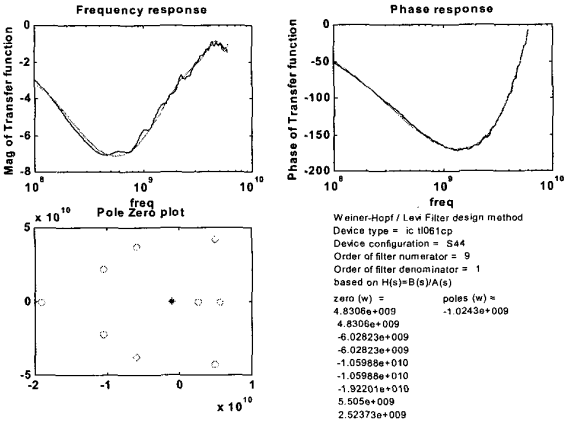

Figure 8 Wiener-Hopf algorithm applied to the device thick line measurement S_{11} for pin 4 with the dotted line the curve fit

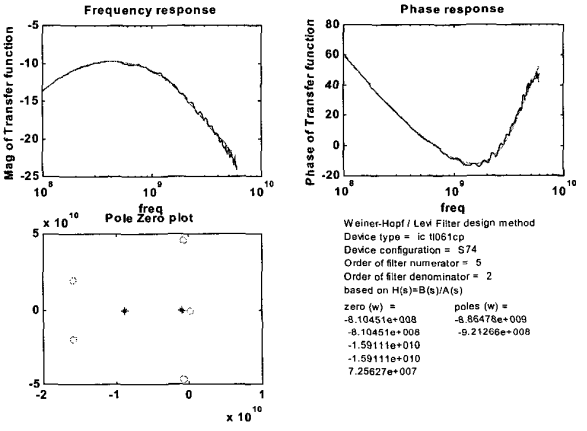

Figure 9 Wiener-Hopf algorithm applied to the device thick line measurement S_{21} between pin 7 and 4 with the dotted line the curve fit

For pin 7 $\rightarrow$ 4 the transfer function in s is

$$H(s)=\frac{2.302e^{-33}+6.546e^{-12}s+0.159s^2+3.194e^9s^2-2.3326e^{17}s^3}{1+9.786e^9s+8.167e^{18}s^2}$$

To implement a circuit model from the transfer function the poles and zeros of the function have to be obtained by factorisation of the quadratics in s-plane form by and displayed in Table 2 and Table 3

$$H(s)=K(s)\frac{(s-z_{s1})(s-z_{s2})(s-z_{s3})\cdots(s-z_{s(N-1)})(s-z_{sN})}{(s-p_{s1})(s-p_{s2})(s-p_{s3})\cdots(s-p_{s(N-1)})(s-p_{sN})} \quad (2)$$

Pin 7	Zeros z_{si}	Poles p_{si}
	$-5.9735e^{10}$	$-3.0239e^9$
	$-6.1997e^8 \pm 4.2634e^{10}i$	
	$-9.3649e^9 \pm 3.1303e^{10}i$	
	$-1.249e^{10}$	
	$4.4931e^{10} \pm 1.0208e^{10}i$	

Table 2 Zero Poles for pin 7 the transfer function in s

Pin 74	Zeros z_{si}	Poles p_{si}
	$-8.1045e^{8}+4.6304e^{10}i$	$-8.8648e^{9}$
	$-8.1045e^{8}-4.6304e^{10}i$	$-9.2127e^{8}$
	$-1.5911e^{10}+1.9897e^{10}i$	
	$-1.5911e^{10}-1.9897e^{10}i$	
	$7.2563e^{7}$	

Table 3 Zero Poles for pin 7 → 4 the transfer function in *s*

This model can be implemented into PSpice using the Laplace Transform (LAPLACE) part.

For large modern devices, the measurement of individual pins will be difficult as the number of measurements on an n pin chip is $n+n^2$. For an 8-pin device we require 72 measurements, for a modern 128-pin device we require 16512 measurements. Another approach is required and a possible solution will be discussed in the next part of the paper.

Since the impedance and transfer functions are of a low order, a model for the input impedance and coupling might be designed using discrete components. To evaluate this methodology, the die of the device tl061cd surface mount JFET operational amplifier has been exposed (Figure 10) and measurements carried out to indicate the size of bonding pads, length of bonding wires and pin separation. The positions of each bonding pad are given in Table 4.

A simple model for the input impedance might be arranged around the inductance of the bonding wire and the capacitance of the bonding pad on the die, illustrated by Figure 11.

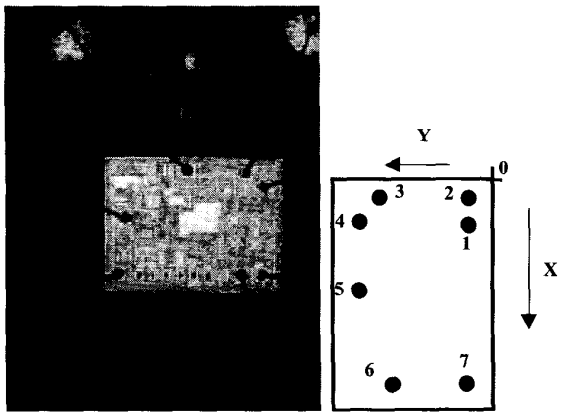

Figure 10 Device tl061cd smt JFET operational amplifier die and pin configuration.

Pin	X (mm)	Y (mm,)
1	0.283	-0.124
2	0.139	-0.115
3	0.131	-0.780
4	0.263	-0.892
5	0.691	-0.901
6	1.157	-0.530
7	1.201	-0.112
8		

Table 4 device pin configuration for each pin – reference point 0 located at bottom right of die.

The inductance of the bond wire may be estimated by considering it as half a circular loop:

$$L = \frac{R\mu}{2}\left[\ln\left(\frac{8R}{a}\right) - 2\right] \quad (3)$$

where R is the radius of the loop formed by the bond-wire, a is its radius, and μ is the permeability of the medium in which the loop is embedded. The radius of the bonding wire for this technology is 12.5μm and the length of the bond-wire l is 1.5-2.5mm giving a loop radius of 0.48-0.8mm. Taking $\mu=\mu_0$ this gives an inductance in the range 1.1-2.1nH.

To calculate the input capacitance of the device, if we assume that the pad forms a simple parallel plate capacitor, and ignore fringing effects:

$$C = \varepsilon_o \varepsilon_r \frac{A}{d} \quad (4)$$

where A is the area of the pad, d is the dielectric thickness, ε_0 is the permittivity of free space and ε_r is the relative permittivity of the dielectric.

The thickness d for this type of technology is 0.5μm and the ε_r has a value of 4 for SiO_2. The pad size is approximately 0.24^0mm, giving a capacitance of 4pF. This model does not take in to account the effect of the device lead frame, which will need further investigation. A simple illustration of this model is illustrated in Figure 11.

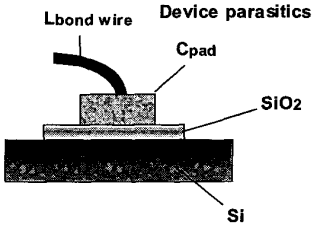

Figure 11 configuration device input characteristic impedance

We also include the series resistance of the bond-wire and a resistor to represent the loss in the silicon, and a parasitic capacitance from the pin to bad in the equivalent circuit shown in Figure 12.

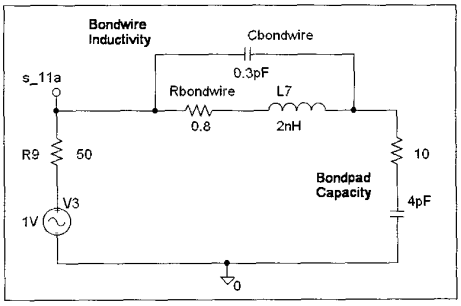

Figure 12 PSpice implementation of the S_{11} value of the device using values equated from equation (1) and (2) to configure pin 7 (positive power rail)

Figure 13 illustrates the comparison of the calculated device parasitics used in the simulation and the measured device scattering parameter S_{11} according to the measurement system in [3].

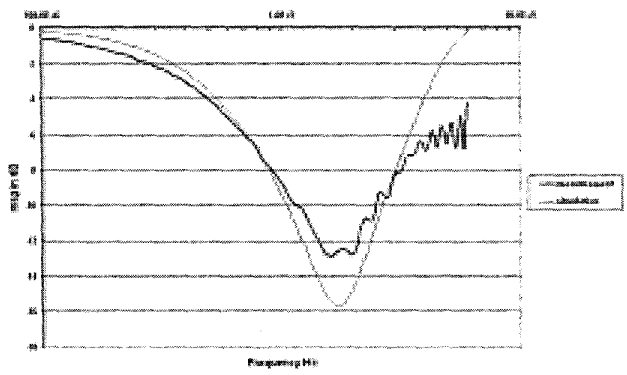

Figure 13 Comparison of the calculated device parasitics used in simulation and the measured device scattering parameter S_{11} for pin 7 of the modelled device.

From this approach the input impedance might be modelled using die measurements. The main future research will be to define the pin-to-pin coupling algorithm to enable an analytical method for the transfer function derived from die measurements and semiconductor physics. Manufacturers IBIS models may also provide some insight into pin properties of unknown IC.

Non-linear parameter measurement

A test circuit has been developed to determine the validity of the non-linear model. The circuit, Figure 14, is an amplifier with a feedback factor, β, which is used in a number of configurations. This was designed around the device test jig described in [3]. The amplifier configurations used are a Voltage follower, a Non-inverting Amplifier, and an Inverting Amplifier. The tests are carried out using a dc Voltage input (V_i) of zero or 200mV which remains constant over the full test.

The amplifier configurations are based on A_{cl} – closed loop gain of the amplifier and a schematic where R_f and R_i are the resistors for feedback and input respectively

Voltage follower $$A_{cl(VF)} = \frac{1}{\beta} = 1 \quad (5)$$

Non-inverting Amplifier $$A_{cl(NI)} = \frac{1}{\beta} = 1 + \frac{R_f}{R_i} \quad (6)$$

Calculations based on

$A_{cl(NI)} = 5$ $R_i = 4.7k\Omega$ $R_f = 18.8k\Omega$

$A_{cl(NI)} = 22.3$ $R_i = 4.7k\Omega$ $R_f = 100k\Omega$

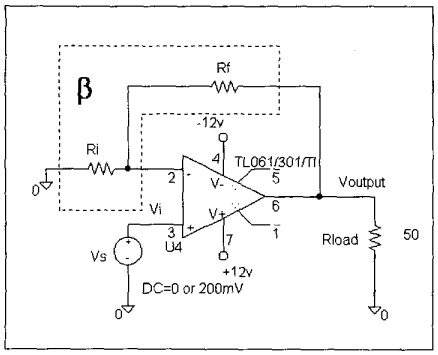

Figure 14 Configuration of Amplifier circuit used.

The RF induced voltages to be used in the LF subsystem, can be derived from direct measurements carried out on the device and used to determine the offset as set of polynomial functions of frequency and incident power or voltage [3]. This is illustrated in Figure 15.

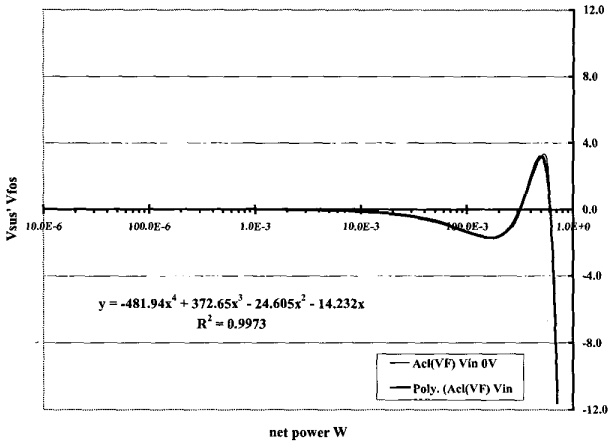

Figure 15 Comparing measured offset voltages and the polynomial approximation of offset voltage with net power for RF injection into Pin 7 of device tl061cp amplifier at 250MHz.

These can be derived by measuring the offset voltage due to the RF against the net RF power levels where V_{fos} is a function of frequency and power. The non-linear equation can be calculated using an n^{th} order polynomial curve fitting routine. Therefor, pin 7 @ 250MHz for input Voltage of constant zero Volts, the equation will be:

$$V_{fos} = -481.94P_{net}^4 + 372.65P_{net}^3 - 24.605P_{net}^2 - 14.232P_{net} \quad (7)$$

The offset voltage is implemented by injecting an input voltage due to the RF V_{ios} into the LF model at the input to the amplifier as shown in Figure 16.

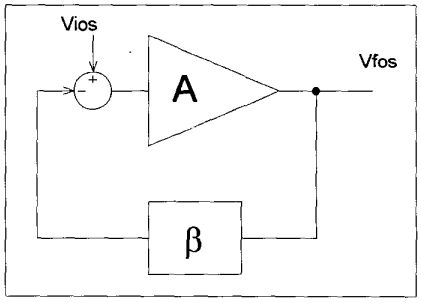

Figure 16 simple configuration of an amplifier A with a feedback of βwhere Vios is input Voltage due to RF and Vfos RF induced offset voltage output

Considering the effect of the input offset on the amplifier output:

$$V_{fos} = AV_{ios} - A\beta V_{fos} \quad (8)$$

$$(1 + A\beta)V_{fos} = AV_{ios} \quad (9)$$

$$V_{fos} = \frac{A}{1 + A\beta} V_{ios} \quad (10)$$

for practical feedback systems Aβ»1 therefore we can derive

$$V_{fos} = \frac{V_{ios}}{\beta} \tag{11}$$

From Equation (11) we can make the assumption that we do not require to know the open loop gain A of the device to determine or model the input offset parameter.

If the amplifier equation is included to equation (11)

$$V_{output} = \frac{V_i}{\beta} + \frac{V_{ios}}{\beta} \tag{12}$$

Figure 17 illustrates the correct assumptions made by equation (12) that the derived output voltage is based on $\mathbf{V_i}$ **plus** $\mathbf{V_{fos}}$ using the circuit described in Figure 14.

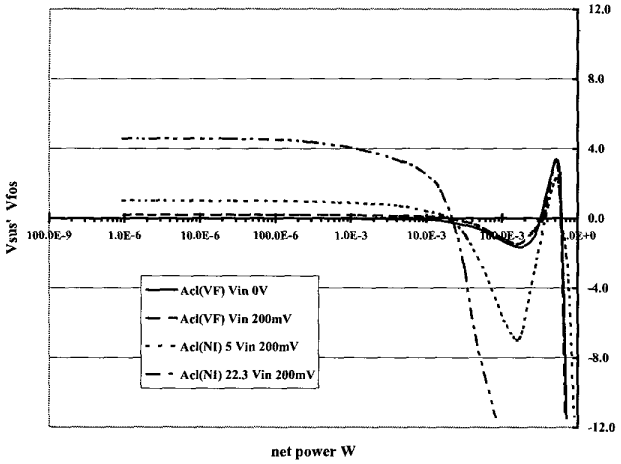

Figure 17 Measured offset voltages using different amplifier gain configuration based on equations (11) and (12).

Conclusions and discussions

The approach presented allows the possibility of predicting the propagation and effect of interference in electronic systems. By the use of a two-level model avoids the difficulty in simulation of the wide disparity in the frequency ranges of out-of-band interference and the operating signals in the circuit. A new method of modelling the Radio Frequency Interference effects on analogue circuits has been presented that incorporates the following features:

1. the model uses a synthesis of a Laplace transfer function or lumped model to represent a subcircuit that describes the input impedance and the radio frequency propagation through the device. This is illustrated by Figure 3 and shows close agreement between the calculated and measured data
2. a non-linear frequency dependent function to generate offset voltages that are injected into the LF part of the model. Simple polynomial functions Figure 15 (7) have been devised, from measurements, to give the correct response on the device from the frequency and power levels of the injected RF.

The method described here could be developed to model the propagation and effect of EMI in systems, whether analogue or digital. Work has been carried out on IC immunity measurements to look at standardisation of RF power levels to upset criteria [11]. The linear propagation model might be used just as a go/no-go detector comparing the power levels from PSpice simulation to this upset criterion for the device i.e. is the RF level on this pin above a susceptibility threshold for upset.

The linear subsystem could be simply interfaced to numerical electromagnetic models to determine its level of susceptibility due to interference from external electromagnetic fields. Numerical electromagnetic tools can be used to determine the induced voltage sources on and s-parameters of PCB tracks and interconnections. These can be combined with the device models to predict interference levels at any node in a system.

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