A Switching Technique for Minimisation of DC-link Capacitance in Switched Reluctance Machine Drives

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***Keywords*: switched reluctance motor drive, switched reluctance machine, dc-link capacitance minimisation**

Abstract

A switched reluctance (SR) machine drive has many advantages over other competing drive technologies in terms of reliability and fault tolerance, which makes it particularly attractive for safety critical applications in more electric aircraft technologies. However, an SR machine drive requires a large DC-link capacitor to buffer the de-fluxing magnetic energy during a phase commutation period and to filter out ac harmonic currents from contaminating the DC supply. This paper describes a switching technique for minimisation of the DC-link capacitance in SR machine drives and presents experimental results from a laboratory demonstrator. The proposed switching method aims to maintain a constant average DC-link current over a switching cycle, thus eliminating commutation-induced low frequency current harmonics. Consequently, the DC-link capacitance can be minimised. The effectiveness of the proposed technique is assessed through filter design and demonstrated by experiments with a dSPACE control platform.

List of Symbols

C	DC-link filter capacitance, F
I_c	Capacitor current, A
I_{dc}	DC-link current, A
$I_{dc,ave}$	Average DC-link current, A
I_{ph}	Phase current, A
$I_{ph,rms}$	Rms value of phase current, A
I_s	Supply current, A
$I_{s,p2p}$	Peak-to-peak phase current, A
L	DC-link filter inductance, H
P	Power, W

R	DC-link filter resistance, Ω
T_c	Period of a pulse width modulation cycle, s
T	Electromagnetic torque, N·m
T_{ave}	Average electromagnetic torque, N·m
T_{p2p}	Peak-to-peak electromagnetic torque, N·m
V_{dc}	DC supply voltage, V
V_c	Voltage across DC-link capacitor, V
$V_{c,p2p}$	Peak-to-peak voltage across DC-link capacitor, V
V_0	Nominal DC-link voltage across capacitor, V
ω^*	Demand speed, r/min
ω	Motor speed, r/min
θ	Rotor angular displacement, mechanical degree

1 Introduction

A switched reluctance (SR) machine drive is a potential candidate for safety critical applications in more electric aircraft technologies, such as a starter/generator system, due to a number of desirable features which include relatively high power density compared to induction machines, high speed, simple construction and their ability to tolerate faults and to operate in high temperature and in harsh environments [1-4]. However, due to doubly salient stator and rotor poles, and discrete phase commutation, significant torque ripple and air-gap radial force pulsation will be generated. Careful electromagnetic and mechanical design is required to minimize resultant noise and vibration. On a different aspect, the de-fluxing magnetic energy released from an outgoing phase winding when being switched off causes significant voltage and current ripples in the DC-link capacitor. The capacitance has to be designed sufficiently large in order to reduce the ripple contents to an acceptable level. Consequently, the DC-link capacitor is one of the most bulky and unreliable parts in an SR machine drive system, and it seriously compromises the attainable system reliability and compactness [5].

It is possible to employ an actively controlled front-end converter or power factor corrector (PFC) to reduce the capacitor size, as has been proposed for both SR and other types of drive systems [6-11]. However, this increases system complexity, size, cost and weight as well as compromises system efficiency. An auxiliary winding and a capacitor are adopted in [12] to buffer and dissipate the de-fluxing energy. In this scheme, a part of the de-fluxing energy is absorbed by the auxiliary winding and the capacitor, instead of by the DC-link capacitor. The converter circuit is specially designed to cope with these changes. The average torque is increased since the energy in the auxiliary winding is utilized. However, the extra winding increases the cost, alters the machine design and reduces power density.

Two techniques which do not require additional winding and circuit components for minimisation of the DC-link capacitance in an SR machine drive have been reported. The duty ratio of the phase currents is controlled in [13] to balance the power transfer between the outgoing phase and the incoming phase during a phase commutation whilst the voltage across the DC-link capacitor is controlled within a hysteresis band in [14]. When the capacitor voltage is higher than the upper voltage band, the de-fluxing current of the outgoing phase will not be allowed to flow back to the DC supply. However, both techniques are only effective in reducing peak-to-peak DC-link voltage ripple when the DC power supply is derived from a diode rectifier and when there is no inductive component between the DC power source and the DC-link capacitor. In many applications, however, the DC supply is derived from a DC power network and an inductive filter is often necessary to meet power quality and EMC requirements or the inductive effect of cables is not negligible. In addition, the current drawn by the SR drive from the DC source with these techniques contain significant harmonics at integer multiple of commutation frequency. Consequently, the power quality may be compromised and do not meet certain standards.

This paper proposes a new switching technique for minimisation of DC-link capacitance in SR machine drives. This is achieved by maintaining a constant average DC-link current over a switching cycle. The proposed technique has been implemented in a laboratory demonstrator and validated experimentally. The rest of the paper is organized as follows: Section 2 describes the principle of operation. Section 3 presents simulation results and comparisons with typical techniques in the current state-of-the art. Section 4 assesses the impact of the proposed techniques on the reduction of capacitor and filter size. Section 5 presents experimental results before drawing conclusion in Section 6.

2 Principle of operation and control modes

Figure 1 (a) shows the schematic of an SR machine drive in which asymmetric H-bridges are connected to the DC power source via a LRC filter which represents the combined effect of the cable and filter. In some applications, the DC power is derived from a diode rectifier, and a simplified representative circuit is shown in Fig. 1 (b).

When conventional hysteresis current control is employed the resulting DC-link current, $I_{dc,}$ contains high frequency switching harmonics as well as commutation-induced low frequency harmonics which are caused by fluxing of the incoming phase and de-fluxing of the outgoing phase during a commutation period.

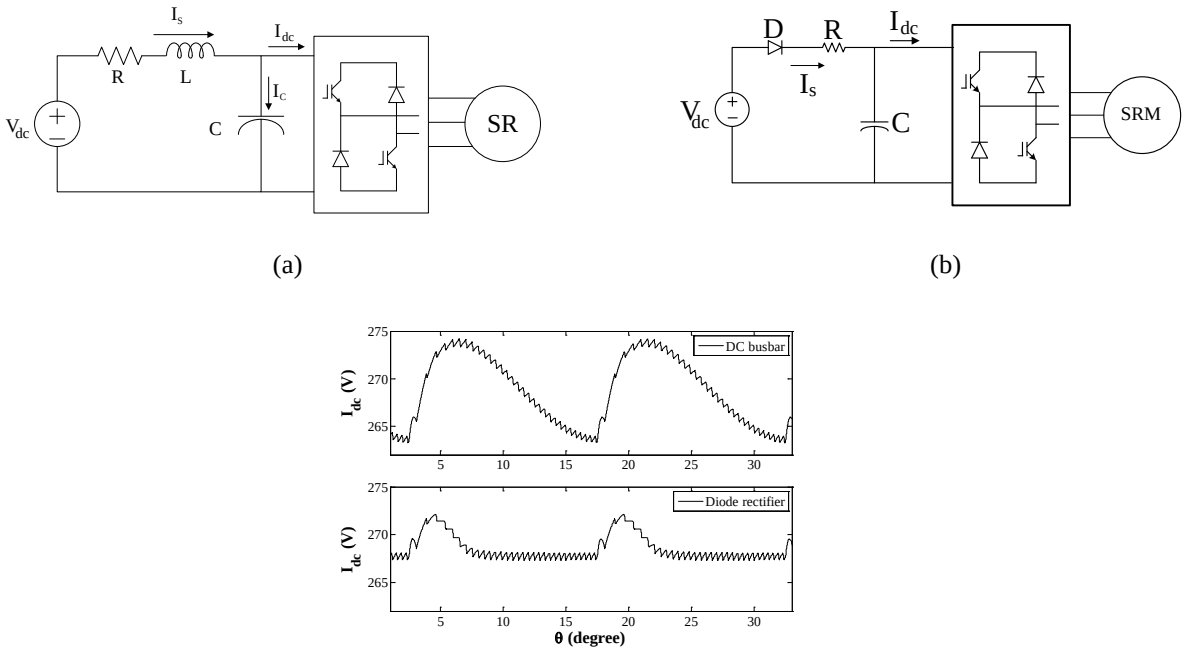


Fig. 1 Schematic of SR drive supply circuits and DC-link capacitor voltage (a) DC bus bar supply circuit, (b) Simplified diode rectifier supply circuit, (c) DC-link capacitor voltages

The DC-link current harmonic is therefore composed of high frequency switching harmonics and low frequency commutation harmonics. This causes significant voltage ripples across the DC-link capacitor as shown in Fig. 1 (c) for the two supply-filter circuits in Figs. 1 (a) and (b), and current ripples in the filter inductor or the DC supply. The frequency of the commutation harmonics decreases with machine speeds. At low speeds, a large DC-link capacitor is

necessary to limit the voltage and current ripples below their permissible levels. Thus, commutation-induced low frequency current harmonics are the fundamental cause of the large capacitor size in SR drives.

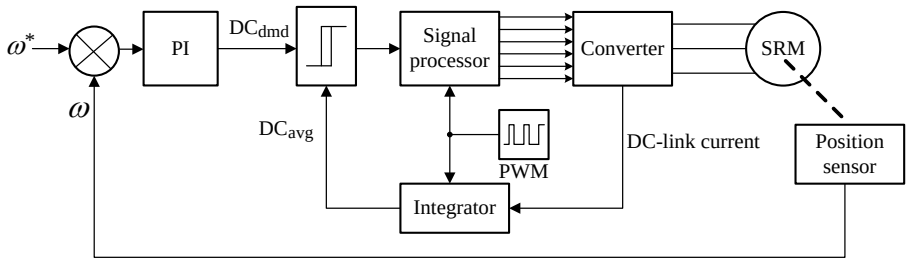


Fig. 2. Control diagram of proposed method

However, if the power transfer between the DC-link and the SR converter is kept constant, the voltage and current ripples can be greatly reduced. The new switching technique for SR machine drives is based on this concept. The DC-link current is measured and integrated over a switching period. The resultant average DC-link current is compared to the demand and the output of the comparison is used to control the switching process as schematically illustrated in Fig. 2.

To keep a constant average DC-link current during the operation, the proposed switching technique operates in two modes: one-phase active mode and commutation mode, depending on the status of the SR drives.

2.1 One-phase active mode

This mode arises when a phase commutation has been completed and only one phase is excited in a dwell period.

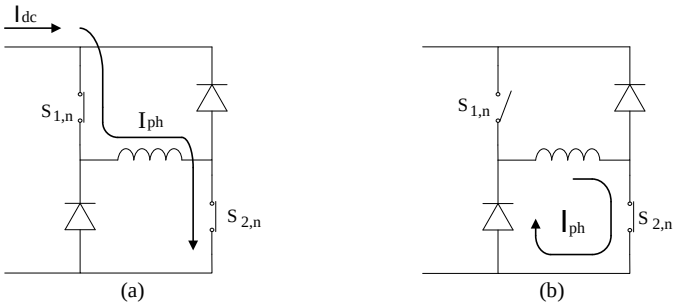


Fig. 3. One active phase mode (a) turn on (b) turn off in freewheeling mode

At the beginning of a switching cycle, two active switches of the converter are turned on, as shown in Fig.3 (a). The phase current rises and so does the dc-link current. The dc-link current is integrated to obtain the average DC-link current (DC_{avg}) as follows:

$$DC_{avg} = \frac{1}{T_c}\int_0^t I_{dc}\,dt \qquad (1)$$

where T_c is the pulse width modulation (PWM) period. Since T_c is constant, DC_{avg} increases with the time integration of I_{dc}. When it reaches the demand value, DC_{dmd}, one of the active switches, e.g, $S_{1,n}$, turns off and the converter now

operates in a free-wheeling mode, as shown in Fig.3 (b). The resulting DC-link current becomes zero, and the integrator output is maintained at DC_{dmd}. The switching process repeats in each PWM cycle by resetting the integrator at the start of each cycle.

2.2 Commutation mode

A commutation mode takes place when an outgoing phase is switched off, releasing the de-fluxing energy and an incoming phase is switched on. In this mode, the switches of both the incoming and outgoing phases are controlled by comparison of the demand and the output of the DC-link current integrator in the similar manner as those described previously.

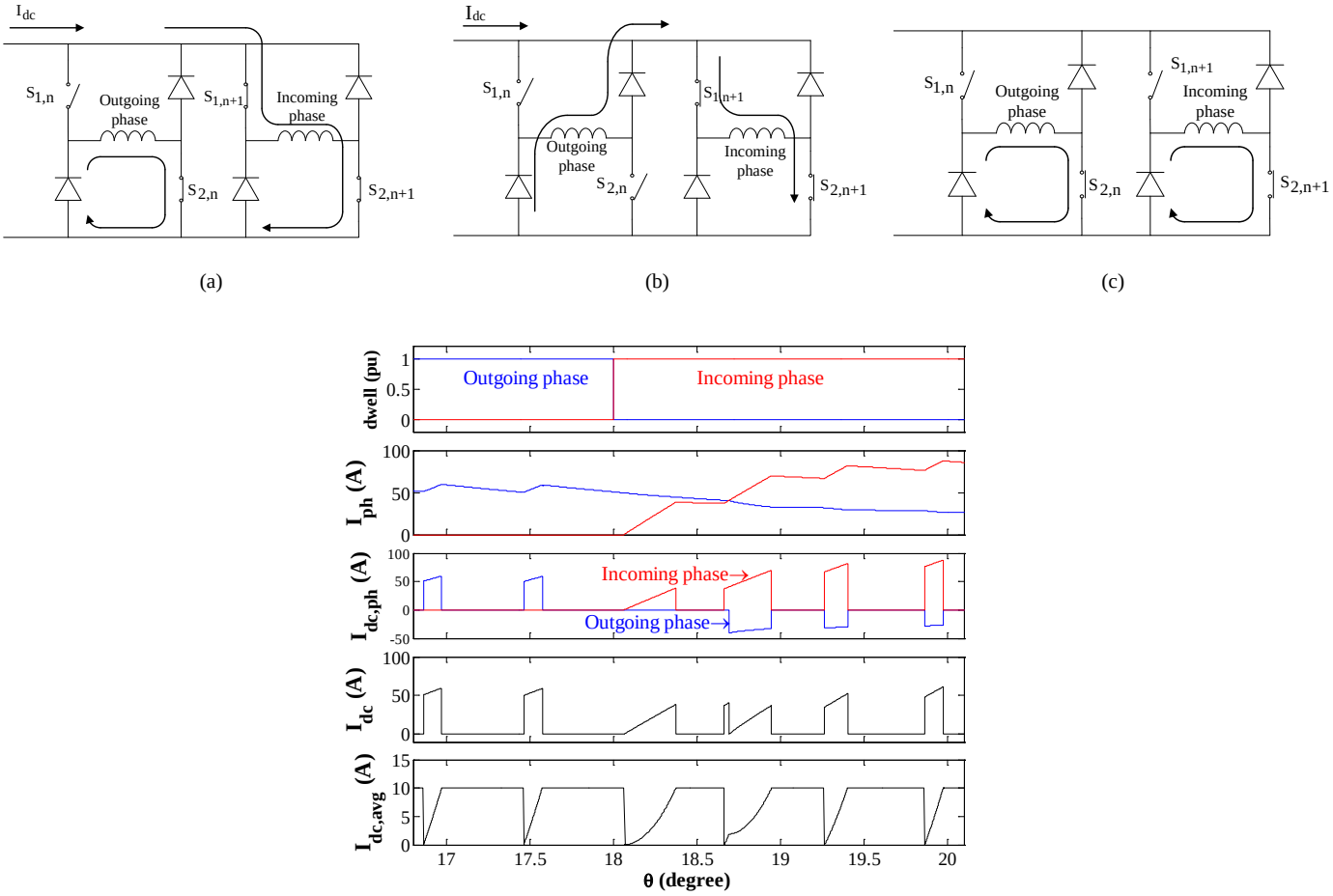


Fig. 4. Commutation mode and resultant waveforms (a) incoming phase turned on, outgoing phase in freewheeling mode, (b) incoming phase turned on, outgoing phase turned off, (c) both incoming phase and outgoing phases in freewheeling mode, (d) waveforms of phase current, dc-link currents contributed by incoming and outgoing phases, net dc-link current and integrator output

However, if the current in the incoming phase is less than that of the outgoing phase, the outgoing phase is turned off in the freewheeling mode, as shown in Fig. 4 (a). Otherwise, it is turned off in the hard switching mode as shown in Fig. 4 (b). The de-fluxing energy of the outgoing phase is therefore fed to the incoming phase. When the output of the integrator or the average DC-link current reaches the demand DC_{dmd}, both the incoming and outgoing phases are turned off in the freewheeling mode, as shown in Fig. 4 (c). The process repeats in each PWM cycle. Thus the de-fluxing

energy released by the outgoing phase is either dissipated by itself through freewheeling or fed to the incoming phase. Consequently, the average DC-link current over a PWM cycle is maintained constant during phase commutations.

The resultant waveforms of the phase currents and DC-link currents in one phase active mode and commutation mode are shown in Fig. 4 (d). In one phase active mode where the rotor angle θ is less than 18 mechanical degrees, the DC-link current flows to the active phase when the integrator output has not reached the demand. During phase commutation, the DC-link current is contributed by the incoming phase only, when the current in the outgoing phase is greater than that in the incoming phase. When this condition is reversed, the de-fluxing energy of the outgoing phase is allowed to feed into the incoming phase, and the net DC-link current drawn by the converter is reduced. The DC-link current becomes zero in both modes when the integrator output reaches the demand. Consequently, the average DC-link current over a switching cycle is kept constant.

3 Simulation studies

The proposed switching technique, referred to as DC-link current integration control (DLCIC), is further investigated by extensive simulations in MATLAB/Simulink environment in conjunction with SimPowerSystem™ Toolbox. The schematic of the simulation block diagram is shown in Fig. 5. For the purpose of comparison, simulations were also performed for the conventional hysteresis current control (HCC), the power balance control (PBC) [13] and the voltage hysteresis control (VHC) [14]. The parameters of the SR machine and the DC filters used in the simulation are listed in Table 1. The SR machine model is derived from electromagnetic finite element analysis. The switching frequency is set at 10 kHz and the machine speed is 1000 r/min.

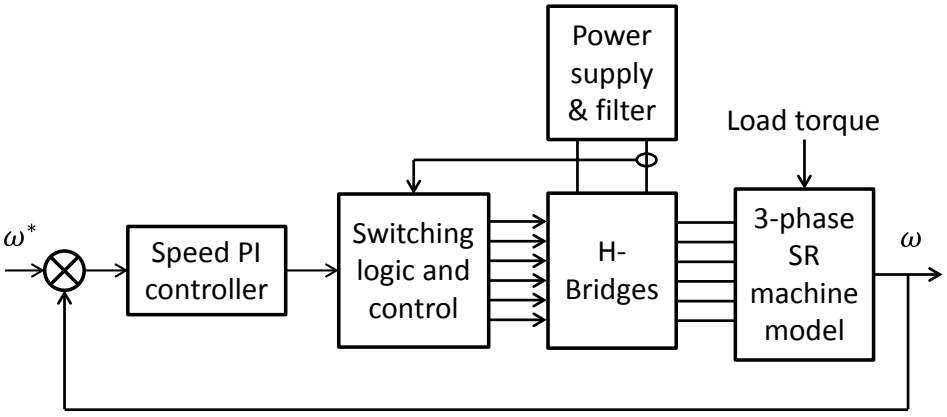


Fig. 5 Schematic of simulation block diagram

TABLE 1
Parameters of SR machine and filter

SR Machine		Filter	
Number of phases	3	Resistance (Ω)	0.1
Number of stator poles	8	Inductance (mH)	0.46
Number of rotor poles	6	Capacitance (μF)	1000
Rated power (kW)	15	DC voltage supply (V)	270
Rated torque (N·m)	20	Maximum speed (r/min)	12000

Each technique was simulated with two supply circuits, DC bus bar circuit, and diode rectifier circuit, as shown in Figs. 1 (a) and (b), respectively.

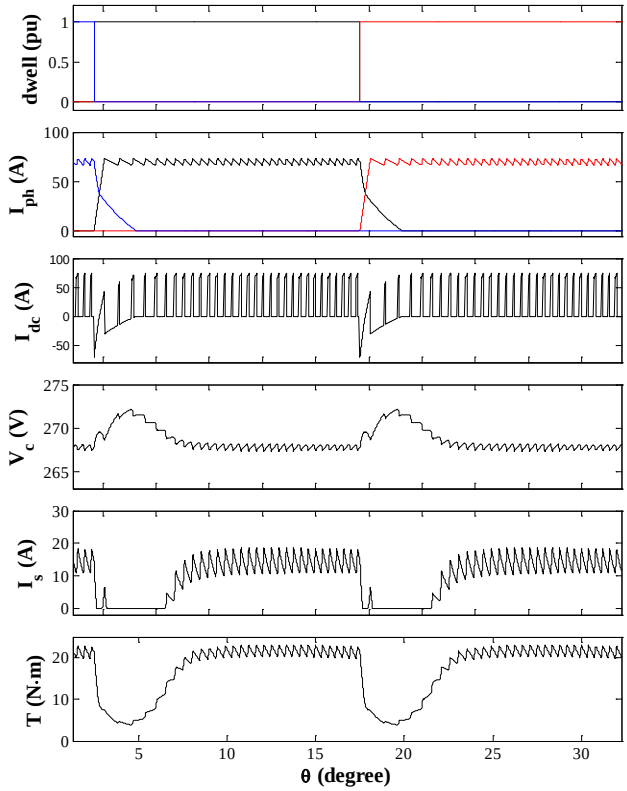
Fig. 6 (a) shows the simulation results of the HCC with the diode rectifier supply circuit. As will be seen, the negative DC-link current as a result of de-fluxing during the commutation period gives rise to a significant increase in the capacitor voltage. Consequently, the diode rectifier will be reverse-biased and the supply current, I_s, becomes zero during the commutation period. Both the capacitor voltage, V_c, and supply current, I_s, contain significant harmonics at the commutation frequency and its integer multiples. The peak-to-peak voltage ripple is 4.82 V.

Fig. 6 (b) shows the simulation results of the VHC with the diode rectifier supply circuit. Due to voltage hysteresis control, de-fluxing energy is not allowed to feed back to the DC-link when the capacitor voltage is greater than a specified upper band. As a result, the capacitor voltage is kept within the hysteresis band, but harmonics in the supply current is still very significant. In addition, the current tail of the outgoing phase is slightly increased as compared to that of the HCC due to the fact that the outgoing phase is turned off in freewheeling mode when the capacitor voltage is greater than the specified upper band.

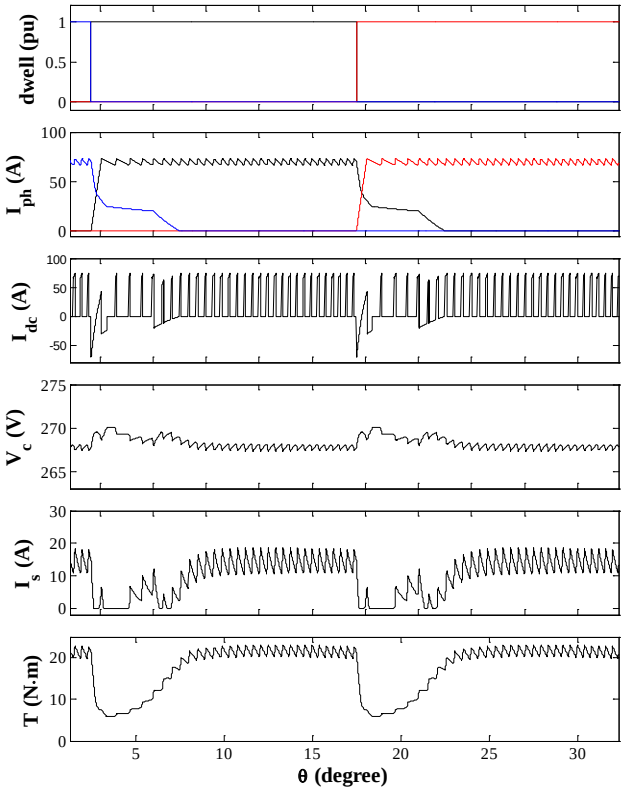
Fig. 6 (c) shows the simulation waveforms of the PBC when supplied by the diode rectifier. The resultant voltage ripple is much lower than that of the HCC as the duty ratio of the phase currents is controlled to balance the power transfer between the outgoing phase and the incoming phase during commutation. Similar to the VHC, significant supply current harmonics is present, and the commutation period is slightly longer than that of the HCC.

The simulation results of the proposed DLCIC supplied from the same diode rectifier circuit are shown in Fig. 6 (d). It is evident that both the capacitor voltage and supply current only contain harmonics at switching frequency and the harmonics at integer multiple of the commutation frequency have been virtually eliminated. Another noticeable difference from the other three techniques is that the current tail in the outgoing phase is much longer and the phase current is not constant, being larger in the first half of the dwell period. Both are due to the fact that the de-flux energy in the outgoing phase is only allowed to feed into the incoming phase under the DLCIC. This eliminates negative DC-link current, but gives rise to longer commutation periods.

Table 2 compares the performance indicators among the techniques being studied. It is evident that the DLCIC yields the lowest voltage ripple, being 5 times and 3 times lower than that of the HCC and the other two, respectively. It is also evident that the peak-to-peak torque ripples which result from all the techniques are quite high, due to relatively lower number of phases being employed in the SR machine. Nevertheless, the torque ripple of the DLCIC is lower than that of the HCC and VHC, and slightly greater than that of the PBC.



(a)



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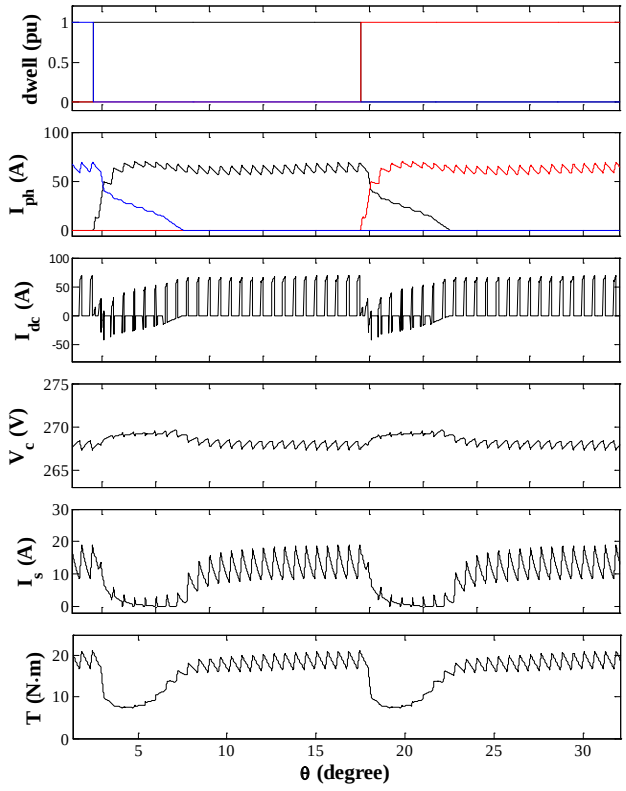

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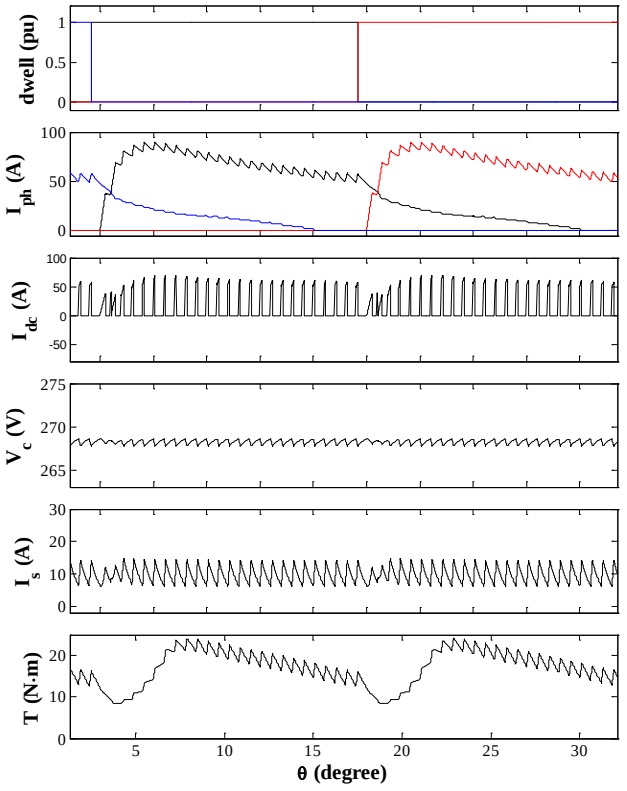


(d)

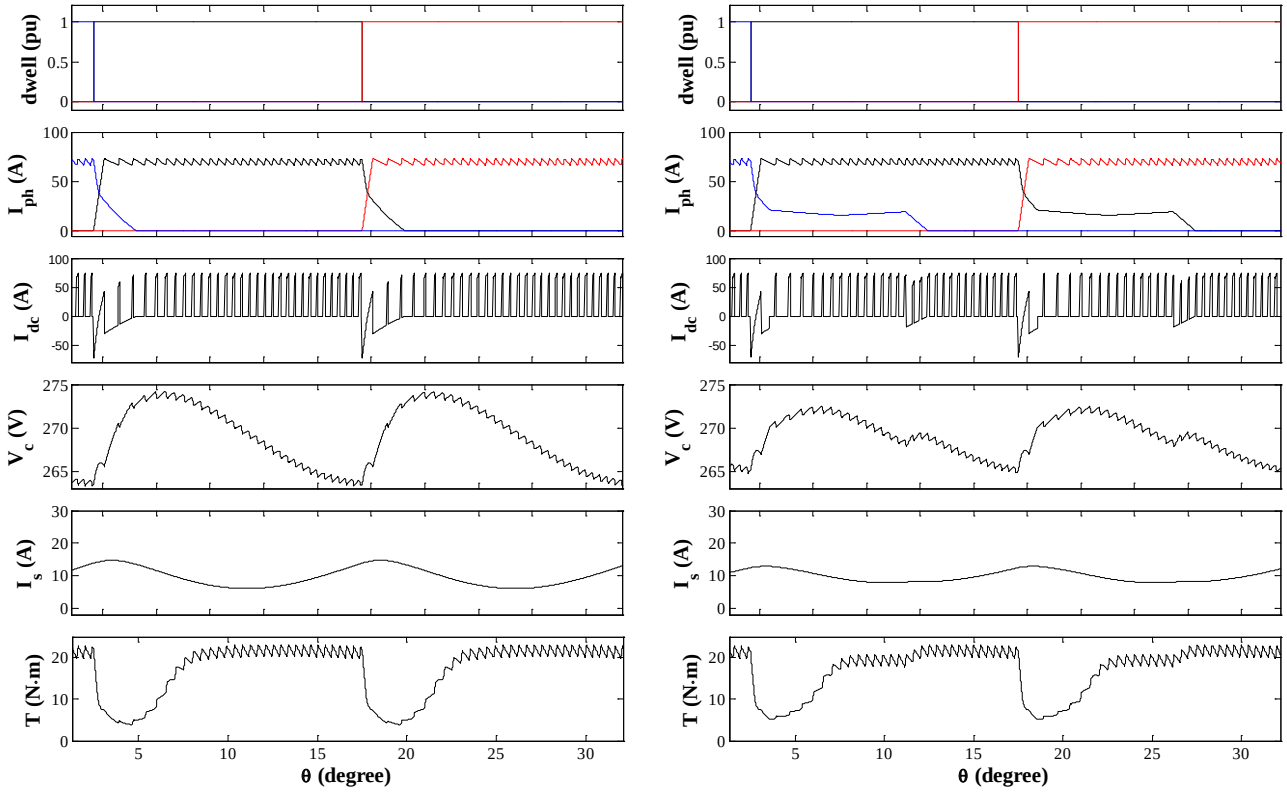
Fig. 6 Simulated waveforms of four switching control schemes of SR converter at 1000 r/min supplied from diode rectifier (a) HCC, (b) VHC, (c) PBC, (d) DLCIC

The supply current ripple from the DLCIC is also much lower and mainly due to PWM switching. The high frequency current harmonics can be easily filtered as will be discussed subsequently. While the capacitor voltage ripples of the VHC and PBC are lower than that of the HCC, their current ripples are still as high as that of the HCC.

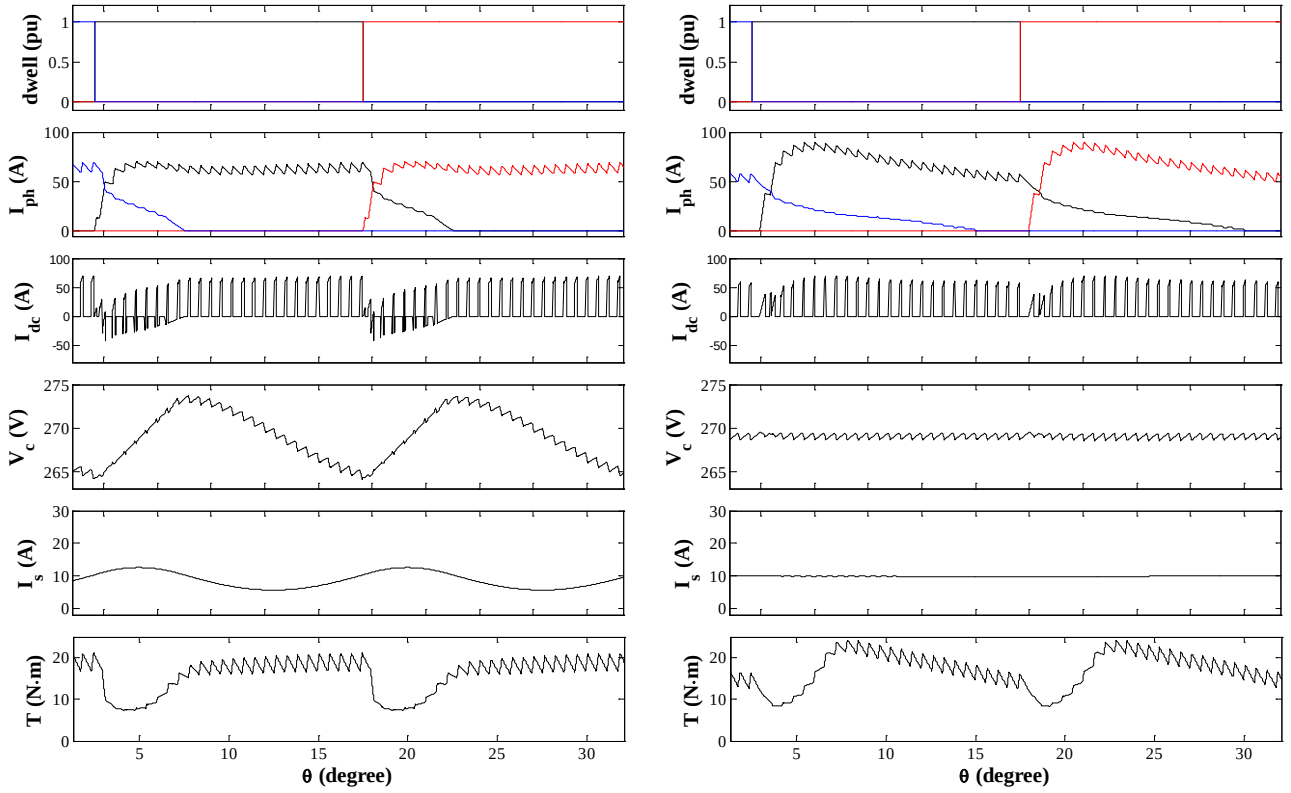
From Table 2, the rms phase current, the average DC-link current, and the average torque of all techniques are close except for the PBC whose values are slightly lower. The torque per rms phase current which is indicative of efficiency is also close albeit the value of the DLCIC is marginally lower due to its longer current tail in the outgoing phase.

TABLE 2
Comparison of performance indicator from diode rectifier supply circuit

Performance	HCC	VHC	PBC	DLCIC
$V_{c,p2p}$ (V)	4.82	2.68	2.35	0.89
$I_{s,p2p}$ (A)	18.56	18.56	18.86	8.77
$I_{dc,avg}$ (A)	9.74	9.98	8.77	9.83
T_{avg} (N·m)	17.08	17.54	15.73	17.03
T_{p2p} (N·m)	19.24	17.24	13.35	15.93
$I_{ph,rms}$ (A)	40.41	40.75	37.18	40.77
$T/I_{ph,rms}$ (N·m/A)	0.423	0.430	0.423	0.418



(a) (b)



(c) (d)

Fig. 7 Simulated waveforms of four switching control schemes of SR converter at 1000 r/min supplied from DC bus bar (a) HCC, (b) VHC, (c) PBC, (d) DLCIC

Simulations were repeated with the DC bus bar supply circuit shown in Fig. 1 (a) under the same operating condition. Fig. 7 (a) shows the resultant waveforms of the HCC. As will be seen, the dwell angle, the phase current, the dc-link current and torque waveforms are essentially the same as those in Fig. 6. However, the absence of diodes allows the de-fluxing energy being stored in the filter inductor or exchanged with the DC supply. The resulting capacitor voltage ripple is increased and the supply current (I_s) also contains commutation induced low frequency harmonics.

Figure 7 (b) and Figure 6 (c) show the waveforms which result with the VHC and PBC, respectively. Compared to the waveforms in Figs.6 (b) and (c) obtained from the diode rectifier supply circuit, the capacitor voltage ripple is increased while supply current ripple is reduced, due to the fact that the energy in the DC-link can be either stored in the inductor or exchanged with the DC supply. This implies that the ability of the VHC and PBC to minimise the capacitor voltage ripple in the DC bus bar circuit is not as good as that in the diode rectifier circuit. In addition, the commutation period of the VHC is also noticeably increased.

Fig. 7 (d) shows the simulated waveforms of the DLCIC from the DC bus bar circuit. They are virtually the same as those with the diode rectifier circuit except that the switching harmonics in the supply current is significantly reduced by the filter inductor.

Table 3 summarises the performance indicators of the simulated techniques. Due to the filtering effect of the inductor, the supply current ripple of all techniques is reduced, compared with those from the diode rectifier circuit. In

particular, the current ripple of the DLCIC is more than an order of magnitude lower than those of the other three. In contrast, the capacitor voltage ripple has been increased except for the proposed DLCIC. The voltage ripples of the HCC and PBC are similar while the voltage ripple of the DLCIC is also an order of magnitude lower.

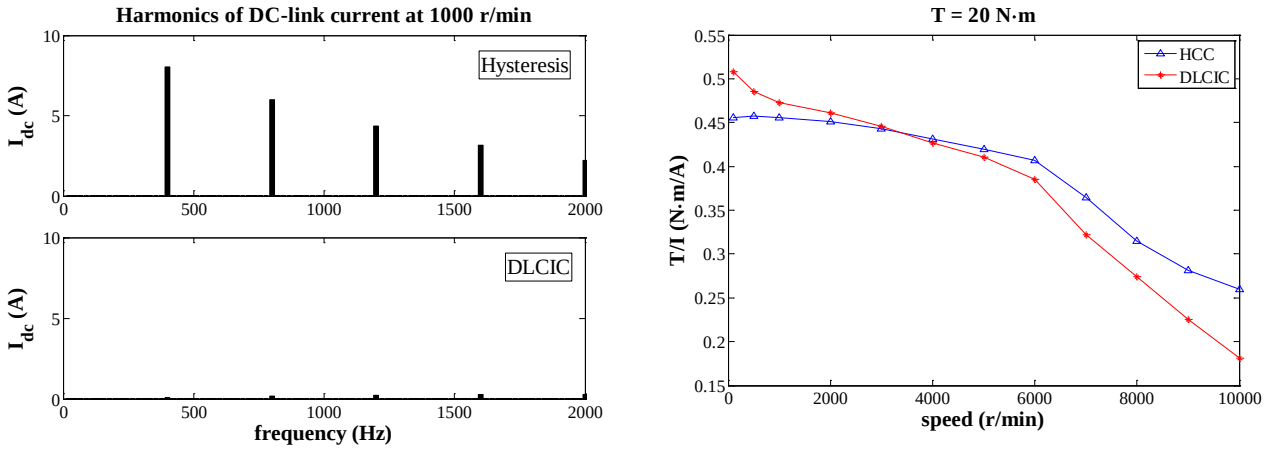
The average torque per rms current of the DLCIC is slightly low than that of the HCC and PBC because the longer current tail of the outgoing phase. However, the difference is very small, being around 2%.

TABLE 3
Comparison of performance indicator from dc bus bar supply circuit

Performance	HCC	VHC	PBC	DLCIC
$V_{c,p2p}$ (V)	10.96	7.70	9.62	1.03
$I_{s,p2p}$ (A)	8.73	5.11	6.94	0.33
$I_{dc,avg}$ (A)	9.75	9.82	8.77	9.86
T_{avg} (N·m)	17.10	16.99	15.73	16.99
T_{p2p} (N·m)	19.24	17.90	13.88	16.44
$I_{ph,rms}$ (A)	40.42	41.09	37.18	41.06
$T/I_{ph,rms}$ (N·m/A)	0.423	0.414	0.423	0.414

It follows that the proposed technique is very effective with both the diode rectifier and DC bus bar supply circuits in minimising the capacitor voltage and supply current ripples.

Fig. 8 (a) compares DC-link current spectrums of the HCC and DLCIC. The commutation frequency of the machine at a speed of 1000 r/min is at 400 Hz. It is evident that the current spectrum of the HCC contains harmonics at the integer multiples of the commutation frequency while the harmonics of the DLCIC at these frequencies are virtually zero.



(a) (b)

Fig. 8 Comparison of DC-link current harmonics and average torque per rms phase current between DLCIC and HCC. (a) DC-link current in the commutation frequency range, (b) average torque per rms phase current

The average torque per rms phase current of the proposed technique can be improved by optimizing the turn-on and turn-off angle as has been done for the HCC and other two techniques [15][16]. Fig. 8 (b) compares the average torque per rms ampere of phase current between the DLCIC and the HCC. As can be seen, when the speed is below 3000 r/min, the torque per ampere in rms phase current of the DLCIC is higher than that of the HCC because the optimal dwell period of the DLCIC at low speeds is now shorter than that of the hysteresis. Better torque production capability of the DLCIC can also be understood from the fact that a significant amount of de-fluxing energy is fed into the incoming phase. Consequently, the torque is boosted.

When the speed is greater than 3000 r/min, however, the torque per ampere of the DLCIC becomes lower than that of the HCC because the current tail of the DLCIC is longer with further advance in the turn-on angle. This leads to a small negative torque due to longer current tail, and hence reduction in the average torque. Therefore, the proposed technique can be used in conjunction with the HCC. When speed is below 3000 r/min DLCIC will be used otherwise the HCC used. The change of the switching techniques can be easily managed by a digital controller.

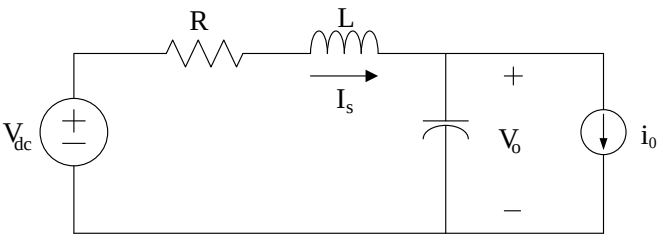
4 Capacitor sizing

Since frequencies of commutation induced voltage and current ripples can be very low at low operating speeds, the SR drive will require a very bulky filter to satisfy power quality requirements in aerospace applications, such as those specified in [17] and [18] when employing the HCC. By combining the DLCIC with the HCC, the minimum operating speed of HCC has been increased to 3000 r/min for the SR drive under study and the resulting commutation frequency of the drive is 1200 Hz. Further, since the voltage and current harmonics of the DLCIC is at a much high PWM frequency (10 kHz), a filter designed to satisfy power quality at 1200 kHz for the HCC operation will be sufficient for DLCIC operation at lower speeds. Hence, the worst scenario for the filter design is HCC operation at 3000 r/min for the SR drive under study.

It is essential that EMI noise of a SR converter is sufficiently attenuated by a filter. However, such a filter design also needs to ensure drive system stability, as the tightly regulated converter behaves like a constant power load and exhibits negative impedance at the input terminal of the converter [19]-[21]. The representative circuit with the 2^{nd} order LRC filter is illustrated in Fig. 9 (a), where the constant power load is represented by the current source i_0. The transfer function of the system is expressed by

$$\frac{V_o}{V_{dc}} = \frac{1/LC}{s^2 + \left(\frac{R}{L} - \frac{P}{V_o^2}\right)s + \left(\frac{1}{LC} - \frac{PR}{V_o^2 LC}\right)} \tag{2}$$

where P is the input power to the drive.



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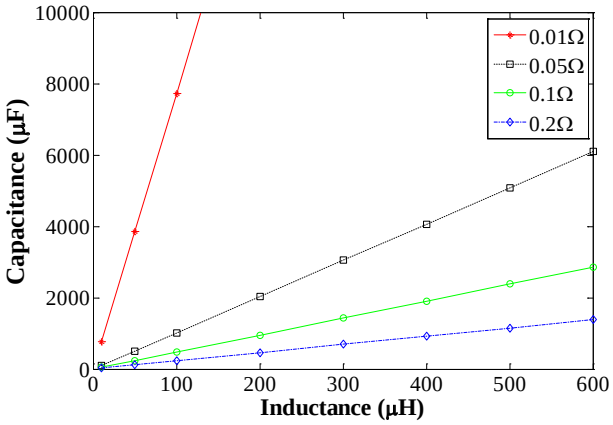
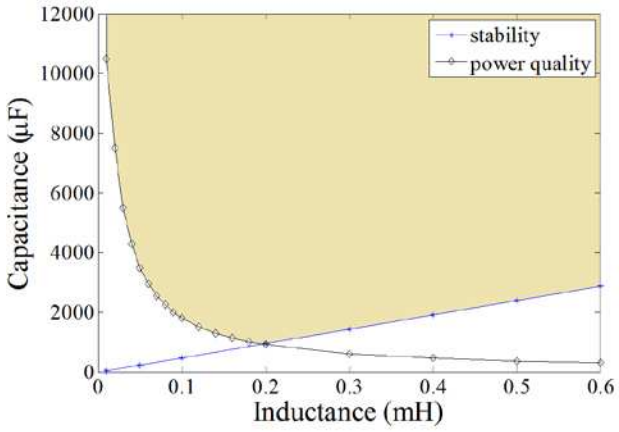




(b) (c)

Fig. 9 Stability and power quality constraints for filter design (a) Equivalent circuit with constant power load, (b) Stability lines with varied input resistances, (c) Stability line and power quality boundary when R = 0.1 Ω.

The stability requirement of eqn. (2) can be expressed by a linear relationship between the filter capacitance and inductance for a minimum system damping of 0.03 [22] for a given R at the nominal supply voltage of 270V, as shown in Fig. 9 (b) where the filter resistance R is varied from 0.01, 0.05, 0.1 and 0.2 Ω. For a given R, any combination of C and L above the corresponding line will satisfy the stability requirement.

To satisfy the power quality the variation of the minimum capacitance as a function of inductance for a given R, which meets 3 conditions listed below:

(i) peak-to-peak capacitor voltage is less than 10% of the supply voltage;

(ii) harmonic spectra of normalized capacitor voltage are within MIL-STD-704F standard [17]; and

(iii) harmonic spectra of normalized supply current are within MIL-STD-416E standard [18].

was obtained by simulations.

The power quality line for HCC operation at 3000 r/min is plotted together with the stability line for R = 0.1Ω in Fig. 9 (c). The intersection of the two lines represents the best combination which satisfies both the power quality and stability requirements.

To obtain a filter design with minimum weight, the filter weights which results with the four resistor values are estimated. The resistor weight is estimated by a range of power dissipation from a suitable commercially available

power resistor series. The inductor weight is minimized and then calculated by an optimal design procedure described in [23 - 24]. The capacitor weight is estimated according to the data sheet of a suitable commercially available metal film capacitor series which has good reliability at the nominal voltage for safety critical applications.

The weights of all filter components are given in Table IV. If the SR drive employs the HCC and operates at a minimum speed of 100 r/min, the resultant filter parameters and weights which satisfy both the power quality and stability are given in Table V for comparison purpose. From Tables 4 and 5, the minimum filter weight is obtained with R = 0.1Ω. It is also evident that the proposed technique in combination with the HCC yields a minimum filter weight of 3.74 kg, which is almost 20 times less than that of the HCC operation. It should also be noted that the smaller filter size with the proposed control is conducive to significant cost reduction.

TABLE 4
Filter Component Weight with Combined DLCIC and HCC Control

Component		Weight (kg.)	Total weight (kg.)
R	0.01Ω	0.05	
L	0.048mH	0.25	9.55
C	3760 µF	9.25	
R	0.05Ω	0.19	
L	0.134mH	0.60	4.2
C	1361 µF	3.41	
R	0.1Ω	0.51	
L	0.195mH	0.86	3.74
C	933 µF	2.37	
R	0.2Ω	1.22	
L	0.282mH	1.25	4.16
C	653 µF	1.69	

TABLE 5
Filter Component Weight with HCC

Component		Weight (kg.)	Total weight (kg.)
R	0.01Ω	0.05	
L	0.89mH	4.56	172.2
C	68870 µF	167.60	
R	0.05Ω	0.19	
L	0.25mH	16.19	77.13
C	24934 µF	60.75	
R	0.1Ω	0.51	
L	3.60mH	26.80	69.17
C	17170 µF	41.86	
R	0.2Ω	1.22	
L	5.17mH	42.88	72.89
C	11797 µF	28.79	

5 Experimental validation

The proposed switching technique for minimising the DC link capacitance has been implemented and tested. Fig. 10 shows the testing rig of the experimental SR motor drive system whose parameters are given in Table 1. The objective of the experiment is to verify that the proposed switching technique can be realized in a practical system for an effective reduction of the DC-link voltage ripple hence minimising the required DC-link capacitance when compared with the conventional hysteresis control. The motor is loaded in the experiment by an induction machine based dynamometer at its rated torque of 4 N·m.

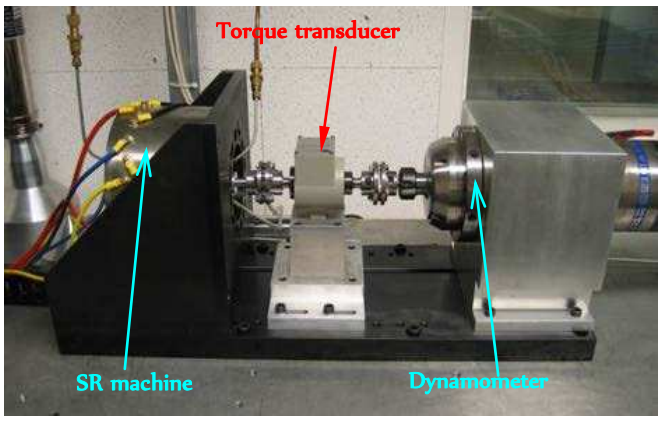


Fig. 10 Experimental set-up

The SR converter is comprised of 3 standard IGBT modules. Each module uses 2 active switches and 2 diodes to form an asymmetric H-bridge. The phase current transducer and the DC-link capacitor are also integrated in the converter module. The DC-link capacitor bank contains eight 40-μF metal film-foil capacitors with a total capacitance of 320 μF. The capacitors are installed beneath the IGBT modules via two planar bus bars. The DC-link current is reconstructed from phase current measurements and converter switching states according to eqn. (3):

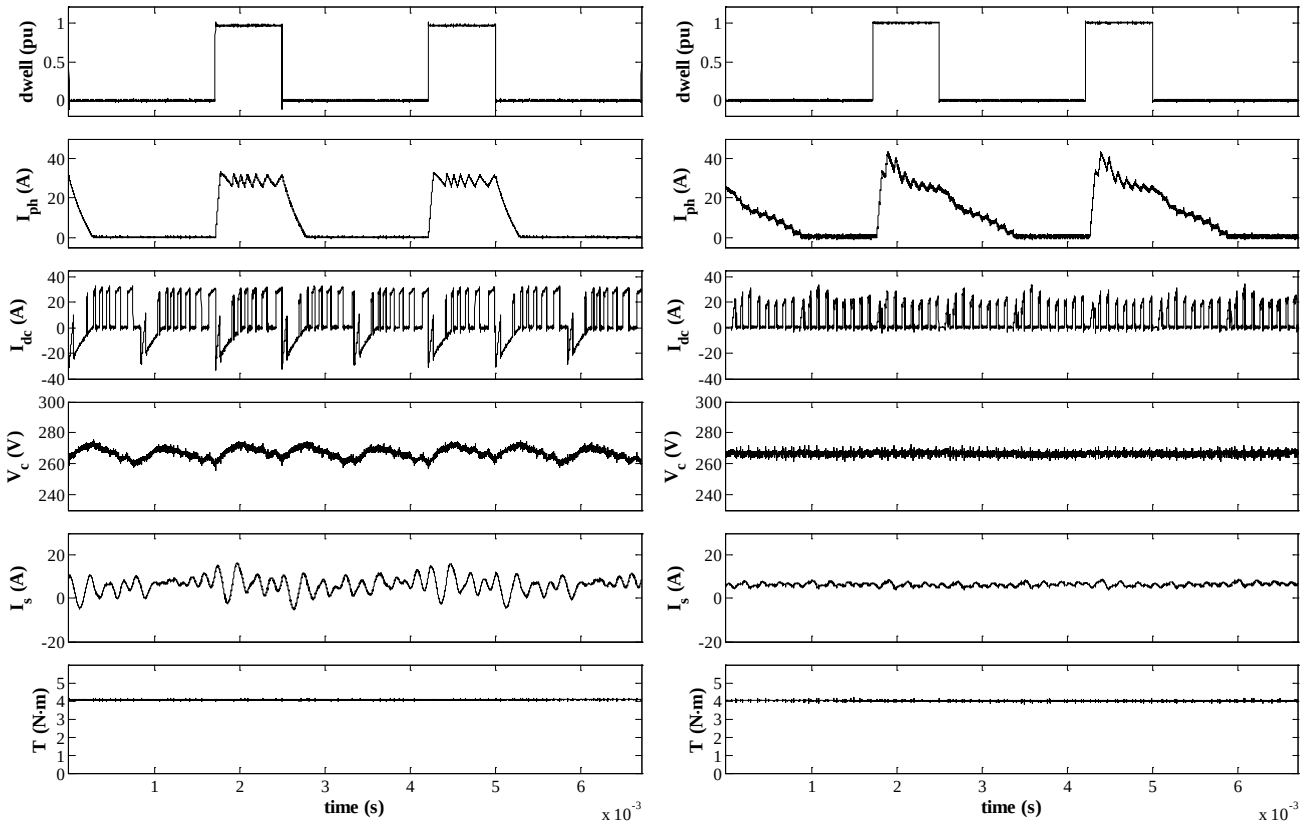
$$I_{dc} = \sum (-i_{ph} \cdot \overline{S_{1,n}} \cdot \overline{S_{2,n}}) + (i_{ph} \cdot S_{1,n} \cdot S_{2,n}) \qquad (3)$$

This signal is fed into a resettable analogue integrator for the DLCIC operation.

A 270V DC power supply is connected to the converter via 25-m cable with estimated parasitic inductance of 100 μH [25]. The proposed technique is implemented in dSPACE system at 10 kHz PWM frequency. For comparison, the hysteresis control is also implemented and tested.

During the tests, the SR drive operated in closed-loop speed control at a constant speed and the load torque was controlled by the dynamometer. Since the proposed method is most effective when operating in speeds at or below 3000 r/min, the experimental results are presented for the 4 N·m and 3000 r/min operating condition. The experimental waveforms for voltage, current and logical signals are measured by high bandwidth voltage and current probes and they are recorded in Yokokawa Digital Scope DL750 with a sampling rate of 10 MHz.

The dwell signal, the phase current (I_{ph}), the DC-link capacitor voltage (V_c), the supply current (I_s), and the machine torque (T) obtained from the conventional hysteresis current control are shown in Fig. 11 (a) and those from the proposed technique are shown in Fig. 11 (b). Both the experiments have the same turned-on and turned-off angles, being 3° and 18° respectively.



(a) (b)

Fig. 10. Experimental waveforms at 4 N·m, 3000 r/min. (a) HCC, (b) Proposed DLCIC

As can been seen, the peak-to-peak capacitor voltage which results from the hysteresis control is 20.67V and is much higher than that from the proposed method 11.33V. More importantly, the proposed switching technique prevents the negative DC current during the de-fluxing period of an outgoing phase and hence effectively removes the commutation induced low frequency harmonics

Not only the capacitor voltage ripple is reduced, the ripple in the supply current which results from the proposed switching technique is much lower compared to that from the hysteresis control. The peak-to-peak value of I_s from the hysteresis control is 22.08A while that from the proposed technique is 5.16A. It should also be noted that although the commutation period of the proposed technique is longer than that of the hysteresis control, the rms phase currents of both the techniques are very close, being 17.08A for the hysteresis and 17.97A for the proposed technique.

The measured torque waveforms for both the hysteresis and proposed control techniques appear to be smooth. This is due to the fact that the output of the torque transducer is processed by a built-in low pass filter with a cut-off frequency of 40 Hz. Thus the torque ripple of the SR machine is smoothed out by the filter.

6 Conclusion

A new switching technique aimed for minimising the DC-link capacitance in an SR machine drive has been described. By maintaining a constant average DC-link current over a PWM switching cycle, the commutation induced low frequency harmonics in the DC-link current can be eliminated. Thus, the proposed technique can significantly reduce the capacitor voltage ripple and the supply current ripple in the DC-link of an SR drive when operating at low speeds. It has been shown that by combining the proposed technique with the conventional hysteresis current control, the capacitor size and filter weight can be 18 times less than that of the conventional hysteresis control for the same power quality and stability requirements. The utility and effectiveness of the proposed switching technique have been validated by experimental results. The developed switching technique facilitates size and cost reduction of SR drives, and removes one of the barriers for the realisation of its full potential in safety critical applications.

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