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Multiplexed charge-locking device for large arrays of quantum devices

R. K. Puddy,[1,a)] L. W Smith,[1] H. Al-Taie,[1,2] C. H. Chong,[1] I. Farrer,[1] J. P. Griffiths,[1] D. A. Ritchie,[1] M. J. Kelly,[1,2] M. Pepper,[3] and C. G. Smith[1]
[1]*Cavendish Laboratory, University of Cambridge, Cambridge CB3 0HE, United Kingdom*
[2]*Centre for Advanced Photonics and Electronics, Electrical Engineering Division, Department of Engineering, 9 J. J. Thomson Avenue, University of Cambridge, Cambridge CB3 0FA, United Kingdom*
[3]*Department of Electronic and Electrical Engineering, University College London, WC1E 7JE, United Kingdom*

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We present a method of forming and controlling large arrays of gate-defined quantum devices. The method uses an on-chip, multiplexed charge-locking system and helps to overcome the restraints imposed by the number of wires available in cryostat measurement systems. The device architecture that we describe here utilises a multiplexer-type scheme to lock charge onto gate electrodes. The design allows access to and control of gates whose total number exceeds that of the available electrical contacts and enables the formation, modulation and measurement of large arrays of quantum devices. We fabricate such devices on n-type GaAs/AlGaAs substrates and investigate the stability of the charge locked on to the gates. Proof-of-concept is shown by measurement of the Coulomb blockade peaks of a single quantum dot formed by a floating gate in the device. The floating gate is seen to drift by approximately one Coulomb oscillation per hour. © *2015 AIP Publishing LLC*.
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Motivation for the study of large arrays of quantum devices, such as electrically defined quantum dots (QD),[1–3] arises both from the requirement to up-scale for quantum information processing[4–7] and from interest in the physics that complex devices may give rise to. One of the many challenges of fabricating such complex devices is the limited number of wires available on measurement setups. Controlling just three[8–10] or four[11–13] quantum dots may require 20 wires, the limit of many research systems. Recent work[14–16] has shown the use of the multiplexer (MUX) to greatly increase the numbers of isolated quantum devices available for study on a single chip. The architectures so far reported however do not allow the simultaneous use of all the MUX outputs, a requirement for the fabrication of large interacting arrays. Here, we present a method that overcomes these restraints by using an on-chip multiplexer to lock charge onto gate electrodes. We fabricated such a device, on a GaAS/AlGaAs substrate, which in principle enables control and measurement of 14 quantum dots using only 19 wires. Proof-of-concept is provided by measuring the Coulomb blockade peaks of a quantum dot defined using this architecture. This scheme represents a powerful tool for up-scaling and investigating new phenomenon.

Figures 1(a)–1(c) show cartoon schematics of a small section of the charge-locking MUX device in various stages of fabrication. The device consists of three separate two dimensional electron gases (2DEGs). These are shown in Figure 1(a) and denoted as (1) the MUX 2DEG, (2) the gate-source 2DEG, and (3) the device 2DEG. The 2DEGs are accessed via ohmic contacts (brown squares). The gate-source 2DEG is a comb-like structure with a main channel and multiple tributaries. A dielectric (green) is then added, Figure 1(b), to the MUX 2DEG to enable addressing (see Ref. 15 for an explanation of the MUX operation), and to the gate-source 2DEG to cover the main channel leaving the tributaries exposed. Finally surface gates are added, Figure 1(c), which we denote as (1) addressers, (2) locks, (3) device-gates, and (4) the central gate. The dielectric used for our device was a ≈600 nm layer of polyimide. The thickness of the dielectric is such that the gate voltage required to deplete the 2DEG underneath the polyimide is around 10 times greater than for gates passing directly over the substrate surface. Each lock is connected to a MUX output ohmic and passes over the gate-source dielectric and covers a single tributary. From each of the tributary ohmics a surface gate passes onto the measurement 2DEG to form the final device. The MUX and gate-source arrangement is repeated, mirrored about the central gate. The central gate crosses the measurement 2DEG allowing two measurement channels to be formed.

The steps required for initialisation and operation of the device are shown in Figures 2(a)–2(d). First, Figure 2(a), the multiplexer 2DEG and addressing gates are set to a voltage, referred to as the locking voltage V_L, which is well beyond the depletion voltage of the 2DEG V_{dpln} (active gates are coloured red). This initial operation depletes the 2DEG under the locking-gates and therefore isolates all the gate-source tributaries from the main channel. Next, Figure 2(b), the addressing gates are set to a second voltage, which we name the double lock voltage $V_{dbL} \approx 2 \times V_L$. This second operation isolates the locking-gates which are now charged and floating at V_L. Steps one and two constitute an initialisation process and the device is ready to be used. We next address one of the multiplexer outputs, e.g., the left branch in Figure 2(c), and set the multiplexer 2DEG to 0 V. This allows the addressed locking-gate to discharge, reconnecting the tributary under the addressed locking-gate to the main channel of the gate-source 2DEG (the white arrows represent available current paths). The device-gate can now be swept to the

a)rkp27@cam.ac.uk

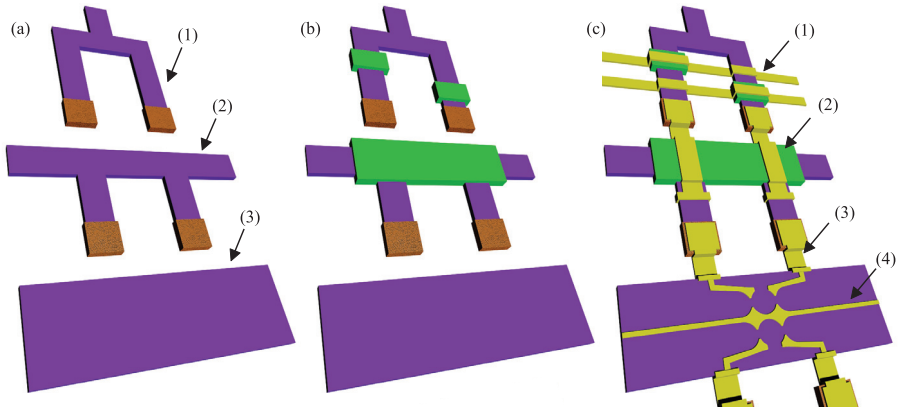

FIG. 1. Cartoon schematics of a section of the charge-locking device in various stages of fabrication. (a) The device consists of three separate 2DEGs referred to as: (1) the MUX 2DEG, (2) the gate-source 2DEG, and (3) the measurement 2DEG. The brown squares are ohmic contacts to the 2DEGs. (b) A dielectric (green) is added to the MUX 2DEG to enable addressing and to the gate-source 2DEG over the main channel leaving the tributaries exposed. (c) Surface gates are added and referred to as: (1) addressers, (2) locks, (3) device-gates, and (4) central gate. Each lock passes over the dielectric to cover a single tributary. Each gate-source tributary terminates in a device-gate which passes onto the measurement-2DEG to form the final device. The MUX and gate-source arrangement is then repeated, mirrored about the central gate on the measurement 2DEG.

desired voltage via the main channel of the gate source 2DEG. Next, Figure 2(d), charge is locked onto the device-gate by setting the multiplexer 2DEG and addressing-gates to V_L, isolating the tributary from the main channel. The lock is then isolated by setting the addressing gates to V_{dbL}. The operations in Figures 2(c) and 2(d) can then be repeated for the other device-gates. In this way, large numbers of gates can be set up to form complex devices.

We first investigate the stability of individual floating device gates. The plot in Figure 2(e) shows the conductance through the measurement 2DEG as a function of the voltage applied to the gate-source 2DEG with a single gate addressed as in panel (c) above. During the measurement the central gate is held at a constant voltage using a directly connected voltage supply. The measurements were made at the base temperature of a dilution refrigerator (≈50 mK). Figure 2(f)

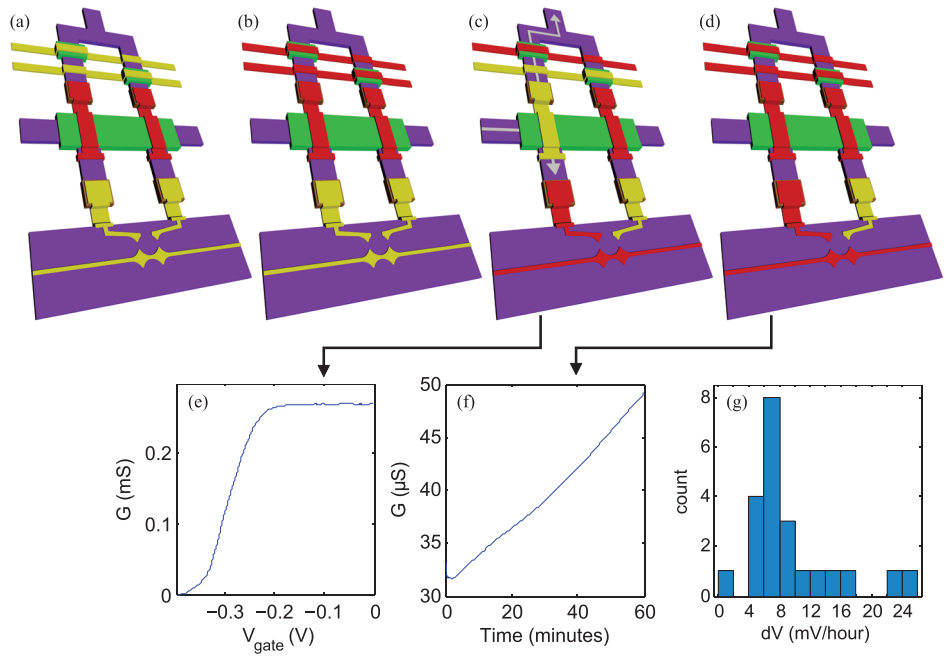

FIG. 2. Operational steps of the charge-locking device. (a) The MUX 2DEG and addressing gates are set to a voltage, named the locking voltage $V_L \gg V_{dpln}$ (V_{dpln} = depletion voltage). This isolates the tributaries from the main channel of the gate-source 2DEG. (b) The addressing gates are then raised to $2 \times V_L = V_{dbL}$. This isolates the locking gates and leaves them floating at V_L. (c) One of the locks (e.g., the left lock in the figure) is addressed and the MUX 2DEG set to zero volts. The addressed lock is then able to discharge via the MUX input and the tributary is reconnected to the gate-source 2DEG input. A voltage may now be applied to the device gate, V_{dg}, via the input and main channel of the gate-source 2DEG. (d) The MUX 2DEG and addressing gates are then set to V_L to lock the charge onto the device gate and the addressing gates are then set to V_{dbL} to isolate the lock. Steps (c) and (d) are then repeated to set the remaining gates. (e) Conductance G of the measurement 2DEG, as a function of device gate voltage V_{dg} of a single addressed gate (stage (c) above). (f) Conductance as a function of time of a single floating device-gate (stage (d) above). The device-gate has been isolated and no external voltages are applied to the device-gate 2DEG. The time varying conductance dG/dt is converted to an effective change in device-gate voltage dV_g/dt, by comparing (e) and (f). (g) A histogram of the calculated dV_{dg}/dt for several device-gates.

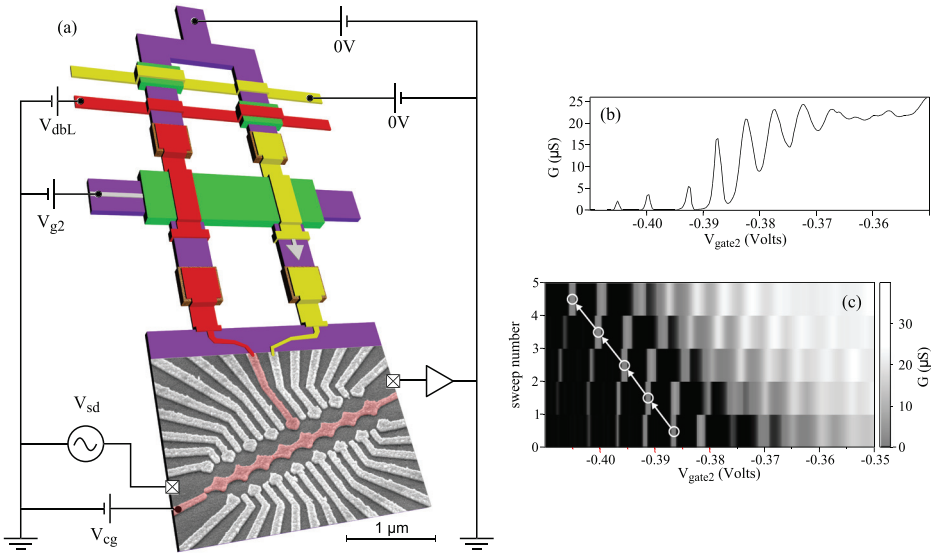

FIG. 3. (a) Schematic and circuit diagram of the charge-locking device with an SEM image of a set of device gates identical to that of the measured device. The central gate is held at $V_{cg} = -0.5$ V by an external voltage source, a device gate (g1) has been addressed, set to −0.45 V, and subsequently isolated. An adjacent gate is then addressed and the voltage V_{g2} swept via the gate-source 2DEG. Panel (b) shows G as a function of V_{g2}, measured at ≈50 mK. Coulomb resonances appear as a QD is formed. This measurement is repeated five times at 1 h intervals whilst the floating gate g1 remains isolated. The five sweeps are shown in panel (c) as greyscale plots. The white circles highlight a single Coulomb peak, which is observed to drift by ≈8 mV/h.

shows the change in conductance as a function of time dG/dt, after the device had been isolated as in panel (d). By comparing the plots in panels (e) and (f), the time varying conductance can be converted in to an effective change in device-gate voltage dV_{dg}/dt. Panel (g) shows a histogram of this effective drift for several gates. The modal average is around 7 mV/h. Possible mechanisms for the observed drift dG/dt include charge leaking from the device gates into surface states on the substrate, into the donor layer or into the main channel of the device gate 2DEG via the depleted region under the locking gates. In addition, charge rearrangement within the donar layer could also give rise to the observed drift. Possible improvements to the drift may be achieved by using different doping configurations, the addition of an insulating layer under the gates and by increasing the gate capacitance to ground.

We next perform a proof of principle measurement by forming a QD between the central gate, an isolated floating device gate and an actively addressed device gate. Figure 3(a) shows a schematic of the device and the circuit diagram used to form and measure the QD. The SEM image shows a set of device gates identical to that of the measured device. During the measurement the central gate is held at $V_{cg} = -0.5$ V using an external voltage source. A device gate (g1) has been addressed, set to −0.45 V and subsequently isolated. An adjacent gate is then addressed and the voltage V_{g2} swept via the gate-source 2DEG. Panel (b) shows G as a function of V_{g2}, measured at ≈50 mK. Coulomb resonances appear as a QD is formed. The voltage sweep with g2 addressed is repeated five times at 1 h intervals whilst the floating gate g1 remains isolated. The five sweeps are shown in panel (c) as greyscale plots. The white circles highlight a single Coulomb peak, which is observed to drift by ≈ 8 mV/h.

The proof of principle measurements presented here show that our device architecture offers, by increasing the number of available electrical contacts, a route toward the investigation of quantum devices of increasing complexity. We found the gate voltage drifts by around one Coulomb peak per hour for the device tested. Improvements to the gate stability may be required for some operations, and so, further investigation into the mechanisms and possible improvements to the gate stability are required.

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[1]U. Meirav, M. A. Kastner, and S. J. Wind, Phys. Rev. Lett. **65**, 771 (1990).
[2]L. P. Kouwenhoven, N. C. van der Vaart, A. T. Johnson, W. Kool, C. J. P. M. Harmans, J. G. Williamson, A. A. M. Staring, and C. T. Foxon, Z. Phys. B **85**, 367 (1991).
[3]C. G. Smith. Rep. Prog. Phys. **59**, 235 (1996).
[4]D. Loss and D. P. DiVincenzo, Phys. Rev. A **57**, 120–126 (1998).
[5]J. M. Taylor, H.-A. Engel, W. Dür, A. Yacoby, C. M. Marcus, P. Zoller, and M. D. Lukin, "Fault-tolerant architecture for quantum computation using electrically controlled semiconductor spins," Nat. Phys. **1**, 177–183 (2005).
[6]J. R. Petta, A. C. Johnson, J. M. Taylor, E. A. Laird, A. Yacoby, M. D. Lukin, C. M. Marcus, M. P. Hanson, and A. C. Gossard, Science **309**, 2180–2184 (2005).
[7]R. Hanson, L. P. Kouwenhoven, J. R. Petta, S. Tarucha, and L. M. K. Vandersypen, Rev. Mod. Phys. **79**, 1217 (2007).
[8]A. Vidan, R. M. Westervelt, M. Stopa, M. Hanson, and A. C. Gossard, Appl. Phys. Lett. **85**, 3602 (2004).
[9]J. Medford, J. Beil, J. M. Taylor, S. D. Bartlett, A. C. Doherty, E. I. Rashba, D. P. DiVincenzo, H. Lu, A. C. Gossard, and C. M. Marcus, "Self-consistent measurement and state tomography of an exchange-only spin qubit," Nat. Nanotechnol. **8**, 654–659 (2013).
[10]F. R. Braackman, P. Barthelemy, C. Reichl, W. Wegsheider, and L. M. K. Vandersypen, Nat. Nanotechnol. **8**, 432–437 (2013).
[11]M. D. Shulman, O. E. Dial, S. P. Harvey, H. Bluhm, V. Umansky, and A. Yacoby, "Demonstration of entanglement of electrostatically coupled singlet-triplet qubits," Science **336**, 202–205 (2012).
[12]R. Thalineau, S. Hermelin, A. D. Wieck, C. Bäuerle, L. Saminadayar, and T. Meunier, Appl. Phys. Lett. **101**, 103102 (2012).
[13]L. Gaudreau, A. Kam, G. Granger, S. A. Studenikin, P. Zawadzki, and A. S. Sachrajda, Appl. Phys. Lett. **95**, 193101 (2009).
[14]D. R. Ward, D. E. Savage, M. G. Lagally, S. N. Coppersmith, and M. A. Eriksson, Appl. Phys. Lett. **102**, 213107 (2013).
[15]H. Al-Taie, L. W. Smith, B. Xu, P. See, J. P. Griffiths, H. E. Beere, G. A. C. Jones, D. A. Ritchie, M. J. Kelly, and C. G. Smith, Appl. Phys. Lett. **102**, 243102 (2013).
[16]J. M. Hornibrook, J. I. Colless, A. C. Mahoney, X. G. Croot, S. Blanvillain, H. Lu, A. C. Gossard, and D. J. Reilly, Appl. Phys. Lett. **104**, 103108 (2014).