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# Development of Phase Shift Lithography for the Production of Metal-Oxide-Metal Diodes

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Metal-oxide-metal (MOM) diodes have been produced by combining two novel techniques: an RIE etch and subsequent plasma oxidation, and a phase shift lithography process. This has resulted in a significant reduction in device feature sizes, down to sub-micron dimensions and with improved zero voltage curvature coefficient of up to 2.8 $V^{-1}$ for the associated diodes. Given the use of MOM diodes in high speed rectification applications, the combination of the reduction in diode area as well as the controlled oxide growth aims to assist in the improved cut-off frequency of the devices, thus ensuring the potential for high speed applications.

**1. Introduction:** Metal-oxide-metal (MOM) diodes have the potential to rectify terahertz radiation collected by micron-scaled antennas from waste heat sources and convert this into a useful DC current [1], [2], [3]. The antennas themselves are comparatively straightforward to make, with micron-scale dimensions. However, the diodes must be much smaller than this, which provides production and characterisation issues.

The MOM diode structure consists of two dissimilar metals separated by a native oxide layer, which is sufficiently thin to allow electron tunnelling to occur, i.e. 5 nm or thinner [4]. A functional diode is best achieved by using one metal which will oxidise readily and another which is inert. By choosing two metals with a maximum difference in work function, we can increase the asymmetry of the resulting diode. Many metal combinations have been tried, e.g. Ni-Au [5] and Al-Pt [6]; here we have chosen titanium, which oxidises readily, and maximised the work function difference by using inert platinum as the other metal.

Initial diodes were produced using furnace oxidation, which gave excellent results with respect to a universal figure of merit, the curvature coefficient [7], [8]. However, more control was required over the thickness and uniformity of the oxide layer, and an alternative method of oxidation was investigated; this involved a reactive ion etch (RIE) of the native titanium oxide and plasma oxidation regrowth [9]. In [9], diodes with a uniform oxide of known stoichiometry was produced and the thickness of this oxide was controlled as a function of the oxygen plasma power used to create it. Having such a level of control on the oxide is vital as even small oxide changes have a significant impact of diode performance.

As well as oxide thickness and uniformity considerations, the diodes must be sufficiently small for high speed rectification to occur. Other groups have produced diodes using electron beam lithography, e.g. [10], which allows very small features to be produced. However, this is a serial writing process, resulting in very slow processing times. If these diodes and their associated antenna are ever likely to be used in energy recovery, there needs to be a way of mass producing large volumes of devices at high speed. A novel, batch scalable process is required which can also produce sub-micron features. Nanoimprint lithography (NIL) is an interesting field for such demands [11], but NIL is a direct copying process and a master stamp is still required. Therefore phase shift lithography (PSL) has been used as an important step towards demonstrating mass manufacturability, with novel PDMS stamps made from master $SiO_2$ patterns on silicon substrates.

1.1. Phase Shift Lithography: Work in [12] describes the production of feature sizes in the region of 90 nm using an elastomeric phase mask and incoherent, polychromatic ultraviolet light. The structures add a phase element to masks which would usually just provide binary amplitude information. By using thick and thin regions in a mask, the phase of two adjacent paths of light can be shifted by an odd multiple of $\pi$, resulting in an intensity of zero at every edge by destructive interference, as seen in Figure 1 [13].

The profile of a phase shift mask can be seen, with the theoretical intensity profile below it (a) and the resultant photoresist patterns which result from such a phase mask; positive photoresist (b) and negative photoresist (c), assuming an intensity which corresponds to the orange line in (a). In order to ensure a repeatable process, regardless of metal choice, lift-off is the preferred method for this technique. However, the contrast of the negative photoresists is insufficient to provide a suitable lift-off profile. By underexposing the photoresist, the intensity of light on the photoresist can be altered, which corresponds to the intersection with the red line in (a). The photoresist profile in (d) is the ideal pattern produced in positive photoresist as a result of underexposure.

Process trials indicated that an additional effect was taking place, resulting in a photoresist profile that did not match that in (a), but instead appeared to be a superposition of the step height of the phase mask and the original intensity profile, which can be seen in Figure 2 (b). This could be due to the different transmission coefficients in different regions at the stamp-substrate interface, due to the presence of air gaps in one of the polarities. This equates to a transmission coefficient of 0.999 in the direct contact regions, compared to a transmission coefficient of 0.898 in the regions separated by an air gap. As a result, the actual photoresist profile, which is an inversion of the intensity profile, can be seen in Figure 2 (c). This profile has been confirmed experimentally, with Figure 3 showing a typical AFM image.

In order to produce a PSL stamp, an N-type <100> silicon of 10-30 $\Omega$cm resistivity was chosen as the substrate material (2" diameter wafers). The depth of the features (also known as surface relief) was calculated for the average wavelength of the UV light used for exposure (330 - 460 nm). The substrate was oxidised to provide an insulating 456 nm film, calculated to provide the correct step height for the average wavelength of light used to successfully invert the phase at the interface. Using standard lithographic techniques, a pattern was then transferred onto the substrate in Microposit SPR-350 photoresist. An Oxford Instruments combined reactive ion etch/plasma etch (RIE/PE) system was then used to etch this pattern into the silicon dioxide layer (25 sccm $CHF_3$, 25 sccm Ar, 40 mT, 200 W, 15 minutes), thus providing a three dimensional master stamp. PDMS (Sylgard 184, 6:1 ratio) was then cast onto the patterned $SiO_2$ substrate and cured to form an UV transparent elastomeric stamp.
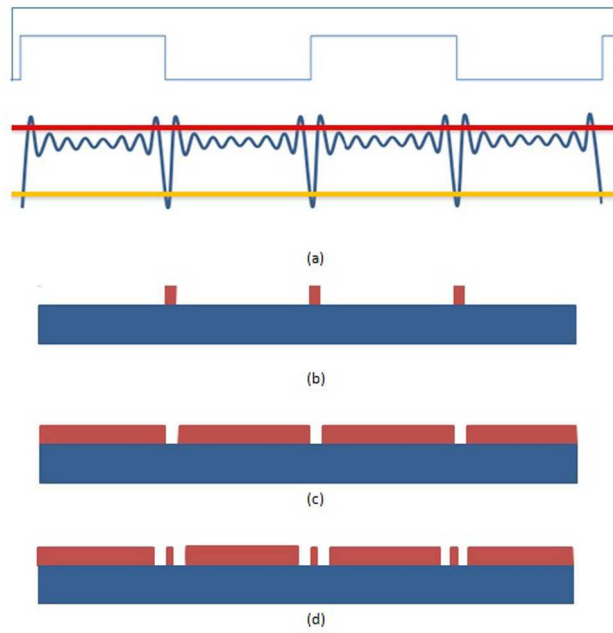
**Figure 1** *The phase shift process - (a) a profile of a phase shift mask with the ideal intensity profile, (b) the ideal effect of this intensity on positive photoresist (orange line), (c) the ideal effect of this intensity on negative photoresist (orange line), and (d) on an intensity inversion in positive photoresist (red line).*
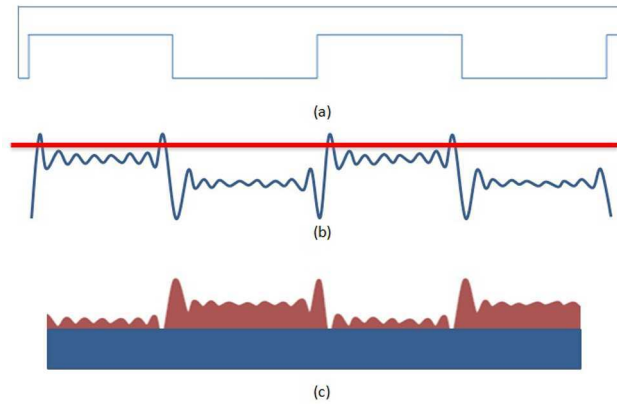


**Figure 2** *(a) The profile of a phase shift mask, (b) the actual intensity profile and (c) the intensity inversion pattern produced in positive photoresist.*

**2. Fabrication:** Borosilicate glass wafers were used as a substrate for the fabrication of diodes. A bi-layer lift-off process, using PMGI SF9 and SPR-350 photoresists and MF-319 developer, were used to produce a base layer pattern on the wafer, on top of which 25 nm of titanium and 50 nm of gold were deposited in the same e-beam evaporation process. The photoresist was removed using Microposit 1165. The resulting pattern included all contact pads and a common connection for final testing, as seen in Figure 4(a) and (b).

The lift-off process was repeated twice; first with a design which allows all but the rectangular contact pad region to be coated with a thin layer of chromium (c), and secondly with a mask design the leaves only the common connection exposed (the horizontal line seen running through (b-e)). An etchant (4:1:8 $KI:I_2:H_2O$) was used to remove the uncovered gold, leaving a region of titanium exposed only on the common connection, which can be seen as a horizontal grey line in (d), with the vertical contact pads remaining covered in gold to ensure a good electrical connection with the phase shifted lines. The exposed titanium was then oxidised using a controlled reactive ion etch and plasma regrowth step, discussed in [9].

The PSL process was then used to provide vertical troughs in photoresist. SPR-350 photoresist, diluted to a 50% concentration with Microposit EC solvent, was then spun on the substrate (approx. 400 nm thick) and the PDMS mask brought into conformal contact with the surface. Exposure to a low UV dose, followed by post-exposure bake and development resulted in narrow trough regions in the photoresist at every point where a height transition had occurred in the PDMS stamp. A dry etch (100 sccm $O_2$, 50 mT, 70 W for 10 s - RIE mode) was used to ensure any unwanted photoresist was fully removed from these regions. 40 nm of platinum was then evaporated, resulting in a small Ti/TiOx/Pt region being produced (e). Finally, the chromium was removed, which also removed unwanted platinum, completing the diode fabrication process.

The phase shifted lines are positioned on the substrate only visually, which means the detailed alignment cannot occur. However, the design of the phase shifted line mask is such that the distance between each phase shift line is equal to the width of each contact pad, therefore there are multiple vertical phase shifted lines within distance between consecutive vertical contact pads, and each contact pad must make contact
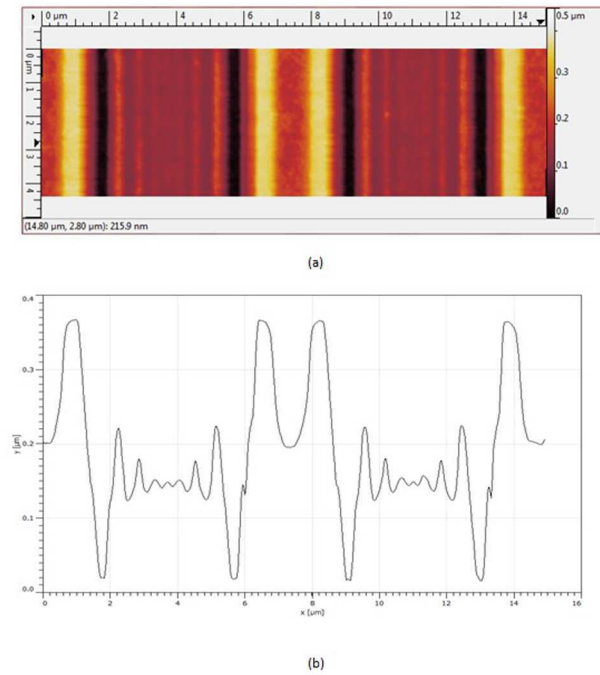
**Figure 3** *(a) AFM image of phase shift lines and (b) their profiles in positive photoresist.*
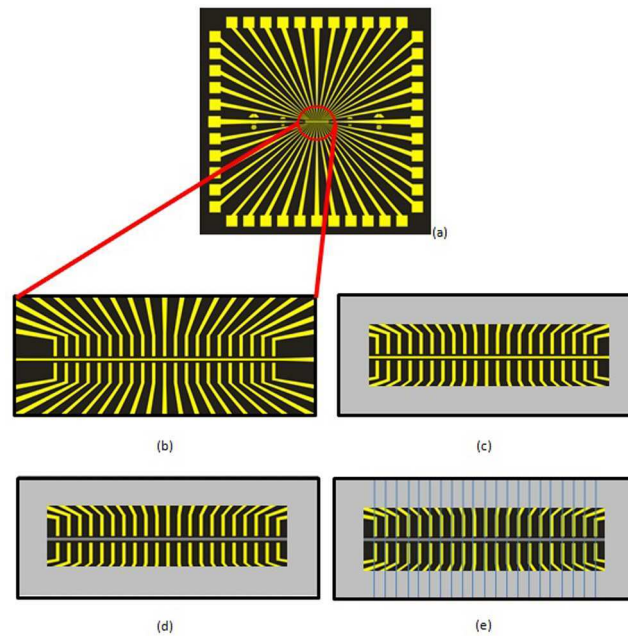


**Figure 4** *(a) Diode base layer in titanium and gold. (b) Close up of connectors for each diode (vertical lines) and common connection (horizontal line). (c) Entire wafer covered in chromium (grey) leaving only the diode contact pad region exposed (d). The common connector has the gold etched away leaving titanium exposed (dark grey), the vertical gold contact pads are protected here by photoresist, and are therefore not etched away. (e) Phase shifted lines over contacts and chromium (blue lines). The chromium is then removed leaving vertical platinum PS lines in contact region only, preventing short circuits between the contact pads as they diverge.*

with a phase shifted line. This ensures a connection between the phase shifted lines and the contact pads, despite having only visual alignment capabilities.

### 3. Results and discussion:

3.1. Phase Shift Diodes - Physical Analysis: Using this technique, line widths in the range 200-400 nm can be achieved routinely. Figure 5 shows images of PSL lines incorporated into diodes, with a 10 $\mu$m common connection (top left to bottom right) overlapped by PSL platinum lines (top right to bottom left), which have been shortened via the etching of a sacrificial chromium layer to prevent shorting. These images

combined with electrical results show the process to be robust, with phase shifting still occurring at the interface of the existing steps height for the contact pads.
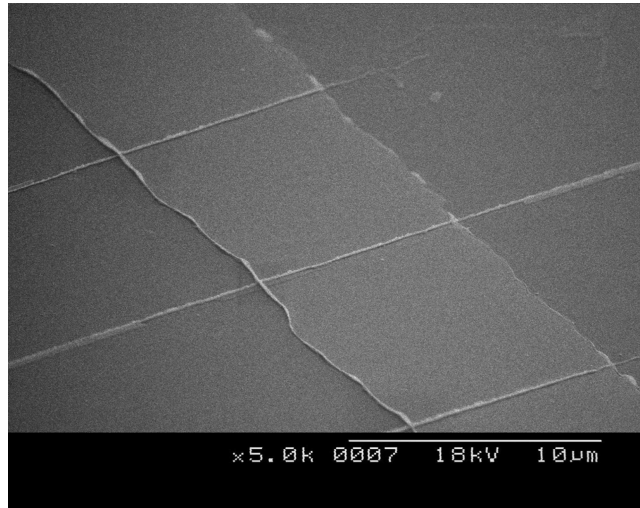


**Figure 5** *Crossover of phase shift Ti-TiOx-Pt diode, with the wide common Ti/TiOx connection (top left to bottom right, seen as horizontal dark grey line in Figure 4 (d) and (e)) and the PSL Pt lines (top right to bottom left, thin vertical blue lines in Figure 4(e)). The diode region is the crossover between the two.*

Due to the lift-off process, the edge roughness of the phase shifted lines would result in reduced yield if used as a base layer in diode production, which is why the PSL lines were used as the top layer, as then the edge profile of the platinum layer does not affect the functionality of the diodes. The yield of the diodes is limited by the ability to align the sub-micron lines with the contact pad and by the number of defect in those lines, neither of which have posed significant issues.

For future devices, a nano-imprint lithography (NIL) tool could be used to align these imprint stamps more accurately, allowing multiple layers of PSL lines to be used in a single device. Control contact between the stamp and substrate could also be accurately controlled, thus improving the quality of the phase shift process and therefore the yield of the devices. Furthermore, this process could be used to produce sub-micron master stamps for standard NIL processing, which would provide a low cost, high speed method of fabricating sub-micron devices.

3.2.   Phase Shift Lithography Furnace Diodes: These devices were also successful electrically as diodes, as can be seen from a typical J-V graph in Figure 6(a). These diodes have a typical zero bias curvature coefficient ($CC_{ZB}$) of 0.7 $V^{-1}$, a peak value of 1.34 $V^{-1}$ and a forward to reverse current ratio of 1.4:1. These values compare favourably with results published by others [6], [10].
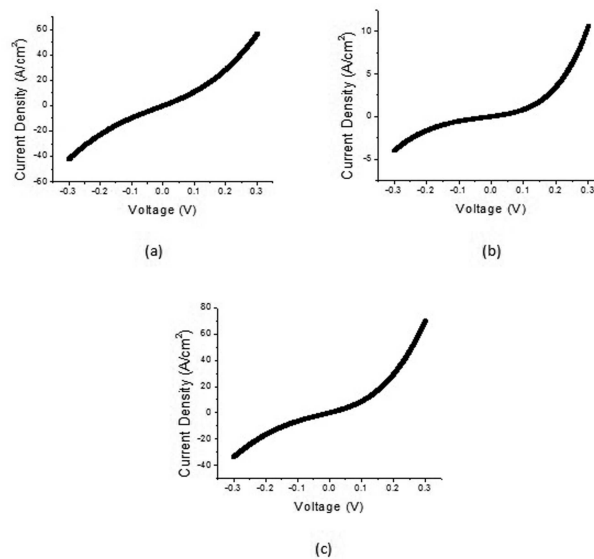


**Figure 6** *The current density-voltage (J-V) characteristics of MOM diodes prepared with the following techniques and dimensions; (a) furnace oxidation, PSL, 0.4 μm x 9 μm, (b) plasma oxidation, PSL, 0.4 μm x 9 μm, and (c) plasma oxidation, standard lithography, 9 μm x 9 μm.*

3.3.   Phase Shift Lithography Plasma Oxidation Diodes: In order to improve yield as well as electrical characteristics, plasma oxidation of the titanium was applied to the phase shift diodes. Figure 6(b) shows a typical J-V characteristic of a diode fabricated this way, with asymmetry and non-linearity comparable to previous, larger diodes [8]. It has been found that a peak current density of 100 $Acm^{-2}$ or smaller is consistent with a diode with good rectifying capabilities, as confirmed by the curvature coefficient and forward to reverse current ratio. These diodes

have a typical zero bias curvature coefficient ($CC_{ZB}$) of 2.8 $V^{-1}$, a peak value of 4.1 $V^{-1}$ and a forward to reverse current ratio of 2.6:1; all these values are improvements on the furnace oxidised diodes. The shrinkage of the device dimensions has not led to any noticeable degradation in diode performance. Figure 6(c) shows a typical J-V of a plasma oxidised diode with larger dimensions prepared by standard lithography, and the corresponding diode performance figures are a typical zero bias curvature coefficient ($CC_{ZB}$) of 3.3 $V^{-1}$, a peak value of 4.6 $V^{-1}$ and a forward to reverse current ratio of 2.1:1. A summary of electrical results, together with the oxide thickness (measured by both TEM and ToFSIMS) and fabrication process, is given in Table 1.

**Table 1** *Summary of Diode Results*

| Oxide Preparation | Size ($\mu$m) | $CC_{ZB}$ ($V^{-1}$) | Oxide Thickness (nm) |
|---|---|---|---|
| 4 hour furnace | 0.4 x 9 | 1.3 | 6.7 |
| 100% $O_2$ Plasma 120 W | 9 x 9 | 3.2 | 5.0 |
| 100% $O_2$ Plasma 150 W | 9 x 9 | 2.9 | 5.0 |
| 50% $O_2$ Plasma 300 W | 9 x 9 | 4.6 | 4.0 |
| 50% $O_2$ Plasma 300 W | 0.4 x 9 | 4.1 | 4.0 |

A comparison of the current densities between the different diodes in Figure 6 is worthy of note. Although the oxide thickness range is where competing conduction mechanisms could occur, the change in current density between diodes is unlikely to be due to this. The values in Figure 6 (a) (furnace oxide - 6.7 nm) and Figure 6 (c) (plasma oxide - 4.0 nm) are similar, yet the current density in Figure 6 (b) (also plasma oxide - 4.0 nm) is a factor 8 down in value. The reasons for this are still being investigated.

**4. Conclusions:** Metal oxide metal diodes with sub-micron features and a controllable uniform oxide have been produced using novel plasma oxidation and phase shift lithography processes. The results have a high yield of high performance diodes, and this represents a significant step towards a mass manufacturable process for MOM diodes. The factor of 23 reduction in size from initial diode results will ensure an improved cut off frequency, thus ensuring the potential for high speed operation. Furthermore these diodes show competitive electrical results, confirming their asymmetry and non-linearity.

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