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Large-Signal Charge Control Modeling of Photoreceivers for Applications up to 40 Gb/s

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***Abstract*—A charge control model was used to simulate the sensitivity and responsivity in a range of photodetector configurations including heterojunction bipolar phototransistors (HPTs), PIN-HBT, and APDs. Our simulations enabled for the first time a direct comparison of the performance between these photodetectors to be made. Simulations have been performed at bit rates from 2 to 40 Gb/s using various combinations of device design parameters (layer thickness, source resistance, and dc base voltage). For a BER $= 10^{-9}$ at 40 Gb/s the best sensitivity of approximately −20 dBm was achieved using an optimized APD-HBT configuration, followed by sensitivities of approximately −14 dBm using optimized PIN-HBTs and HPTs. These results were found to agree well with published experimental data.**

***Index Terms*—APDs, heterojunction bipolar phototransistors (HBTs), photoreceivers.**

I. Introduction

BIT-RATES are set to rise to 40 Gb/s in next-generation optical fiber systems and there is a requirement to maximize the sensitivity such that repeater stations can be widely spaced. Devices that may be used as photoreceivers include the APD, PIN diode, metal–semiconductor–metal (MSM) diode, the heterojunction bipolar phototransistor (HPT), erbium-doped fiber amplifier-PIN (EDFA-PIN), and optically controlled MESFET [1]. Of these devices, the HPT, the PIN-HBT, and the APD-HBT are promising candidates because of their built-in gain and relative simplicity. These devices are shown schematically in Fig. 1 and are the subject of this study.

The HPT has the same structure as the HBT, where the BC region is used to absorb the light and the intrinsic gain of the transistor amplifies the signal, eliminating the need for interconnects. The photocurrent is injected directly into the base in an HPT rather than through the base resistance in the case of a PIN-HBT but the HPT has to be relatively large to accommodate the fiber diameter. PIN diodes operate at high speed and are readily compatible with HBT technology. Two integration schemes exist for the PIN-HBT combination. The first is the shared layer scheme where the base–collector (BC) region of the HBT also acts as the i-region for absorption in the PIN [2]–[6]. This design is simpler to implement, requiring a less complex grown structure and a simpler fabrication process [2], and is generally preferred for this reason. However, although the area of each element can be optimized for speed and fiber coupling efficiency, a compromise between the transit delays and absorption efficiency is required. The second scheme uses separate layer structures for the PIN and the HBTs, allowing the layer structures of both to be independently optimized [7], [8]. Parasitics associated with interconnects [9] are a drawback for both PIN-HBT structures. APDs provide internal gain through the impact ionization process, which is intrinsically noisy in most III–V semiconductors, but work on APDs with thin avalanche regions has allowed the excess noise factor associated with the ionization to be reduced [10]. This has enabled APD-based receivers to achieve high sensitivities [11]–[13]. However, the gain–bandwidth product of current APDs operating at optical communication wavelengths are around 170 GHz at best. Therefore, at 40 Gb/s, only a small improvement in sensitivity is expected for stand-alone APDs.

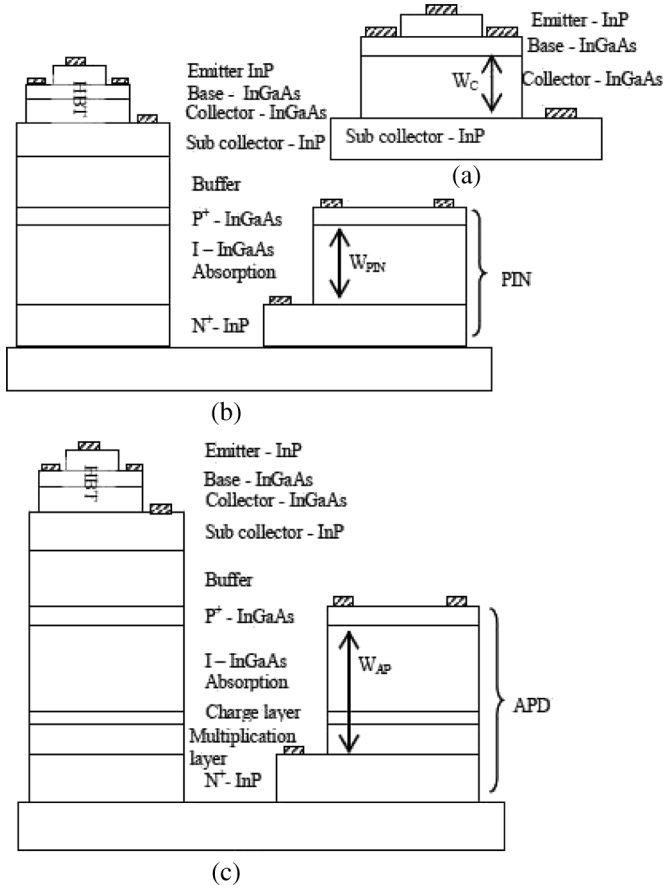

Fig. 1. Schematic diagrams of the (a) HPT, (b) separate PIN-HBT, and (c) APD-HBT material structures. The shared layer PIN-HBT is fabricated from the same structure as the HPT, but with two mesas, one of which has the emitter layer removed to form the PIN diode.

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Although the devices studied here are promising detectors for future high-speed communication systems, no detailed theoretical comparison has been carried out that would enable the choice of the best scheme for set system design parameters to be carried out. Various theoretical models have been presented for both the HPT [14], [15] and the PIN-HBT [16]. However, these models are lacking in that they either neglect often significant transit times or are circuit-based and do not offer the same physical insight as a purely physics-based analytical model. The transistors in this paper are modeled using charge control, together with the effects of the carriers drifting through the depletion regions (treated intrinsically), rather than approximating the transit with a diffusion capacitance as in a circuit model. This modeling is described in more detail in [17] for the HPT where the time-dependent output currents are produced, enabling realistic eye diagrams to be generated, including the effects of noise. In this paper, the modeling methodology is extended to include a PIN-HBT (two configurations) and an APD-HBT combination. This allows the effects of increasing complexity of the receiver from the HPT to a shared layer scheme PIN-HBT, a PIN-HBT with separate PIN and collector layer, and a proposed monolithic APD-HBT structure to be compared. The APD-HBT combination is considered since a hybrid APD-HBT has been shown experimentally to achieve high sensitivity [18]. The APD could be integrated on the same wafer as the HBT if the APD structure is grown first, followed by a buffer layer, and then the HBT layer, as illustrated in Fig. 1. This structure should minimize parasitic effects. The model allows the photodetectors to be directly characterized in terms of sensitivity, responsivity, bit rate, and design parameters. We compare three simple schemes (HPT, PIN-HBT, and APD-HBT), each involving only one amplifying transistor but all could be included with more complicated transimpedance amplifiers to improve the performance of the detector [2]. The sensitivities of the devices are calculated at different frequencies and a direct comparison of optimized designs for different applications is achieved.

II. Charge Control Modeling of HPT and PIN-HBT

The equivalent circuit diagrams of the HPT and the diode-HBT are shown in Fig. 2(a), where the dashed lines represent the connections inherent in the HPT and the dashed–dot lines are interconnects between the diode and the HBT. $V_{\rm APD}$ is an optional extra voltage source for controlling the avalanche gain in the APD. The avalanche duration in the APD can become significant at higher avalanche gains, and therefore, a mean current impulse response is included in the modeling. The BC region of the HPT is essentially a reverse-biased PIN diode, thus, the form of the photocurrent $i_{\rm ph0}(t)$ is the same in the HPT and PIN-HBT and is given in [17]. $i_{\rm ph0}(t)$ includes

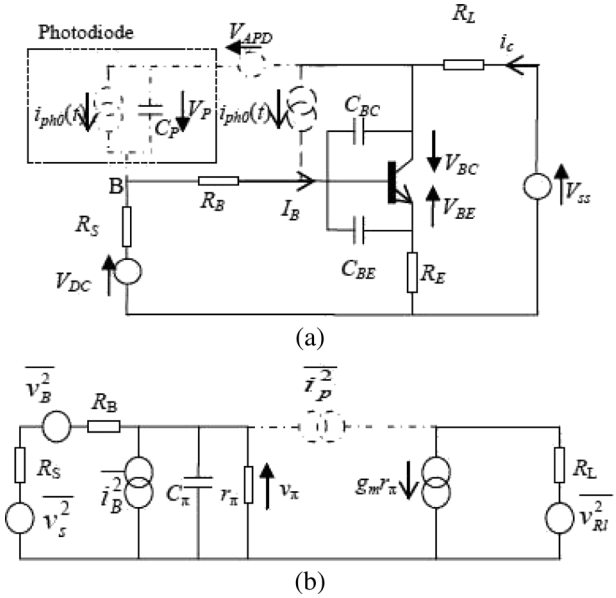

Fig. 2. Circuit diagrams of the HPT and the PIN-HBT. (a) Large-signal charge control model and (b) small-signal noise model. Circuitry only applying to the HPT is shown in dashed lines and that only to the PIN-HBT is shown in dashed–dot lines. Solid lines are common to both devices.

the drift and diffusion currents in the depletion region but excludes the charging of any geometric capacitance, as described later in Section III. In the APD-HBT, $i_{\rm ph0}(t)$ is calculated by convolving the impulse response [19] with the input bit train.

The base current must supply any transient charges in the transistor, i.e., the charge on the base–emitter (BE) and BC junction capacitances and the positive charge required to balance out the excess electron charge in the base and collector regions. The base bias considered here is a voltage source $V_{\rm dc}$ and resistor R_S as shown in Fig. 2(a). Variation of these parameters allows for a tradeoff between effective gain and speed, resulting in improved sensitivity performance at high bit rates over a current source biased device [17]. Following the procedure outlined in [17], expressions for the collector current can be extended to include the photodiode as in Fig. 2(a), as shown at the bottom of the page, whereI_S is the saturation current of the BE diode, $C_{\rm BC}$ and $C_{\rm BE}$ are the base–collector and base–emitter junction capacitance, respectively, $V_{\rm dc}$ and $V_{\rm BE}$ are the base bias voltage and base–emitter junction voltage, respectively, and R_S, R_B, R_E, and R_L are the source, base, emitter, and load resistances, respectively. $i'_{\rm ph0}$ is the first differential of the photocurrent with respect to time, $R_{\rm SUM}=R_B+R_S+R_E$, $R_{\rm Eff}=R_L+k_1R_E$, and $k_1=(R_B+R_S)/R_{\rm SUM}$. β is the dc gain given by τ_e/τ_B, where τ_e is the minority electron lifetime in the base and τ_B is the base transit time. k is the Boltzmann constant, T is the absolute temperature, and e is the electronic charge. This is a

$$\left.\frac{di_c}{dt}\right|_{\rm HPT}=\frac{\beta\frac{V_{\rm dc}-V_{\rm BE}+(R_B+R_S)i_{\rm ph0}(t)+C_{\rm BC}R_E(R_B+R_S)i'_{\rm ph0}(t)}{R_{\rm SUM}}-\left(\frac{\beta R_E}{R_{\rm SUM}}+1\right)i_c}{\tau_e+\frac{\beta\tau_{\rm ce}}{2}+\beta R_{\rm Eff}C_{\rm BC}+\beta\frac{kT}{e(i_c+I_S)}(C_{\rm BE}+k_1C_{\rm BC})} \tag{1}$$

key expression similar to (10) in [17] with the addition of R_S in the biasing circuit and including a time-varying photocurrent for completeness.

The increased parasitics associated with the integration of PIN-HBTs and APD-HBTs have not been included since they are specific to individual designs, and therefore, cannot be accurately calculated. From a performance comparison point of view, the intrinsic (neglecting interconnect effects) performance of the three photodetection schemes is of interest.

In the circuits shown in Fig. 2(a), it is assumed that the collector current flows though a load resistor without any further amplification, but the form of the current derived here may be applied to further amplification stages, which can be used to improve the performance of the receiver unit as described in [2], [8], [16], and [21].

III. Transient Photocurrent

In the HPT and PIN diode, the light is absorbed in a decaying exponential throughout the collector (i-region). The electrons and holes are separated by the electric field in the absorption region, with the electrons drifting to the n-side and holes to the p-side. This changing distribution of electrons and holes changes the electric field in the collector, causing a displacement current that can be accounted for by using the Ramo–Shockley theorem. Considering illumination from the p-side of the PIN (i.e., through the emitter of the HPT) and summing the drift current due to the electrons and holes, and this displacement current gives the total photocurrent as

$$i_{\rm ph}(t) = i_{\rm ph0}(t) - C_{\rm jn}\frac{dV_{\rm jn}}{dt} \tag{2}$$

where $i_{\rm ph0}(t)$ is the time-dependent primary photocurrent that is calculated according to Ramo–Shockley. The second term in (2) is the displacement current that occurs due to the changing junction voltage, equivalent to the charging of the junction capacitance.

The light in an APD is absorbed as a decaying exponential in the absorption region and the photocurrent from this is then amplified by avalanche multiplication in the avalanche region. Increased avalanche gain extends the transit effects and are included in the APD impulse response, calculated in [19]. To find the photocurrent, $i_{\rm ph0}(t)$, for the APD, the impulse response is convolved with a rectangular pulse train. The APD impulse response is a weighted mean of the impulse response of each carrier. The effects of deadspace on the excess noise factor and the effective transit times in the APD are included. In the calculation of the APD impulse response, it is assumed that the electrons and holes travel at their respective saturation velocities, but their differing ionization coefficients and ionization threshold energies are taken into account.

IV. Noise

The sources of noise in the photoreceivers are the thermal noise from the load resistor, source resistor, and the base resistance, and the shot noise due to the collector and base currents in the transistor [14]. An additional source of shot noise in the PIN-HBT and APD-HBT occurs as the photocurrent flows across the junction in the diode. The excess noise factor of the APD is calculated according to [22]. The shot noise from the APD is increased by the excess noise factor and the avalanche multiplication relative to the shot noise in the PIN diode, before being amplified by the HBT. The HBT circuit acts as a low-pass filter to the noise and the small-signal noise analysis by Liu [20] is used. The expressions derived in [17] for the base and load thermal noise and the base and collector current shot noise are the same for the diode-HBT receiver. At the frequencies of interest, the diode capacitance has a negligible effect on the small-signal frequency response and can be neglected. The source resistor is in series with the base resistance, and therefore, the response to the source noise is the same as the base thermal noise. The resultant equivalent noise circuit is shown in Fig. 2(b). The diode shot noise must be included in the diode-HBT and is given by

$$\overline{i_c^2}\Big|_{\rm diode-HBT} = \overline{i_c^2}\Big|_{\rm HPT} + 2eFMi_{\rm ph0}B_n \tag{3}$$

where $\overline{i_c^2}|_{\rm HPT}$ is similar to that from [17], F is the noise factor, M is the avalanche multiplication, and B_n is the noise bandwidth. An additive Gaussian noise distribution is assumed [23], which is superimposed on the calculated signal in order to calculate the bit error rate (BER) as described in [17].

V. Results and Discussion

We modeled InP/InGaAs devices here, but the model could be applied to other materials by changing the material parameters. The output characteristics for the photodetectors considered include bit rate, sensitivity, and responsivity. The material systems of the different schemes considered are shown in Fig. 1.

The diameter of the photodetector portion of the receiver is important since it affects the fiber coupling efficiency and capacitance in the device. This is particularly important in the HPT since the forward-biased base–emitter junction capacitance contributes significantly to the delays. The tradeoff between coupling efficiency and capacitance is somewhat removed in the diode-HBT since the coupling of light is into the separate reverse-biased photodiode, allowing the HBT junction capacitances to be reduced. This independence of transistor capacitance and optical coupling efficiency is a major advantage of the PIN-HBT over the HPT, and offers greater design flexibility.

The diameters of the optical window PIN diode, APD and the HPT are taken as 9 μm, giving a diode or an emitter area of 63.6 μm^2. The base–collector diameter has been set at 8 μm in the HPT. An emitter area of 5 μm^2 and the base–collector junction area of 10 μm^2 are used in the separate HBTs. A minimum lateral dimension of 1 μm is assumed in the HBT, i.e., an emitter width of 1 μm, and the spacing between the base contact and the emitter edge of 1 μm is used in calculating the base resistance. The base resistance is calculated as the resistance of the base material between the base contact and the emitter edge. It is a function of the base thickness that is used to define the dc gain β. The base–emitter bias source resistance $R_S = 100\ \Omega$ unless otherwise specified and the load is 50 Ω.

The receivers are characterized by sensitivity and responsivity. The sensitivity is defined as the minimum power of the light that passes though the absorption region to achieve BER =

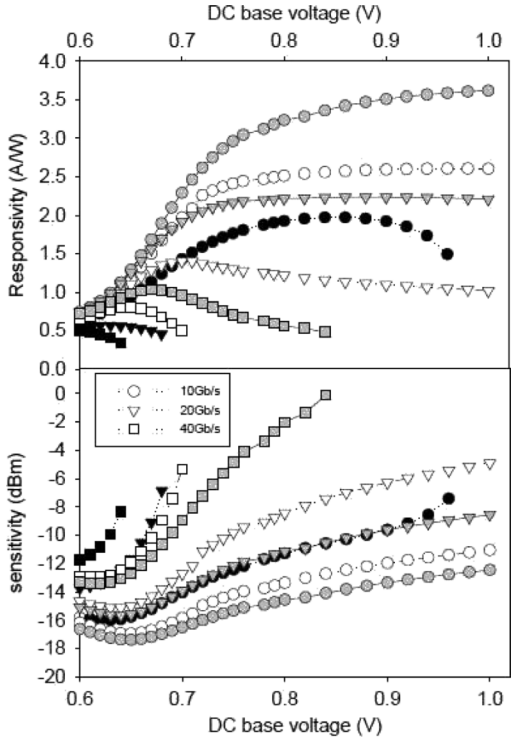

Fig. 3. (a) Responsivity and (b) sensitivity as a function of dc base–emitter voltage, $V_{\rm dc}$. Calculated values at 10 Gb/s (circles), 20 Gb/s (triangles), and 40 Gb/s (squares) for HPT (solid symbols), shared PIN-HBT (open symbols), and separate PIN-HBT (gray symbols) are shown.

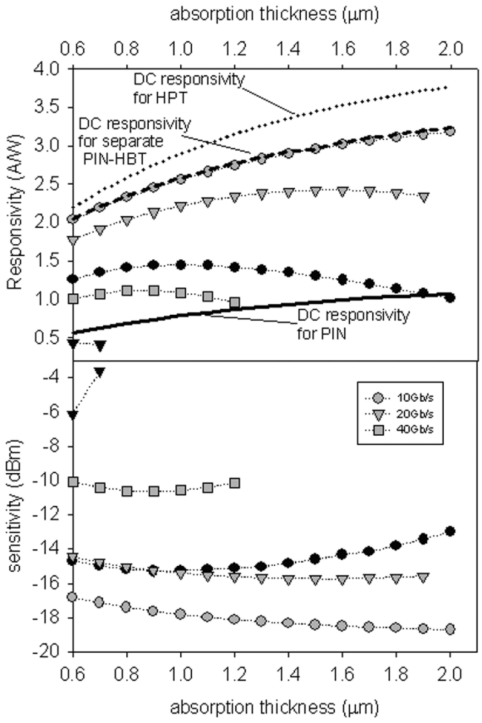

Fig. 4. (a) Responsivity and (b) sensitivity as a function of absorption thickness for the HPT (solid symbols) and the separate PIN-HBT (gray symbols) at bit rates of 10 Gb/s (circles), 20 Gb/s (triangles), and 40 Gb/s (squares). The maximum responsivity from each device and that of a PIN diode are represented by lines.

10^{-9}. Intersymbol interference was not included in our analysis. In order to account for coupling and other external limitations, the optical power applied to the device is given by $P_0/\eta_{\rm ext}$, where $\eta_{\rm ext}$ is the external efficiency. The frequency-dependent responsivity is defined by the minimum change in collector current (Δi_c), which indicates a digital "1" divided by the input power. The sensitivity has a direct bearing on repeater station spacing in a fiber optic system. The responsivity affects the voltage that appears across the load resistance that will be applied to subsequent electronics.

The effect of the base–emitter dc bias voltage on the sensitivity and responsivity is shown in Fig. 3 for transistors with $\beta = 10$ and absorption thickness $W = 0.6$ μm. In the HPT and the shared layer PIN-HBT, the latter defines the collector thickness, but in the separate PIN-HBT, the collector thickness has been reduced to 0.2 μm to reduce the collector transit delay [the second term in the denominator of (1)]. Increasing the dc bias voltage increases the collector current that reduces the emitter dynamic resistance. However, as the latter is reduced, the effective gain is increased since more primary photocurrent flows into the base of the transistor. This has the effect of increasing the overall charging delay [17], leading to a closure of the eye and a reduction in the responsivity if charging delays are significant with respect to the bit rate. This can be seen in Fig. 3(a), where the responsivity initially improves with increasing gain (controlled by $V_{\rm dc}$) for the two lower bit rates, but then decreases as the charging delays become important. The increasing gain also initially improves the sensitivity, but it too starts to degrade [Fig. 3(b)]. The factors contributing to the degradation of the sensitivity are the increased charging delays, an increase in the noise due to a reduced r_π, and an increase in the base shot noise with larger base current. The complex interplay between these many factors makes it difficult to explain all the trends in Fig. 3 in a simple fashion. However, in the two PIN-HBT configurations, the reduced HBT areas possible compared to the HPT mean that the capacitance delays play a smaller part in the degradation of the device performance. Optimizing the collector thickness for reduced collector transit delay without compromising the capacitor charging delay in the separate PIN-HBT leads to the improved performance compared to the HPT alone and the shared PIN-HBT device.

Increasing β in the model by reducing the base thickness, while keeping the collector current constant, leads to some degradation in the sensitivity due to increasing delays from the Miller effect. The dc responsivity does not increase linearly with β since the effective gain is determined by the bias conditions as well as β.

One of the most important factors affecting the performance of the HPT and PIN-HBT is the absorption thickness. The responsivity and sensitivity are plotted as a function of absorption thickness in Fig. 4(a) and (b), respectively, for the HPT (absorption thickness = collector thickness) and the separate layer PIN-HBT (absorption thickness = PIN I-region) for a collector current of 1 mA. The tradeoffs inherent in the choice of collector thickness of the HPT and shared layer PIN-HBT are increasing its thickness to increase the internal quantum efficiency and reduce the base–collector capacitance on the one hand, versus reducing the thickness to minimize the collector transit times on the other hand. To preserve clarity, only the HPT and separate

PIN-HBT devices are compared in Fig. 4. The collector thickness in the HBT of the separate PIN-HBT has been set at 0.2 μm as a compromise between the capacitance charging delays and the collector transit delay in the HBT. An optimum absorption thickness is evident for some of the curves in Fig. 4(a) and (b). The optimum thickness is smaller for the HPT compared to the separate PIN-HBT since the collector transit delays rapidly become dominant in the HPT. In the separate PIN-HBT, the sensitivity and responsivity only start to degrade when the transit delays in the PIN diode are significant with respect to the inverse bit rate. For comparison, the calculated dc responsivity for the HPT, separate PIN-HBT, and a single PIN diode are shown in Fig. 4(a). The dc responsivities were calculated using $R = e/h\upsilon(1 - \exp(-\alpha W))$ applied to the absorption regions in each. At 40 Gb/s the responsivity of the separate PIN-HBT is close to the dc value for a PIN diode. At 10 and 20 Gb/s, the responsivity of the separate PIN-HBT is much greater than the PIN alone, while the HPT has higher and lower responsivity values at 10 and 20 Gb/s, respectively, compared to the value for the PIN diode. In the HPT, the biasing condition of 1 mA leads to large capacitance delay that prevents the operation of the HPT at 40 Gb/s. Hence, no results for HPTs at 40 Gb/s are shown in Fig. 4.

The most complicated structure considered here is the APD-HBT [Fig. 1(c)]. Alongside the factors discussed before for the HPT and separate PIN-HBT, the avalanche gain in the APD can be used to optimize the performance of an APD-HBT receiver. In Fig. 5, the avalanche gain is varied by changing the applied APD bias. The HBT has a collector thickness of 0.2 μm and $\beta = 10$. The modeled InGaAs/AlInAs APD has an absorption layer thickness of 0.6 μm and an avalanche region of 150 nm. The charge layer, which is 50 nm thick and doped at 5×10^{17} cm^{-3}, is designed to ensure that the high field in the avalanche regions does not extend into the absorption region. The APD structure was chosen such that tunneling current is negligible and the noise from the APD is dominated by the multiplied photocurrent shot noise. This enables the avalanche gain and excess noise factor to be well controlled. The responsivity and sensitivity as a function of avalanche gain have been plotted in Fig. 5(a) and (b), respectively, using the model described in Section III. Initial improvement in both sensitivity and responsivity of the receiver with increasing avalanche gain can be clearly seen. The optimum values of avalanche gain occur at a point where the diode transit times and excess avalanche noise start to close the eye. The APD avalanche duration increases with increased avalanche gain and dominates the delay at lower gain for the higher frequencies. Consequently, the responsivity that can be achieved at 40 Gb/s is lower than the maximum (dc) at 10 and 20 Gb/s, but is still larger than the responsivity achieved by the separate layer PIN-HBT at 40 Gb/s (shown by the solid symbols in Fig. 5 at $\text{gain} = 1$).

To optimize and compare all the devices considered, simulations were performed at bit rates from 2 to 40 Gb/s and the design parameters of layer thickness, source resistance, and dc base voltage have been varied. The avalanche multiplication, adjusted by the APD supply voltage V_{APD} is a further variable used in the optimization of the APD-HBT. The input power is adjusted until a BER of 10^{-9} is achieved, and this is then

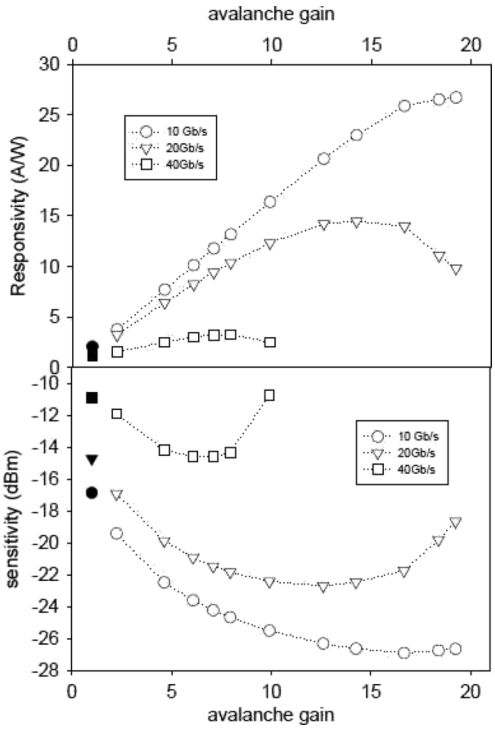

Fig. 5 APD-HBT (a) receiver responsivity and (b) sensitivity as a function of avalanche gain in the APD for bit rates of 10 Gb/s, 20 Gb/s, and 40 Gb/s. The solid symbols are PIN-HBT receiver simulations which can be thought of as an APD-HBT with an avalanche gain of unity.

taken to be the sensitivity. The device structure that achieves the best sensitivity at a given bit rate is taken to be the optimum device and the line plotted in Fig. 6 is the locus of these optimums. Thus, each point at a given bit rate is a different optimized device. The separate layer PIN-HBT achieves sensitivities of -21.1 and -14.1 dBm, which represents 2.3 and 0.6 dB improvement over the HPT, for bit rates of 10 and 40 Gb/s, respectively. This improvement is due to the reduced collector transit times in the HBT which is achieved without loss of internal efficiency, and the reduced capacitance of the separate transistor. The shared layer PIN-HBT has no real advantage over the HPT considered here. At the highest and lowest bit rates considered, the photoreceivers have similar sensitivity performance. At low bit rates, the optimum absorption thickness for each detector is large (limited to a maximum of 2 μm in the optimization process). Since the switching period is large compared with the delay times in each of the devices at low bit rates, the responsivity and sensitivity are not degraded by the delays. At the highest bit rates, the optimum gain is reduced in all three devices; therefore, each starts to look more like a PIN diode and their response is similar. At bit rates around 10 Gb/s, the collector transit delays are significant with respect to the bit period. There is, therefore, a strong tradeoff between collector thickness and responsivity/sensitivity in the HPT and shared layer PIN-HBT. The PIN diode thickness can be kept large, increasing the responsivity and giving higher sensitivity, in the separate layer PIN-HBT at these bit rates. The PIN-HBT has the advantage that the photodetector area can be increased to ease fiber alignment with less degradation of the sensitivity than in the HPT. If it is of interest to increase responsivity at the high bit

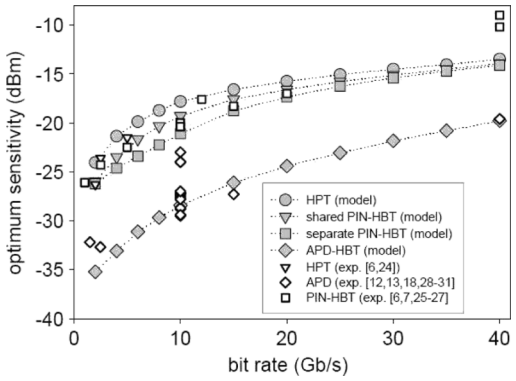

Fig. 6. Calculated optimum sensitivities for HPT, shared layer PIN-HBT, separate PIN-HBT, and APD-HBT as a function of bit rate are represented by gray symbols. Experimental data for HPTs, PIN-HBTs, and APD-based receivers are represented by open symbols.

rates, e.g., through increasing effective gain using bias, it is the separate layer PIN-HBT whose sensitivity will degrade least.

The APD-HBT receiver has a clear advantage over the other receivers, achieving -28.7 and -19.9 dBm (translates to >140 GHz gain–bandwidth product) at 10 and 40 Gb/s, respectively. The decrease in the difference of the sensitivity of the APD receiver compared to the other devices at high speeds is expected since the optimum avalanche gain is decreased due to avalanche duration delays, and therefore, the APD begins to behave more like a PIN diode. At speeds greater than 40 Gb/s, Fig. 6 indicates that the APD-HBT performance will approach that of the PIN-HBT since the optimum avalanche gain will tend toward one.

Data from [6] and [24] for the HPT, [6], [7], and [25]–[27] for the PIN-HBT, and [12], [13], [18], [28]–[31] for the APD-HBT have been plotted to compare with experimental data. The differences between calculation and experimental data up to 20 Gb/s are within ± 1 dB for the HPT and PIN-HBT receivers, which seems reasonable given that measured sensitivity values can vary by as much as ± 1 dB between identical channels of a PIN-HBT photoreceiver in [32]. At 40 Gb/s, parasitics due to interconnects between the PIN diode and the HBT, which have been neglected here, are likely to degrade the experimental results compared to the modeling.

The measured sensitivities of hybrid APD-based photoreceivers from [12], [13], [18], and [28]–[31] are plotted and show a good fit to the simulated line. It should be noted that a waveguide APD, which removes the tradeoff between transit times and absorption efficiency, is used to achieve the record result of -19 dBm at 40 Gb/s [12]. Furthermore, the circuitry used in the photodetectors above 10 Gb/s includes transimpedance amplifiers, which improve the sensitivity of the photodetectors [21] but have not been included here.

We have also optimized these photodetectors under more stringent conditions of BER $= 10^{-10}$ and BER $= 10^{-12}$. The predicted optimum sensitivities achieved at 40 Gb/s are summarized in Table I. Under these conditions, the APD-HBT offers the highest sensitivities of -19.5 and -19 dBm, while the HPT has the lowest sensitivities of -13.2 and -12.8 dBm, for BER of 10^{-10} and 10^{-12}, respectively.

TABLE I
PREDICTED OPTIMUM SENSITIVITIES OF VARIOUS PHOTODETECTORS FOR THE TWO HIGHER BERS

Device	BER=10^{-10}	BER=10^{-12}
HPT	-13.2 dBm	-12.8 dBm
Shared-Layer PIN-HBT	-13.7 dBm	-13.3 dBm
Separate-Layer PIN-HBT	-13.9 dBm	-13.4 dBm
APD-HBT	-19.5 dBm	-19.0 dBm

VI. CONCLUSION

Large-signal charge control models based on the same theory for the HPT, the PIN-HBT, and the APD-HBT have been developed. These photoreceivers have been optimized in terms of sensitivity, responsivity, and design parameters, which enable the schemes to be compared directly for the first time.

The HPT and PIN-HBT are very similar devices in both operation and fabrication, including a similar layer structure. One disadvantage of the PIN-HBT is that it is a slightly more complicated photodetector than the HPT because of the need for two mesas and the interconnects between them. The parasitic capacitance and inductance associated with the interconnects have not been included in this modeling. The advantage of the separate mesas is the decoupling of the capacitances in the transistor (which affect the speed) and the area of the photoreceiver (which affects the coupling efficiency). The HPT is simpler, being only one mesa, but the need to minimize area to reduce capacitance is limited by the need for efficient optical coupling. For the active detection area considered here (63.6 μm^2), there is little to be gained from using the shared layer PIN-HBT. Using a separate layer for the PIN diode to the collector removes the tradeoff between internal efficiency and collector transit delays. The APD-HBT receiver is the best performer, but at the expense of a more complicated structure. Optimizing the growth of such a structure could be problematic and the yield may be low. However, the increased sensitivity afforded by the APD suggests that APD-based receivers will be key to next-generation systems.

Optimum sensitivities of -13.5 dBm for the HPT, -14.1 dBm for the separate layer PIN-HBT, and -19.9 dBm for the APD-HBT have been calculated for single transistor amplifier receivers operating at 40 Gb/s (for BER $= 10^{-9}$) using a single pass of light. This trend remains when calculations were repeated for BER $= 10^{-10}$ and 10^{-12} showing that the APD-HBT offers the highest sensitivities as the bit rate increases.

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