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Hybrid architecture for shallow accumulation mode AlGaAs/GaAs heterostructures with epitaxial gates.

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Accumulation mode devices with epitaxially grown gates have excellent electrical stability due to the absence of dopant impurities and surface states. We overcome typical fabrication issues associated with epitaxially gated structures (e.g. gate leakage and high contact resistance) by using separate gates to control the electron densities in the Ohmic and Hall bar regions. This hybrid gate architecture opens up a way to make ultrastable nanoscale devices where the separation between the surface gates and the 2D electron gas is small. In this work, we demonstrate hybrid devices made from the same wafer have reproducible electrical characteristics, with identical mobility and density traces over a large range of 2D densities. In addition, thermal cycling does not influence the measured electrical characteristics. As a demonstration of concept, we have fabricated a hybrid single-electron transistor on a shallow (50 nm) AlGaAs/GaAs heterostructure that shows clear Coulomb blockade oscillations in the low temperature conductance.

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Much attention is focused on modulation doped AlGaAs/GaAs devices which utilize an intentional doping layer to populate the 2D conducting channel. These type of devices are at the center of key experiments in semiconductor spintronics[1], qubits[2] and many body effects[3]. However these devices may not be ideal for applications requiring high charge stability or low carrier densities: not only do the remote dopants act as scattering centers (particularly in shallow devices [4]), charge motion between dopants is a significant source of noise in quantum devices[5–7]. Furthermore the surface gates can leak through the doping layer causing additional charge noise[8–10]. The alternative, accumulation-mode GaAs/AlGaAs heterostructures require a voltage applied to an overall top-gate[11,12] to induce carriers into the conduction channel, removing the need for intentional ionized dopants. Accumulation-mode devices are advantageous due to their charge stability[13] and robustness under thermal cycling[14].

In most accumulation-mode devices the top-gate spans the entire conduction region and slightly overlaps the Ohmic contacts in order to effectively contact, and induce, a continuous 2D conducting region. However the close proximity of the contacts to the top-gate can cause electrical shorts between the two[15–17]. The shorting of the top-gate to the contacts is particularly problematic in shallow semiconductor-insulator-semiconductor field effect transistors (SISFETs)[12] in which the top-gate is an *in situ*, degenerately-doped GaAs cap. In SISFETs a self-aligned Ohmic technique[18] is used to isolate the top-gate from the contacts, but despite tight control of the Ohmic fabrication steps, top-gate leakage is still a major issue[17]. The problem of top-gate leakage is enhanced in shallow devices because the contacts are in close proximity to the *in situ* top-gate, due to a thinner insulating AlGaAs region. Circumventing the top-gate leakage problem can be done with an alternative architecture whereby a metallic gate replaces the doped-cap. The metallic top-gate is isolated from the contacts by an amorphous dielectric layer in a metal-insulator-semiconductor field effect transistor (MISFET) configuration[15,19]. Furthermore MISFETs are advantageous because dual-gating is possible by using two metallic gates (with insulating layers in between) to either realize sub-micron features in accumulation-mode devices[20–22], or to independently control the accumulation layers near the contacts and in the conducting channel.[23,24]. The advantages introduced by the MISFET design come at the cost of using an amorphous dielectric which can cause charge noise[19,25]. Additionally surface states on the wafer can cause scattering even in 300 nm deep devices[26].

Here we demonstrate a hybrid device which combines the benefits of the MISFET and SISFET deigns: like MISFETs the hybrid architecture is simple to fabricate with a high yield and the design is compatible with both shallow and deep devices. Like some dual gated MIS

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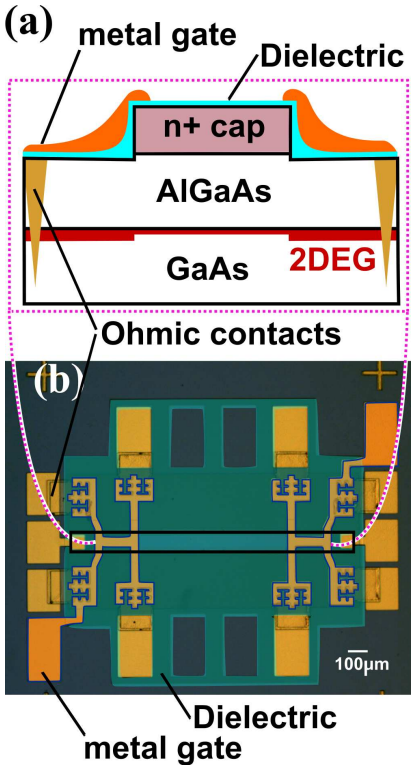

FIG. 1. (Color online) (a) A vertical profile of the hybrid-architecture is shown for a slice of the device shown in (b). The 2DEG is depicted with thick and thin lines representing the high density of electrons induced near the contacts, and the lower (variable) density of electrons in the 2D conduction channel respectively. (b) A colored optical micrograph of the device is shown here, the conduction channel lies under the doped $n+$ GaAs top-gate (outlined in black). An insulating dielectric AlO_x layer (light green) covers the top-gate isolating the top-gate from the metallic Ohmic gates which sit on top (colored orange). The dark blue box shows the location of one of the Ohmic contacts which lie under the Ohmic gates and dielectric. The bonding pads are shown in gold.

devices, the hybrid device has independent control of the contact and channel resistance; like SISFETs the active region of the hybrid device is all high-quality single-crystal with a heavily doped GaAs cap that eliminates the deleterious effects of surface charge and amorphous dielectrics. Furthermore standard nanostructure fabrication steps[14,27] can be incorporated into the hybrid device fabrication. The hybrid architecture retains the benefits of MIS and SIS structures by spatially separating the top-gate from the contacts using a dual gating scheme composed of two different materials. A degenerately doped GaAs cap is used as a top-gate similar to SISFETs, and metallic gates are deposited on top of a dielectric layer like MIS structures (see Fig. 1(b)). The carrier density near the contacts is controlled by metal ('Ohmic') gates which are deposited on an amorphous dielectric away from the active device region. The top-gate leakage is reduced by spatially separating the Ohmic contacts from the *in situ* GaAs top-gate, thus increasing the yield and simplifying the fabrication process. Additionally the independently-gated Ohmic regions ensure low density measurements are limited by the sample and not the contact resistance.

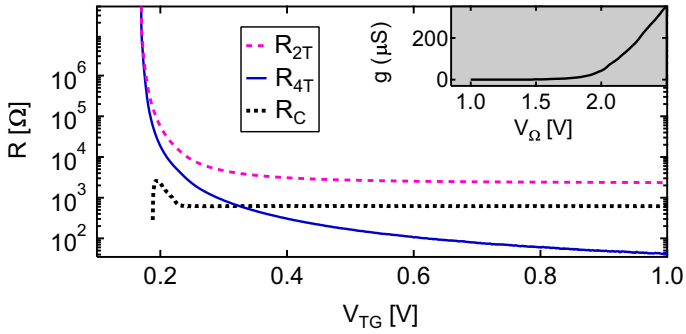

FIG. 2. (Color online) Contact resistance, two- and four-terminal resistance versus the voltage applied to the top-gate (V_{TG}) is shown for the 160 nm deep device. A constant voltage is applied to the Ohmic gates ($V_\Omega = 2.5\,\mathrm{V}$) while V_{TG} is varied. The contact resistance is independent of V_{TG}. Inset: two-terminal conductance versus V_Ω for one of the 160 nm deep devices when the top-gate is held fixed at $V_{TG} = 1\,\mathrm{V}$. The ohmic gates can 'turn off' the channel independently of the top-gate.

Figure 1(a) shows a side-profile schematic of a typical hybrid device. We fabricate both deep and shallow devices, the 'depth' of a device being defined as the thickness of the AlGaAs region. The deep (shallow) W0773 (B14507) heterostructure consists of a 160 nm (50 nm) AlGaAs layer on a GaAs buffer to form the 2DEG interface, followed by 25 nm (10 nm) of undoped GaAs spacer, and a 35 nm (31 nm) $n+$ doped cap. Optical lithography and a deep wet etch > 220 nm (> 91 nm) define the mesa then a shallow wet etch of the $n+$ cap is used to pattern the top-gate. A false color optical micrograph of a complete device is shown in Fig. 1(b), the top-gate region is outlined in red. Two gold bond pads contact the top-gate. NiAuGe Ohmic contacts are made to the 2DEG and a 30 nm layer of aluminum oxide (blue)[28,29] isolates the device from the Ti/Au ohmic gates (orange) deposited on the surface.

The behavior of the contact and channel resistances are first characterized at 4 K in a dc dip station using standard four-terminal ac lockin techniques, with an excitation voltage of 100 μV. The hybrid device operates by applying a fixed voltage to the Ohmic gates ($V_\Omega = 2.5\,\mathrm{V}$) to minimize the contact resistance. The resistance of the 2D channel is controlled by applying a separate voltage bias to the *in situ* top-gate (V_{TG}) and the maximum top-gate voltage ($V_{TG;max}$) is chosen so the leakage current between the Ohmic contacts and top-gate is ≤ 10 pA (the resolution limit of the Source Measure Unit SMU) when $V_\Omega = 2.5\,\mathrm{V}$. For the deep device $V_{TG;max} = 1\,\mathrm{V}$ and for the shallow device $V_{TG;max} = 0.5\,\mathrm{V}$.

Figure 2 is a plot of the two-terminal (R_{2T}), four-

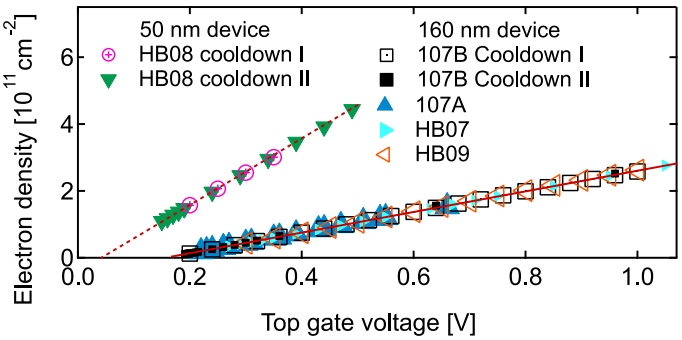

FIG. 3. (Color online) Electron density versus top-gate voltage for four deep devices and one shallow device. The density is identical for four different deep devices, and between thermal cycles both shallow and deep devices have reproducible density traces. The dashed and solid lines are lines of best fit for the shallow and deep devices respectively.

terminal (R_{4T}) and contact (R_C) resistances for the deep device 107B, and are representative of the traces obtained for other deep and shallow devices. Independent control of the channel resistance and contact resistance are evident in the dependence of R_C and R_{4T} on the top-gate voltage as the contact resistance is flat over a large range of top-gate voltages (the small upturn at low V_{TG} is probably an artifact of subtracting two large numbers R_{4T} and R_{2T} to get R_C). The channel resistance however, is dependent upon the top-gate voltage and decreases as V_{TG} increases. The two terminal resistance is the sum of all resistances from the source to the drain ohmics and follows a trend reflecting the sum of R_{4T} and R_C as expected. Independent control of the Ohmic gate is demonstrated in the inset to Figure 2, here the top-gate bias is fixed at $V_{TG} = 1\,\mathrm{V}$ while V_Ω is swept from 2.5 V down to 1 V. Although the channel is conducting when $V_{TG} = 1\,\mathrm{V}$, as V_Ω is reduced R_C increases correspondingly, until it comes to dominate the total resistance between the source and drain, resulting in the two-terminal conductance decreasing to zero.

The 2D electron density (n_s) and mobility (μ) are measured at low temperatures in a ^{3}He cryostat with a base temperature of 229 mK. The electron density is extracted from the slope of the Hall trace[30] at low magnetic field and is linearly dependent on V_{TG} as shown in Figure 3. The linear dependence of n_s is explained by treating the top-gate and 2D conducting channel as a simple parallel plate capacitor: $n_s = C_g(V_{TG} - V_0)/e$ where C_g is the parallel capacitance between the top-gate and the 2D channel, and V_0 is the gate bias at which $n_s = 0$. Both C_g and V_0 should be the same for all devices made from the same wafer. However if any charge accumulates between the gate and the channel over time, or between thermal cycles this will be reflected as a shift up or down in the n_s versus V_{TG} traces[31], and will result in different values of V_0. In MISFET devices, variations in charge trapped at the dielectric-GaAs interface can cause variations in V_0 from one cool down to the next. However in SISFET structures the variation in V_0 should be much smaller as only the reconfiguration of a (small) number of charges in the undoped AlGaAs can affect V_0. For each of the deep devices measured, with one device being measured on two separate cool-downs from room-temperature, all of the density traces lie on top of each other indicating any variation in charge trapped in the dielectric layer or elsewhere is not interfering with the applied gate potential in any of the deep devices measured. Lines of best fit for the 160 nm deep devices are $n_s = \left(\{3.08, 3.09, 3.16, 3.10, 3.14\} \times 10^{11}\mathrm{cm}^{-2}/\mathrm{V}\right) V_{TG} - \left(\{0.49, 0.48, 0.50, 0.49, 0.51\}\right) \times 10^{11}\mathrm{cm}^{-2}$ for devices 107A, 107B (first cooldown), 107B (after thermal cycling), HB07 and HB09 respectively. The y-intercept b is proportional to V_0[32], from the average b we calculate $V_0 = 0.13 \pm 0.001\,\mathrm{V}$[33]. The 1 mV error is less than the stability of the source meter unit[34] used to bias the top-gate. The electron density of the shallow device HB08 was varied over the range $9.86 \times 10^{10}\,\mathrm{cm}^{-2}$ to $4.44 \times 10^{11}\,\mathrm{cm}^{-2}$, with a line of best fit $n_s = (-0.40 + 9.86 V_{TG}) \times 10^{11}\,\mathrm{cm}^{-2}$. The line of best fit to the density for the shallow 50 nm device has a gradient ~ 3 times larger than that of the deep device as expected since the top-gate of the shallow 50 nm device is ~ 3 times closer to the 2DEG than the deep device.

Figure 4 shows the density dependent mobility for each of the devices measured. The mobility traces are highly reproducible, they lie on top of each other for devices made from the same wafer, and are stable when the devices are thermal cycled. We investigate the dominant scattering mechanism in the 2DEG by fitting a power-law exponent to the μ versus n_s traces[4] ($\mu \propto n_s^\alpha$). The 160 nm device has $\alpha = 1.1$, suggesting background impurities limit the mobility[4]. Detailed transport modeling[26] confirms a higher level of background impurities in the shallow 50 nm wafer[35] explaining the lower mobility. The deep (160 nm) and shallow (50 nm) devices are grown in different MBE chambers with different impurity concentrations, which is why they have different mobilities.

Accumulation-mode devices, with reproducible transport properties and low R_c at low n_s are promising candidates to study the effects of disorder and interactions in the low density regime[36], where interactions are strongest. Indeed Figs. 4 (b) to (d) show clean, symmetric Shubnikov de Haas (SdH) oscillations for low and high electron densities in both shallow and deep devices, indicating there is no parallel conduction, and the clean traces down to low density for the deep device show the ohmic resistance is not dominating the ρ_{xx} traces.

Clean, symmetric SdH are shown in Fig. 4(d) for the lowest measured density ($n_s = 1.2 \times 10^{10}\,\mathrm{cm}^2$) in the deep device HB08. Such low density SdH are possible due to the ohmic resistance remaining constant so that the operating range of the device is limited by the intrinsic properties of the conducing channel and not the resistance of the ohmic contacts. Indeed the SdH remain smooth as the sample undergoes a transition from quantum Hall liquid to insulator[37] at $B = \pm 0.5\,\mathrm{T}$ ($\nu \lesssim 1$),

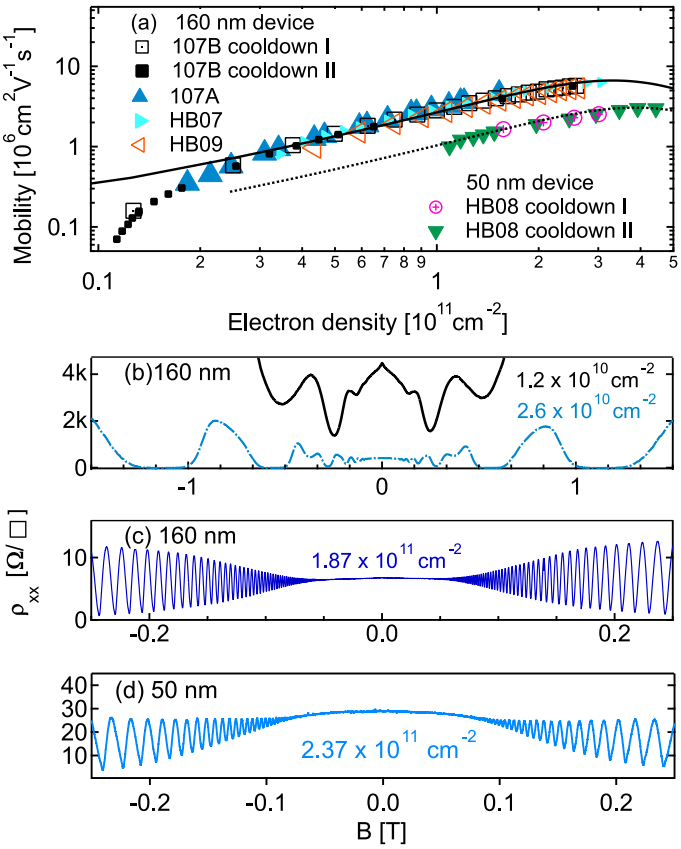

FIG. 4. (Color online) (a) Electron mobility versus electron density for four different deep devices and one shallow device. The mobility is reproducible for different devices and between thermal cycles when fabricated from the same wafer. The black dashed (solid) line is a fit to the mobility for the shallow 50 nm (deep 160 nm) device in the weak scattering limit ($k_f \ell \geq 10$, where ℓ is the mean free path). (b) Low and (c) high density Shubnikov de Haas oscillations appear in the longitudinal resistance (ρ_{xx}) for deep device 107B and are representative of the traces in other deep devices. The trace in (d) shows data from the shallow device HB08.

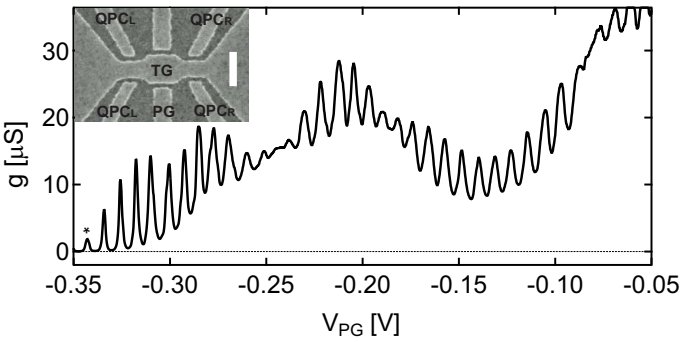

FIG. 5. A plot of the two-terminal conductance g versus plunger gate voltage V_{PG} of a quantum dot device made with the hybrid architecture. Measurement were performed with $V_L = -0.34\,\mathrm{V}$, $V_R = -0.28\,\mathrm{V}$, $V_{TG} = 1.2\,\mathrm{V}$, $V_{OG} = 2.5$ V at $T = 40\,\mathrm{mK}$ with an ac excitation of $30\,\mu\mathrm{V}$. A SEM image of the device is shown as an inset with a scale bar of 500 nm.

where ρ_{xx} increases over five orders of magnitude (the complete ρ_{xx} trace is not shown).

Combining the hybrid architecture with nanostructures is a reliable alternative to fabricating SISFET nanostructures. SISFET and hybrid nanostructures have identical fabrication steps[14], and thus the advantages of SISFET devices are retained by hybrid devices, with the additional benefits of reliable fabrication and low contact resistance. Here we demonstrate a quantum dot (QD) fabricated with the hybrid architecture (see Fig. 5). The QD is fabricated[14] on the deep 160 nm wafer, whereby the QD is defined by etching the $n+$ cap into seven separate gates forming a left quantum point contact (QPC), central dot region and right QPC in series, as shown inset to Fig. 5. The quantum dot and adjacent 2DEG reservoirs are populated using the top-gate, and the quantum point contacts at each end are used to control the tunnel barriers. Figure. 5 shows a series of Coulomb blockade oscillations when the bottom plunger gate is used to tune the dot occupancy. Coulomb blockade oscillations are manifested in the two terminal conductance g with clear zeros in g either side of the last peak (marked with a * in Fig. 5).

In summary, a hybrid architecture is presented for both deep and shallow AlGaAs/GaAs heterostructures, which use both a metallic and an *in situ* epitaxial gate. Reproducible transport measurements demonstrate the devices are highly stable with measurements limited by the intrinsic properties of the wafer and not by the contact resistance. Furthermore we demonstrate nanostructures can be integrated into the hybrid architecture.

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[33] $V_0 = ed/\epsilon_r\epsilon_0 b$, where $b = \{0.49, 0.48, 0.50, 0.49, 0.51\} \times 10^{11}\text{cm}^{-2}$. The mean value for V_0 is 0.13 ± 0.001 V. The standard error of the mean is calculated by $s/\sqrt{n} = 1$ mV, where $s = 0.00308$ V is the standard deviation, and $n = 5$ is the number of points.
[34] The reported limit to the reproducability/stability of the SMU, $\ell_{SMU} = 2\,mV$ (2400 Series SourceMeter Users Manual, Keithley Instruments, Inc. Cleveland, Ohio, U.S.A., Seventh Printing, May 2002 Document Number: 2400S-900-01 Rev. G).
[35] Reference [27] describes the model and fitting parameters used. The 50 nm (160 nm) device is fit using a background impurity density in the AlGaAs layer of $N_{AlGaAs} = 7.8(3)\times10^{20}$ m^{-3} and a thickness d_{AlGaAs}=50 (160) nm; $N_{GaAs} = 2.6(1) \times 10^{20}$ m^{-3} in the GaAs buffer layer ($d_{GaAs} = 1\,\mu$m for both devices); the surface charge density is set to zero in both cases and the interface roughness parameters are $\Lambda = 1.4\,(1.25)$ nm (correlation length) and $\Delta = 2.8(2.5)$ Å (roughness amplitude).
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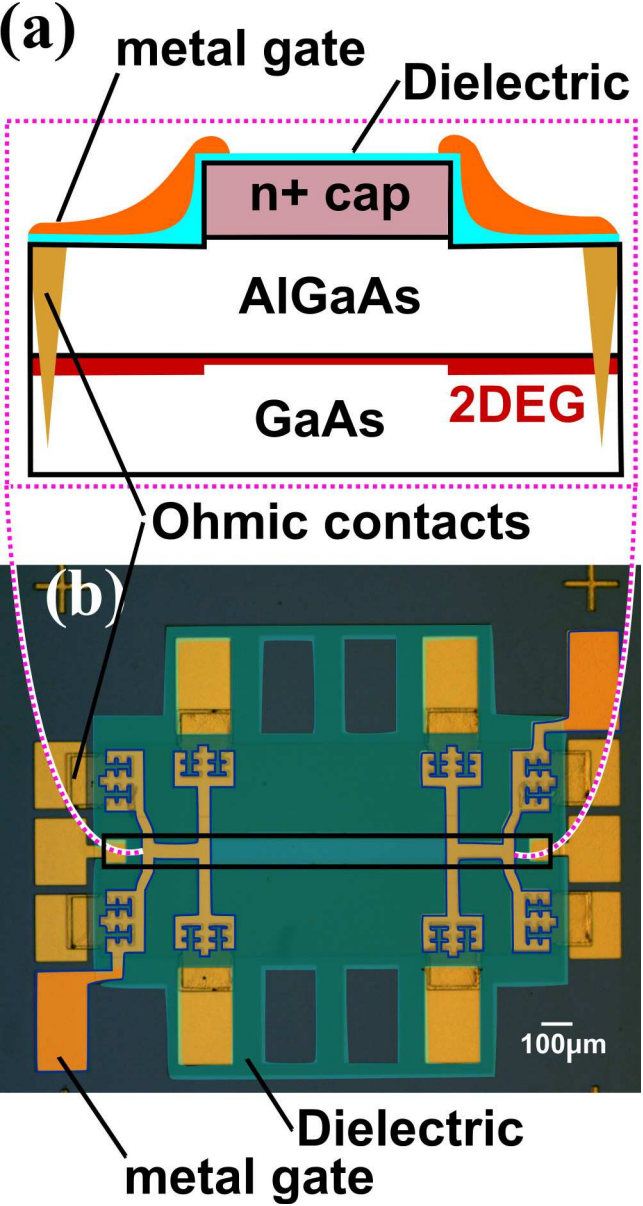
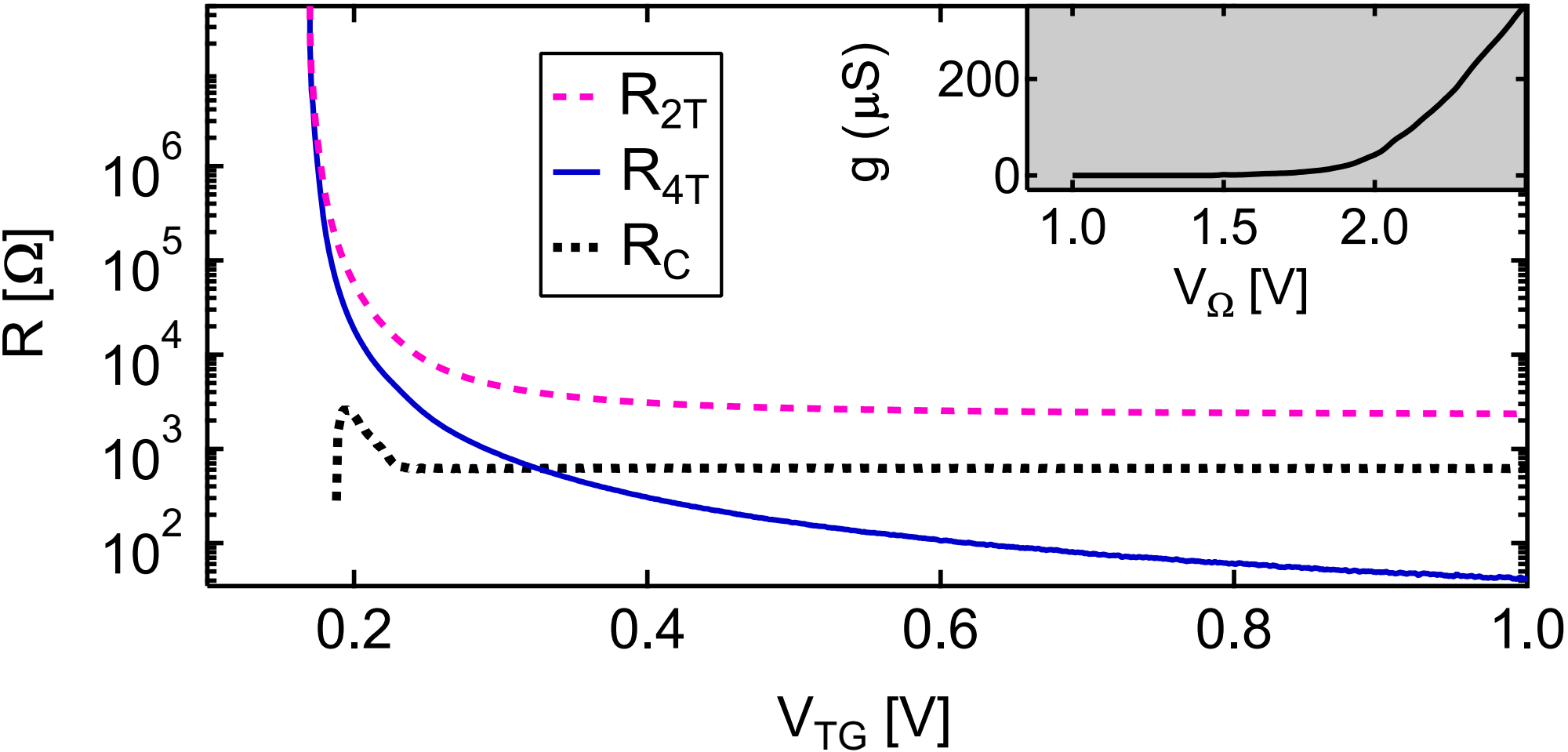
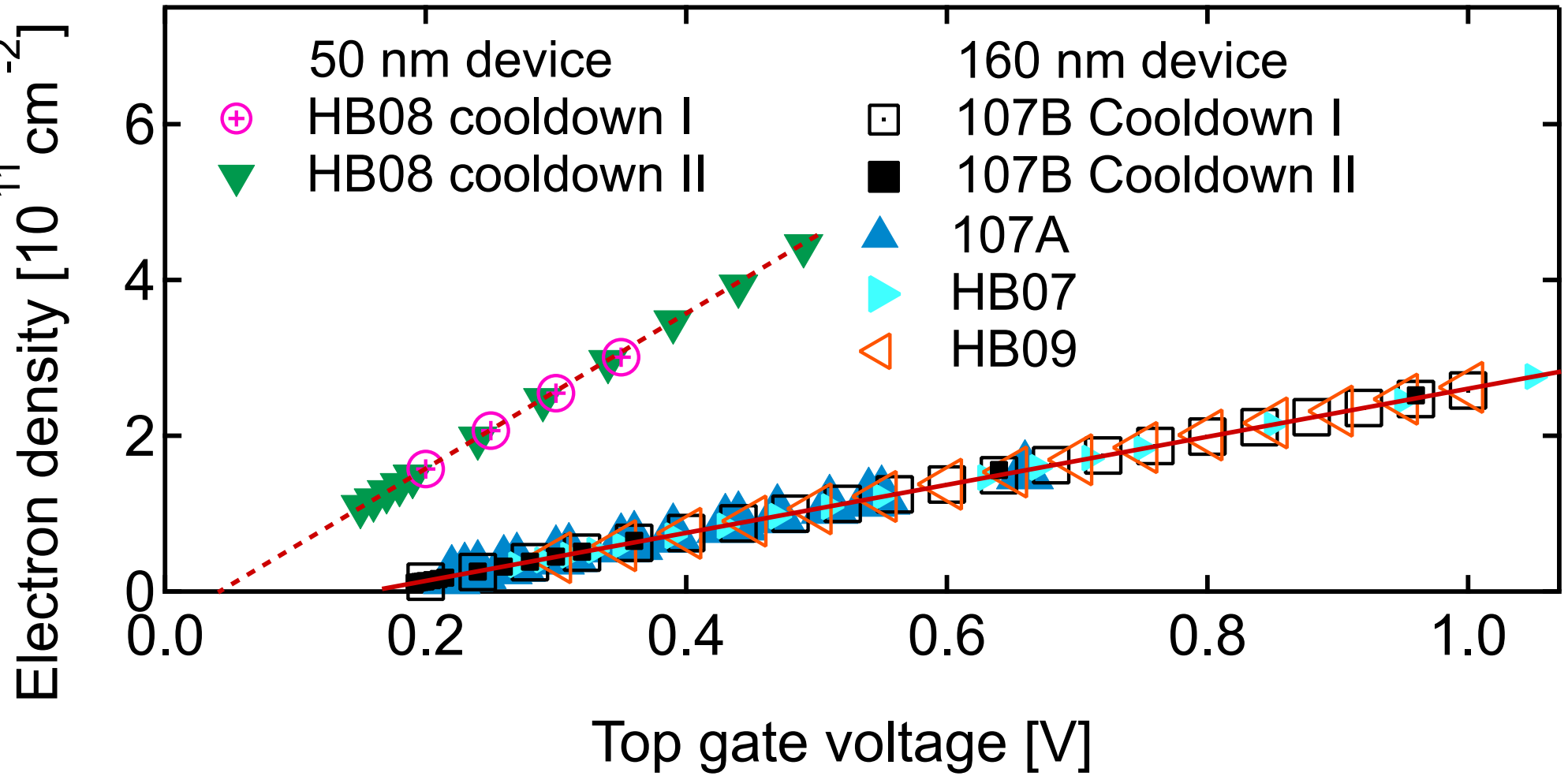
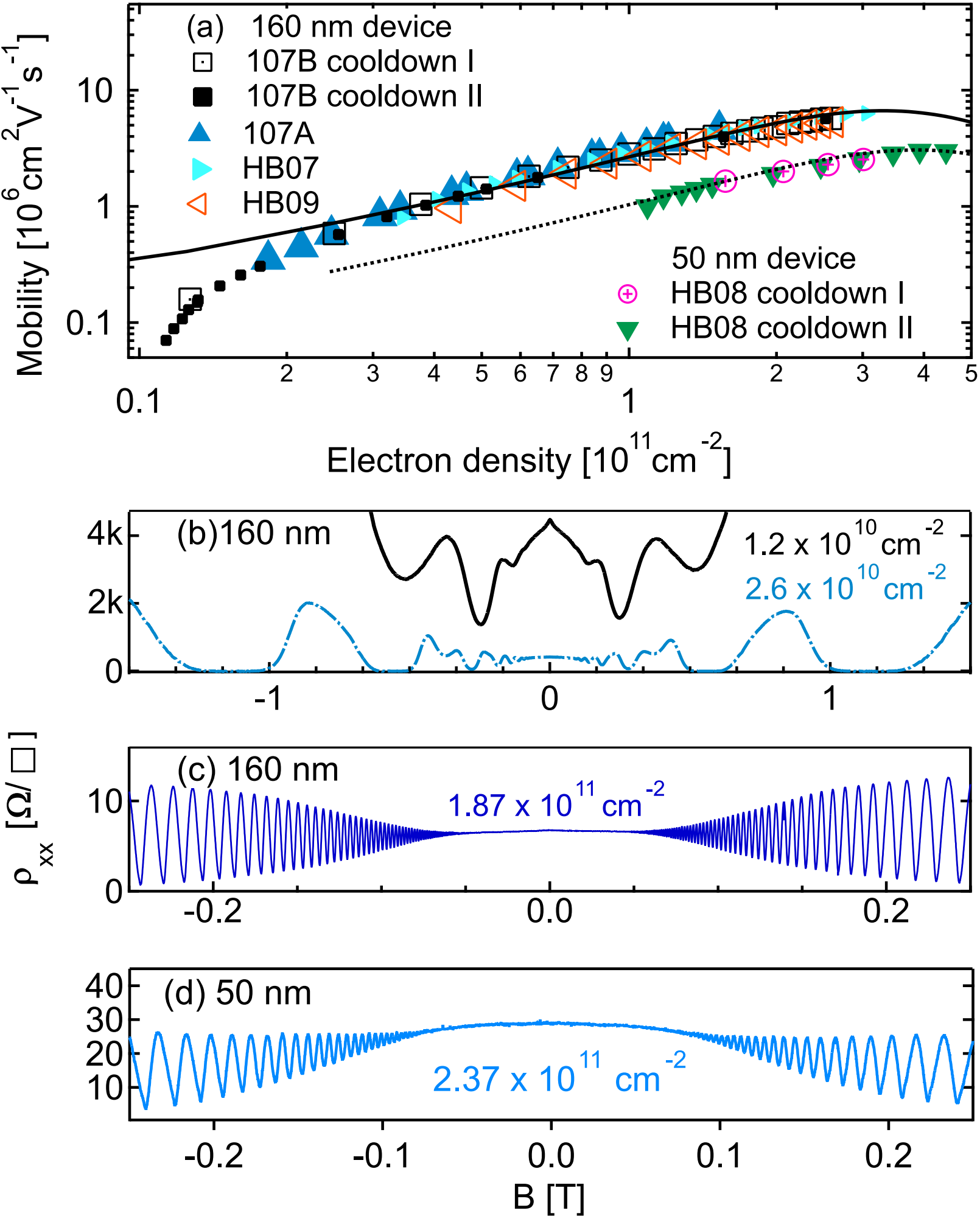
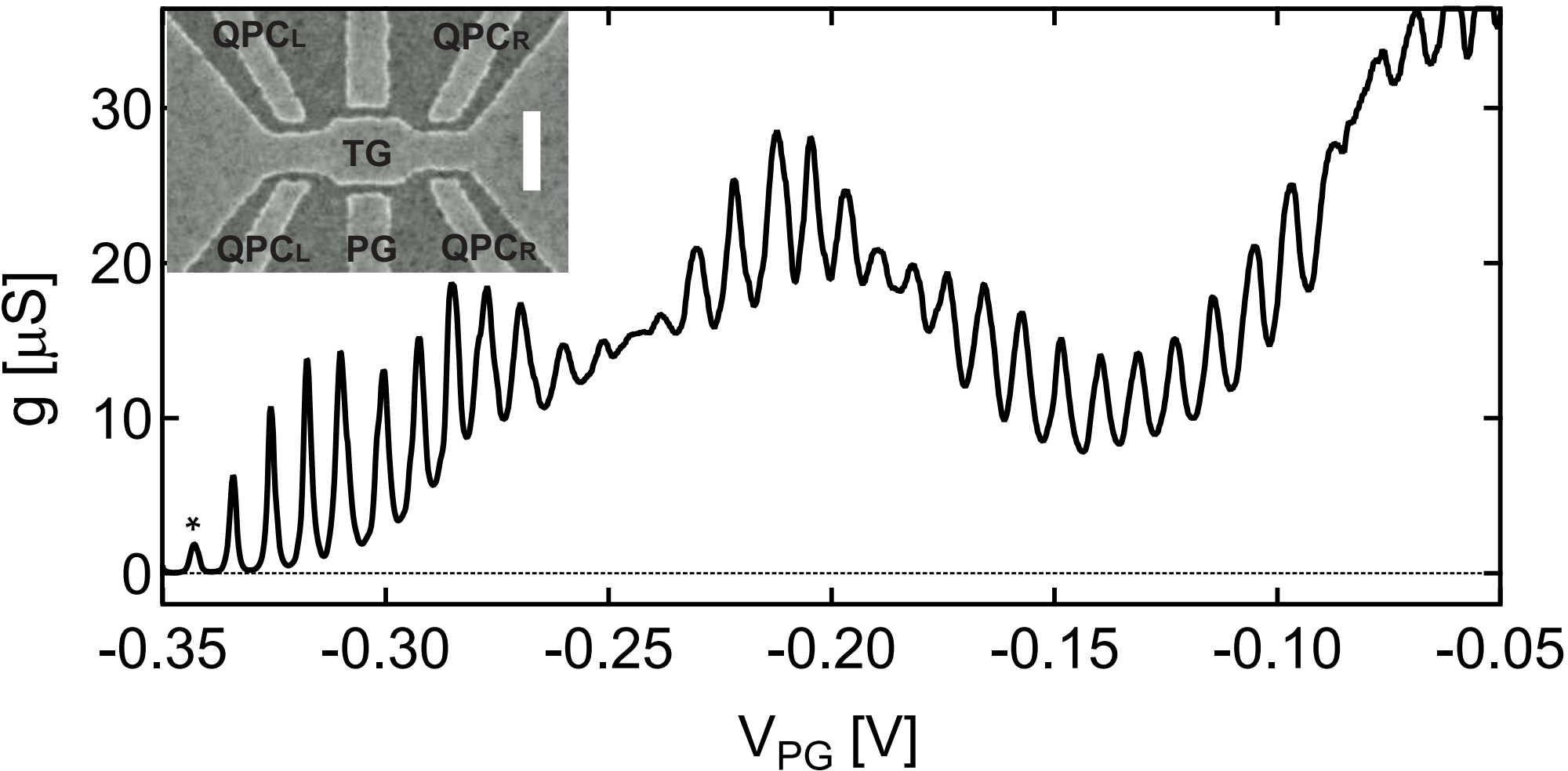

(a)
metal gate
Dielectric
n+ cap
AlGaAs
GaAs
2DEG
Ohmic contacts
(b)
100μm
Dielectric
metal gate


R [Ω]
10^6
10^5
10^4
10^3
10^2
0.2
0.4
0.6
0.8
1.0
V_{TG} [V]
R_{2T}
R_{4T}
R_C
g (μS)
200
0
1.0
1.5
2.0
V_Ω [V]


50 nm device
HB08 cooldown I
HB08 cooldown II
160 nm device
107B Cooldown I
107B Cooldown II
107A
HB07
HB09
Electron density [10^11 cm^-2]
Top gate voltage [V]
0
2
4
6
0.0
0.2
0.4
0.6
0.8
1.0


(a) 160 nm device
107B cooldown I
107B cooldown II
107A
HB07
HB09
50 nm device
HB08 cooldown I
HB08 cooldown II
Mobility [10^6 cm^2 V^-1 s^-1]
Electron density [10^11 cm^-2]
(b)160 nm
1.2 x 10^10 cm^-2
2.6 x 10^10 cm^-2
(c) 160 nm
1.87 x 10^11 cm^-2
ρ_xx [Ω/□]
(d) 50 nm
2.37 x 10^11 cm^-2
B [T]


QPC$_L$
QPC$_R$
TG
QPC$_L$
PG
QPC$_R$
30
20
10
0
g [μS]
*
-0.35
-0.30
-0.25
-0.20
-0.15
-0.10
-0.05
V_{PG} [V]