THE NEED FOR MACRO–MODELS IN THE SIMULATION OF EMI EFFECTS IN INTEGRATED CIRCUITS

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Abstract

The paper briefly reviews the previous work on the simulation of EMI effects in integrated circuits. Both component level and macro-models are considered. The relative merits of component level models and macro-models for EMI effects are discussed. In particular the problem of obtaining accurate data for component level models and the possibility of obtaining macro-model parameters by measurement are considered. The need to consider the coupling between all terminals is discussed. This contrasts with previous published work where only input to output effects are presented. Results are presented for some simple CMOS amplifier circuits.

I Introduction

Computer simulation of the performance of an ICL8741 operational amplifier was first described by Wooley & Wong in 1971 [1]. This paper provides an insight into the detail and complexity of simulating a subsystem which is so common that we now take if for granted. Among the programs used for this simulation was CANCER (Computer analysis of non-linear circuits excluding radiation), from which the SPICE (Simulation program with integrated circuit emphasis) family of simulators was developed by the University of California, Berkeley in the mid–1970s. Tuinenga's book [13] provides an excellent introduction to the history and capabilities of the SPICE family of circuit simulators though its emphasis is on the commercial package PSPICE.

The complexity of fully modelling each of the devices within a simple circuit, such as a logic gate or operational amplifier, caused the search for simplified models capable of accurately representing the overall function of a circuit to follow closely after the development of the first circuit simulators. The ICL8741 was again the first chip to feature in the literature with a simplified macro–model described by Boyle et al [2]. The macro–model reduced the computation time for simple op-amp circuits by a factor of six whilst producing results which were very close to the full model. The ideas of Boyle et al have been developed by a number of other workers [3], [4], & [5]. Macro models based on this work are widely available for modern operational amplifiers, often supplied by the IC manufacturers. An excellent overview of the technique is given in [6], which also suggests a number of developments to improve the performance of the macro–models.

As well as the reduction in complexity, the use of macro–models has the major advantage that detailed knowledge of the chip fabrication parameters is not required — the macro–model parameters can be determined easily from the manufacturers data sheet. This allows the chip manufacturers to keep their commercially sensitive fabrication data secret whilst providing the user with a model which is accurate for the specified operating range of the chip. However many macro–models do not accurately reproduce the operation of an integrated circuit outside its normal operating range or for power supply currents.

Modelling of the effects of electromagnetic interference on electronic circuits was first described by Larson & Roe [7] who developed a modified Ebers–Moll transistor model to allow the demodulation effect due to the non-linearity of a bipolar transistor junction to be simply modelled in circuit simulations. The essence of the model was to introduce a dc current into the transistor proportional to the incident rf power. The rf signal does not need to be simulated, greatly reducing the simulation time. However the model is only appropriate where a single frequency interference is present and could not be used for transient effects. This transistor model was used by Tront, Whalen et al [8] to develop an EMI macro–model for the 741 op-amp. Other macro-models of the 741 op–amp have been developed ([10, 11]) which use full transistor simulations for the input stage, where most of the non-linear effects occur, whilst using ideal circuit elements (e.g. dependent voltage sources) for the remainder of the amplifying stages.

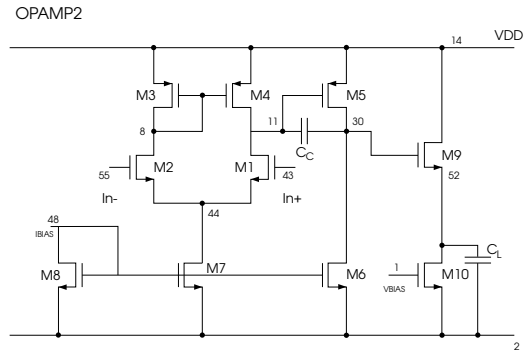

Figure 1: The op-amp circuit showing node numbers

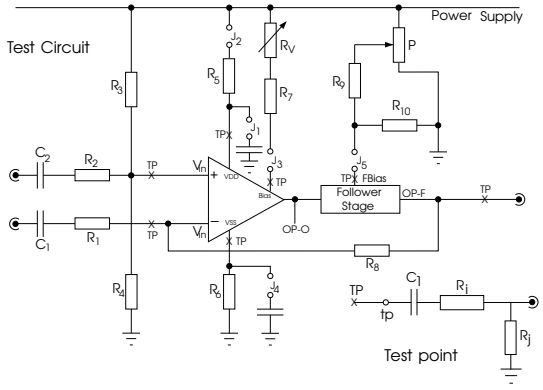

Figure 2: Test circuit for the op-amp showing the output source follower stage as a separate block, and current monitoring links. The EMI injection circuit (test point) is shown separately.

The published EMI macro–models concentrate on mimicking the demodulation effects of EMI at the input terminals of a 741 (or similar) op-amp. However EMI may enter through any terminal and macro–models are required which will accurately mimic the complete circuit behaviour. Work is currently being carried out at the University of York, in collaboration with KIHWV to develop full macro–models which mimic the interaction of EMI between all terminals.

A significant entry point for EMI is via the power supply rails of a circuit. It is in this area that this paper presents some results.

The work described above and the remainder of this paper considers only interference entering the chip from outside via the circuit connections. This approach is valid for many applications because the small physical size of the chip means that direct pick-up by the chip itself is negligible.

II The CMOS Integrated Circuits

A CMOS integrated circuit fabricated as part of a student project at the Katholieke Industriele Hogeschool West-Vlaanderen (KIHWV), Belgium, is used for the work carried out in this study because the detailed device parameters are available. On the chip are fabricated two op-amps, and two operational transconductance amplifiers (OTAs). The two op-amps use the same circuit configuration but different transistor geometries; as do the two OTAs.

The op-amp circuit is shown in Figure 1. The input stage is a differential amplifier input stage (M1 & M2) with current mirror active loads (M3 & M4). This is followed by a common source stage (M5) with a constant current active load (M6). A source follower output stage (M9) is used with a constant current load (M10). The bias current for the differential amplifier and common source stages are supplied via the current mirror circuit M6, M7, and M8. The current in M8 is set by an external bias circuit and controls the current in M6 and M7. The current in the output stage is set by the gate bias voltage applied to M10. Closed loop stability is ensured by the on-chip miller capacitance C_c. The test chip is encapsulated in a 40-pin dual in-line package with each circuit having separate power supply and ground connections.

III The test circuit

A test circuit was devised (Figure 2) to determine the performance of the op-amp and OTA circuits when configured as a differential amplifier. The circuit was fabricated on a double sided printed

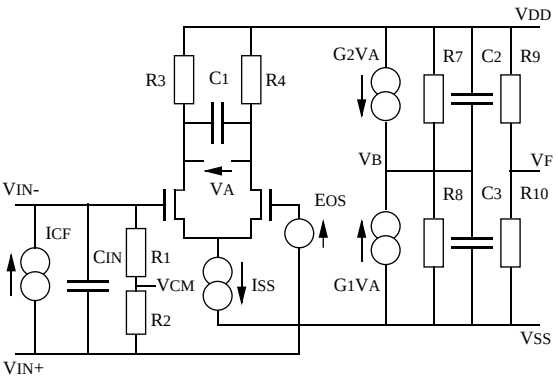

Figure 3: PMI Macro–model (input circuit).

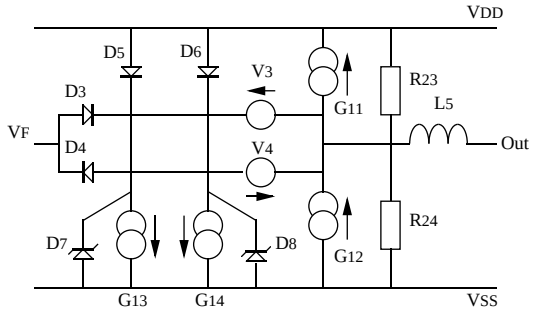

Figure 4: PMI Macro–model (output stage).

circuit board with one side dedicated to a continuous ground plane. The presence of a ground plane provides well defined parasitic capacitances for the circuit board and minimises inter-track coupling. Test points were included to allow radio-frequency interference to be injected at any pin of the IC with minimal effect on normal circuit operation. Current monitoring jacks (J2 and J5) were also provided to allow the circuit quiescent conditions to be set accurately.

IV The Macro–model

The enhanced Boyle macro–model of Alexander and Bowers of Precision Monolithics Inc. (PMI) [6] is used to determine the low frequency performance of the amplifier. This is shown in Figures 3, 4, and 5. The input stage is simplified version of the real op–amp. Subsequent stages using voltage controlled current sources (VCCSs) allow the frequency response of the amplifier to be set with an arbitrary degree of accuracy.

The output stage also uses a number of VCCSs (Figure 4) with diodes to limit the output voltage swing and to provide output current limiting. The common mode gain and frequency response is set independently by further VCCSs (Figure 5). The voltage, V_E generated by the common mode circuit is scaled and added to the input offset voltage source in Figure 3. This part of the model can easily be created directly from the manufacturer's data sheet for any op-amp.

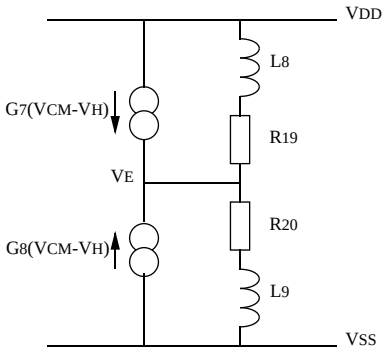

Figure 5: PMI Macro–model (common mode gain section).

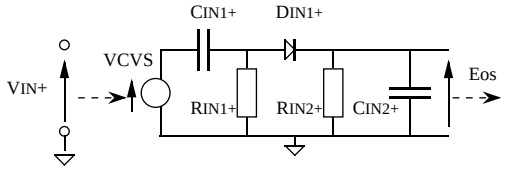

Figure 6: Addition to the PMI Macro–model to model demodulation effects at each input of the op–amp.

In order to model the demodulation effects in the op–amp a separate circuit can be included (Figure 6). The ac coupled input waveform is directly rectified and a scaled version fed to the offset voltage source in Figure 3. Though a simple frequency independent network has been used here, it would be straightforward to add a frequency dependent network to cause the demodulation to have a variation with frequency. A polynomial source could be used to model the real non-linearity more closely.

In order to model coupling from the power supply pin to the output of the op-amp a frequency dependent network was developed (Figure 7) which mimics the small signal response of the full circuit model. An additional non–linear network (currently of the same form as Figure 3) is used to account for additional demodulation effects in this coupling path. These networks control a current source (G_{DD}) which acts in parallel with those in the output stage (4).

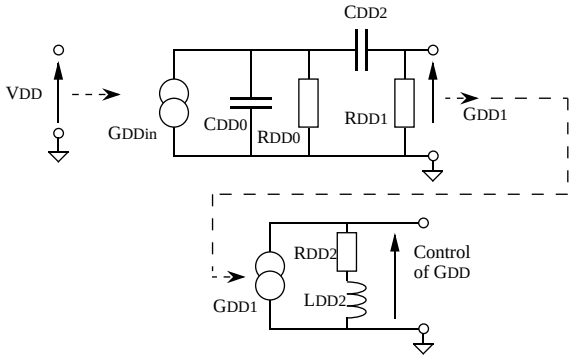

Figure 7: Addition to the PMI Macro–model to mimic coupling from Vdd to the output of the op–amp.

V Results

V.1 Frequency response

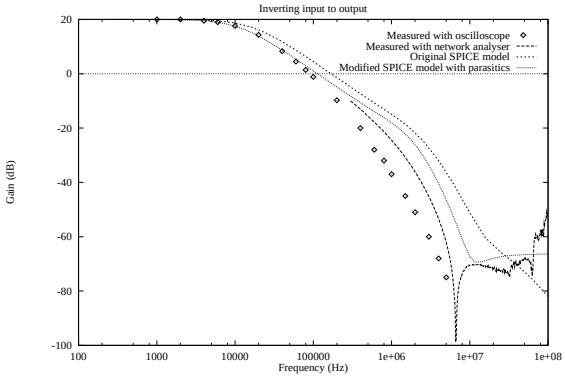

Figure 8: Frequency response of op-amp circuit – computed (full circuit models) and measured.

For frequencies below 300 kHz the response was measured using a signal generator and oscilloscope. Above 300 kHz a vector network analyser was used. Due to the low currents used in the op-amp circuit an oscilloscope was used as a pre-amplifier for the network analyser. Whilst the phase and gain characteristics of the oscilloscope are removed from the measurement in the analyser calibration process, the oscilloscope has only a 50 MHz bandwidth so measurements above this frequency must be regarded with suspicion.

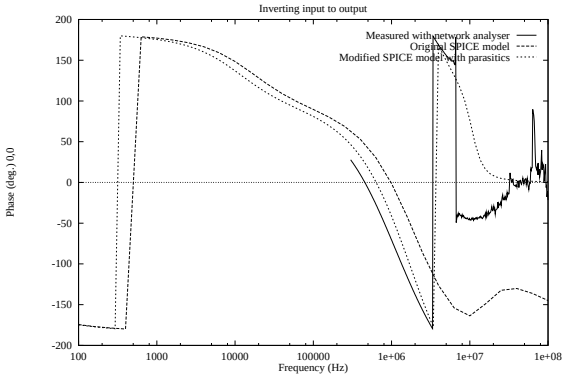

Figure 9: Phase response of op-amp circuit – computed (full circuit models) and measured.

The measured and computed (SPICE full circuit model) frequency and phase responses of the op-amp, inverting input (non-inverting open circuit) are shown in Figures 8 and 9. It can be seen that the measured and computed responses begin to diverge at 1 MHz. The addition of the parasitic capacitances around the circuit improves matters to some extent but there is still a significant difference between computed and measured curves. The parasitic capacitances of each track to ground (2 pF approx.) affect the frequency response around 1 MHz whilst a very small coupling capacitance (0.01 pF) between input and output connections causes the leveling of the frequency response above 10 MHz.

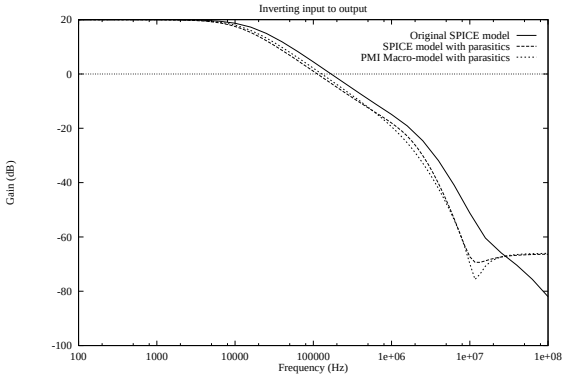

Figure 10: Comparing the amplitude response of the PMU Macro–model with the full (SPICE) circuit models.

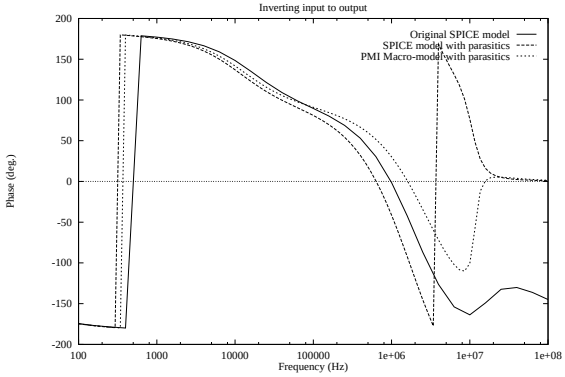

Figure 11: Comparing the phase response of the PMI Macro–model with the full circuit models.

Figures 10 and 11 show the frequency and phase response of the full circuit (SPICE) model and the PMI macro–model design for inverting input to output. Figures 12, and 13 show the frequency and phase response between Vdd and output for the full circuit (SPICE) model and the PMI macro–model; the macro–model response is shown with, and without the EMI coupling circuit added. The EMI effects in the model result in a response that closely matches that of the full circuit (SPICE) model at frequencies below about 30 MHz. It can be seen that the basic PMI macro model shows significant power supply to output coupling and that this still dominates the overall coupling above 10 MHz.

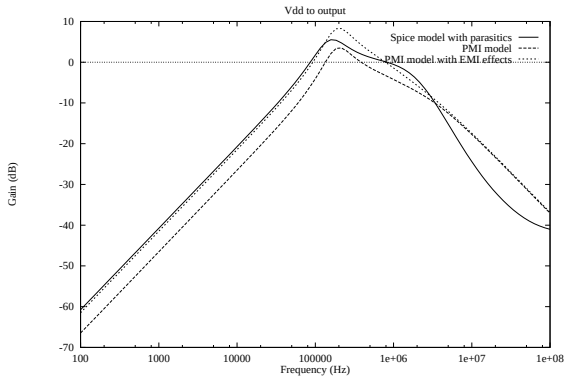

Figure 12: Comparing amplitude response Macro–models with the full circuit models.

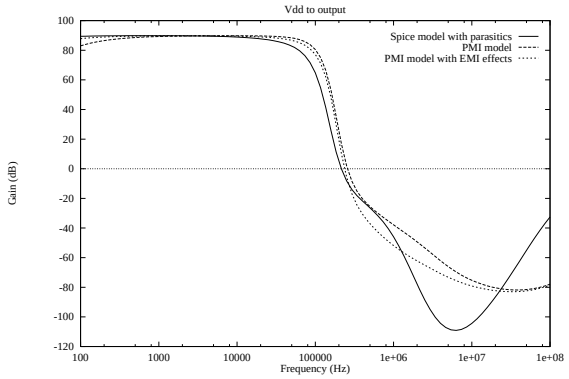

Figure 13: Comparing the phase response of the Macro–models with the full circuit models.

V.2 Time response

In order to observe the demodulation effects a short burst of 1 MHz sine–wave was injected into the Vdd rail and the output observed. Figure 14 shows the response of the full circuit SPICE model, and 15 shows the response of the EMI enhanced PMI macro-model. It can be seen that the major effect is carrier feedthrough. A small low–frequency disturbance can be seen near the start of each burst. This is due in part to the non-linearity in the path from Vdd to the output and partly to the non–linear response of the the input circuit to energy from the pulse coupled via other circuit elements (the separate effects can be observed if parts of the PMI model are selectively disabled). The PMI model was tuned to match the full–circuit SPICE model, however when measurements were carried out the real circuit showed a smaller carrier feedthrough and a larger non–linear effect (Figure 16). The PMI macro model can easily modified to follow this as is shown in Figure 17.

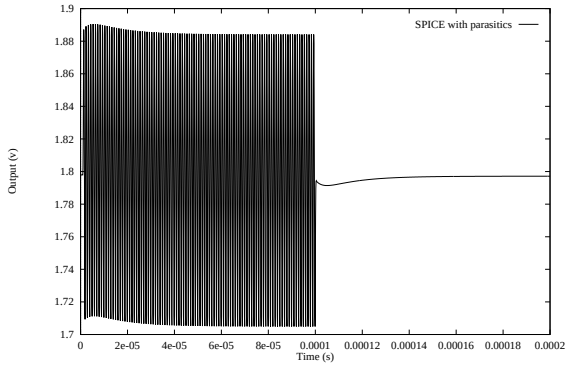

Figure 14: Amplitude response of the full circuit model with 0.2 V_{pp} 1 MHz tone burst on Vdd rail.

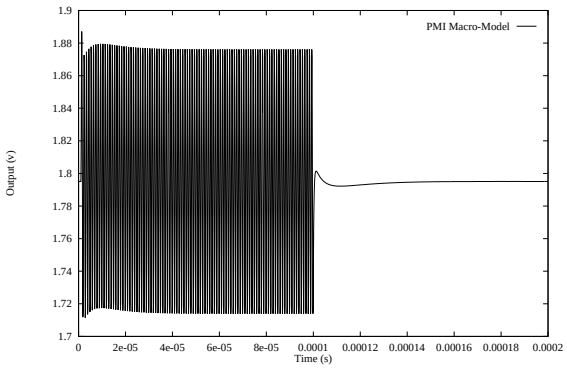

Figure 15: Amplitude response of the PMI Macro–models with 0.2 V_{pp} 1 MHz tone burst on Vdd rail.

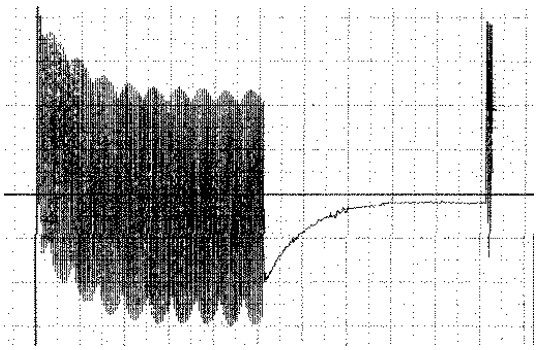

Figure 16: Measured response of op-amp circuit to 0.2 V_{pp} 1 MHz tone burst on Vdd rail (scale: 20 μ s, 20 mV per div).

VI Conclusions

The paper has suggested some ideas for further developing EMI macro–models for operational amplifier circuits. It is important that all terminals are considered if the effect of EMI on electronic circuits is to be modelled. The ingress of EMI via the power rails (and other terminals) is a topic which must be addressed if susceptibility modelling of circuits is to be possible.

The particular macro–models suggested are intended to demonstrate some possibilities. Further work must be carried out to optimise the models and determine the degree of accuracy required.

The work presented has shown results for small signal coupling, and non-linear effects in limited circumstances. If EMI macro–models are to be used effectively further work must be carried out to determine the measurements required to develop an adequate model.

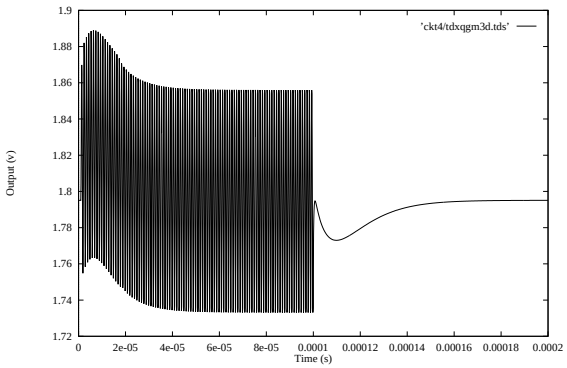

Figure 17: Amplitude response of the PMI Macro–model with 0.2 V_{pp} 1 MHz tone burst on Vdd rail: tuned to measured response.

VII Acknowledgements

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