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Si-Ge-Sn heterostructures: growth and applications

D. Buca[1*], S. Wirths[1], D. Stange[1], A.T. Tiedemann[1], G. Mussler[1],
Z. Ikonic[2], S. Chiussi[3], J.M. Hartmann[4], D. Grützmacher[1] and S. Mantl[1]

[1]Peter Grünberg Institute 9 and JARA - FIT, Forschungszentrum Juelich, 52425 Juelich, Germany
[2]Institute of Microwaves and Photonics, University of Leeds, LS2 9JT, United Kingdom
[3]Dpto. Física Aplicada, Univ. de Vigo, Rua Maxwell s/n, Campus Universitario, 36310 Vigo, Spain
[4]CEA, LETI, MINATEC Campus, 17 rue des Martyrs, 38054 Grenoble, France

*Tel: +49-2461-61-3663, E-mail: d.m.buca@fz-juelich.de

1. Introduction

It is now beyond controversy that one of the major issues of future information processing systems is power consumption. Hence, the integration of Si based photonics and CMOS electronics on a common platform is the key for efficient data processing. The novel group IV alloys Si-Ge-Sn are emerging as an ideal platform to combine both electronic and photonic operations on conventional Si platform.

Recently, binary GeSn alloys attracted strong research interest due to their "directness" given by the low energy difference between the Γ and L valleys, thus offering new possibilities of strain engineering [1]. Moreover, low bandgaps and lower effective carrier masses as compared to Si(Ge) these alloys will provide nanoelectronic device performance boost/improvements. The incorporation of Sn and tensile strain strongly decreases the carrier effective mass leading to higher carrier mobility [2]. In addition, the small bandgap around 0.5eV will enhance the tunneling probability and thus the on-currents of Tunnel-FETs, a novel class of ultralow power devices [3, 4]. However, the introduction of these new materials in electronics requires research on device design and process module developments.

In this contribution, we will first present band structure engineering based on high Sn-content (Si)GeSn buffers towards tensile strained Ge and GeSn layers. Then the use of this structure for FET applications including gate stack formation on strained GeSn and SiGeSn will be addressed.

2. Experimental

Several groups have succeeded in synthesizing (Si)GeSn alloys applying different growth techniques like APCVD [5], UHVCVD [6,7], or MBE [7]. Our approach is based upon Reduced Pressure CVD [8] with showerhead technology using $SnCl_4$, Ge_2H_6 and Si_2H_6 precursors appropriate for growth temperatures between 350°C and 475°C. Here, we focus first on the achievement of direct bandgap group IV semiconductors by strain-engineering of (Si)GeSn alloys and Ge. Then insights into two MOSFET process modules, namely high-k/metal gate stacks and Ni based contact on GeSn with Sn contents up to 12 % are presented.

3. Results and discussion

Our theoretical calculations claim that cubic GeSn with a Sn content of about 8-9% is a direct gap semiconductor. Growth studies indicated that GeSn layer does not fully relax and thus the residual compressive strain prohibits a perfect cubic lattice. However such layers are ideal buffer layers for straining Ge and GeSn alloys. Theoretical electronic band calculations show that indirect semiconductors as GeSn and Ge can be strain tailored to become direct bandgap semiconductors [1]. Figure 1 shows that a low tensile strain of 0.4 % is sufficient to obtain a fundamental direct bandgap in $Ge_{0.94}Sn_{0.06}$.

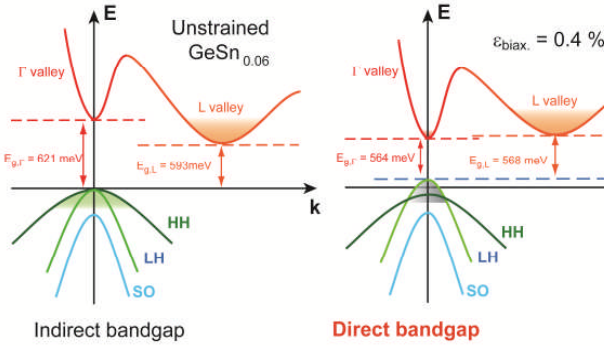

Fig. 1: Calculated band structures indicating that a low tensile strain induces a transition from indirect to direct for $Ge_{0.94}Sn_{0.06}$ alloys.

The growth of a 30 nm tensile strained $Ge_{0.94}Sn_{0.06}$ layer was realized on a 250 nm thick $Ge_{0.89}Sn_{0.11}$ buffer layer. The reciprocal space map (RSM) in Fig. 2 (left) reveals the in-plane and out-of-plane lattice constants of the grown layer in the heterostructure. By means of bowing corrected Vegard's law the biaxial tensile strain within the overgrown GeSn layer have been determined to about 0.4 %. According to the aforementioned band structure calculations this material exhibits a direct bandgap. On the right in Fig. 2a transmission electron micrograph (TEM) shows a processed sGeSn/sGe/GeSn/Ge-VS MOS capacitor (MOScap) confirming the single crystalline quality of the layer stack with sharp interfaces and a smooth surface.

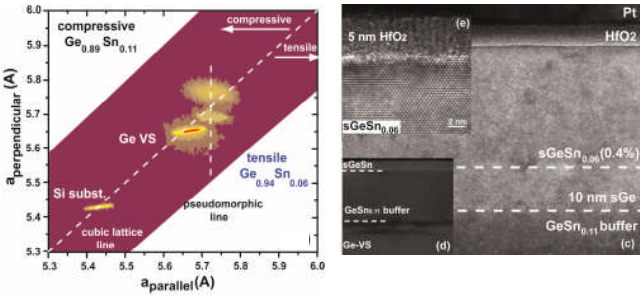

Fig. 2: (left) RSM spectra of 250 nm $Ge_{0.89}Sn_{0.11}$ buffer overgrown with 10 nm Ge and 30 nm tensile strained $Ge_{0.94}Sn_{0.06}$ (right) HRTEM image of the same structure with 5 nm HfO_2 gate oxide.

An important step toward nanoelectronic integration is the gate formation on GeSn alloys. For such studies HF:HCl pre-cleaned samples were loaded into an ALD reactor where the Al2O3 and/or HfO_2 deposition of 5 nm followed an *in-situ* O_3 oxidation step. The interface of the strained GeSn and the 5 nm HfO_2 dielectric with a thin interfacial layer of about 0.8 nm is underlined in the high resolution TEM inset in Fig 2b.

On the other hand, using similar processing as developed for NW fabrication on SOI/GOI substrates, free standing tensile strained GeSn NW MOSFETs can be fabricated. Moreover, by applying a novel "bridge technology" [9, 10] highly strained GeSn NWs can be achieved with potential for both, optic and electronic devices.

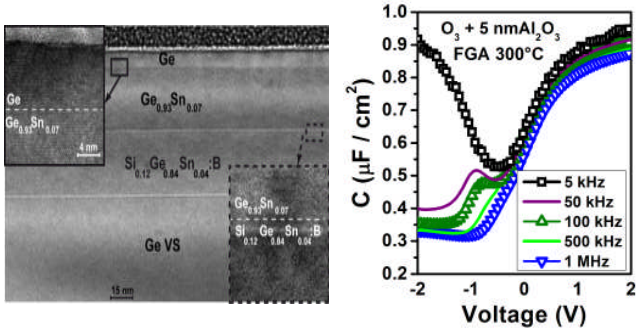

Fig. 3: (left) TEM image of a 4 nm Ge/30 nm $Ge_{0.93}Sn_{0.07}$/ $Si_{0.12}Ge_{0.84}Sn_{0.04}$/Ge-VS; (b) CV characteristics of MOS capacitors formed on similar GeSn structure with 5 nm Al_2O_3 gate oxide.

An interesting approach for fabricating high mobility n-MOSFETs is shown in Fig. 3. The introduction of a in-situ doped SiGeSn layer has the advantage of channel-substrate isolation via band offset and counter doping. The multi frequency capacitance-voltage (CV) response of a n-MOS capacitance formed on a similar p-MOSFET heterostructure with 5 nm Al_2O_3 gate oxide is shown on the right in Fig. 3. Due to the smaller bandgap of the GeSn a stronger inversion response compared to Ge MOScaps at low frequencies is obtained. For compressively strained GeSn channel MOSFETs, Ge can be used as capping, similar to Si caps on SiGe quantum-well (QW) MOSFETs to reduce the surface scattering effects which reduce the device performance significantly. However, for relaxed GeSn layers with large Sn contents the Ge cap will be under high tensile strain which will result in a similar gap as the GeSn channel. SiGeSn will maintain a large, beneficial offset to the relaxed GeSn due to the incorporated Si. Figure 4 shows CV characteristics of Ge and $Si_{0.12}Ge_{0.84}Sn_{0.04}$ MOS structures processed under identical conditions. Both layers have a similar bandgap which results in a similar frequency behavior.

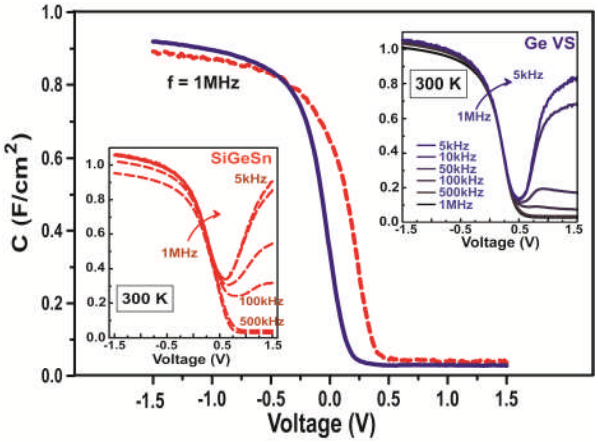

Fig. 4: Comparison of CV characteristics for MOS capacitors formed on Ge and $Si_{0.12}Ge_{0.84}Sn_{0.04}$ layers with 5 nm Al_2O_3 gate oxide.

In addition to CMOS, SiGeSn ternary alloys are proposed as cladding layer for GeSn QW laser offering the possibility to tune the bands offset via the Si/Sn ratio [11].

4. Conclusions

This new class of group IV semiconductors, i.e. GeSn and SiGeSn, will enable novel integrated photonic and electronic devices due to the direct gap, the feasibility to tune the gap energies and the band alignments. Remarkable progress has been achieved in the growth of high quality heterostructures, high-k gate stacks and metal contact formation required for future nanodevices.

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