Article:
Rooney, J.P., Parry, R., Hunter, I. et al. (1 more author) (2002) A filter synthesis technique applied to the design of multistage broad-band microwave amplifiers. IEEE Transactions on Microwave Theory and Techniques, 50 (12). pp. 2947-2953. ISSN 0018-9480

https://doi.org/10.1109/TMTT.2002.805156

A Filter Synthesis Technique Applied to the Design of Multistage Broad-Band Microwave Amplifiers

John-Paul Rooney, *Student Member, IEEE*, Richard Parry, *Senior Member, IEEE*, Ian Hunter, *Senior Member, IEEE*, and Roger D. Pollard, *Fellow, IEEE*

***Abstract*—A method for designing multistage broad-band amplifiers based upon well-known filter synthesis techniques is presented. Common all-pole low-pass approximations are used to synthesize prototype amplifier circuits that may be scaled in frequency and impedance. All-pass filters introduced at the first stage are shown to improve input match while maintaining circuit performance less 6 dB gain. A theoretical comparison is made with the distributed amplifier and the cascaded single-stage distributed amplifier. Theoretically, a larger gain-bandwidth product is achieved using the synthesis technique. A proof-of-concept Butterworth low-pass two-stage amplifier was designed, simulated, and measured and achieved a flat gain performance of 1–4 GHz with a power gain of 14.5±1 dB close to the predicted 1–4.2 GHz, 15±1 dB.**

***Index Terms*—Active filters, all-pass circuits, broad-band amplifiers, Butterworth filters, microwave circuits, microwave FET amplifiers.**

I. Introduction

THE distributed amplifier (DA) has been firmly established for the past two decades in the design of amplifiers spanning multioctave bandwidths [1], [2]. The advantages of this type of amplifier are flat gain, flat group delay, low noise figure, and low voltage standing-wave ratio (VSWR) performance over broad bandwidths. The key applications are electronic warfare (EW) and digital optical communications.

The main disadvantage of the DA is the high number of active devices required per unit gain. The cascaded single-stage distributed amplifier (CSSDA) matches the bandwidth of the DA, but by cascading single stages, increases the gain significantly [3]–[8]. This technique relies upon computer optimization to meet the final design specification, but this nonscientific method is costly in terms of design hours.

This paper proposes a new method of multistage broad-band amplifier design utilizing normalized low-pass prototypes. The advantages of using prototype circuits in amplifier design are commensurate with filter design. Solutions valid for fixed topologies are given for normalized frequency and characteristic impedance and, therefore, a significant proportion of the total design time is invested in developing the prototype; there is no need for amplifier designers to duplicate this effort. The prototype is simply scaled in frequency and impedance to suit a particular application. It is also possible, and useful, to discuss the performance of varying topologies in an environment that allows comparisons to be generally applicable regardless of the final application and components used, especially the active device.

The amplifier response can be fully specified using Butterworth, Chebyshev, Bessel, or other all-pole approximations to the ideal low-pass response.

Manuscript received April 5, 2002; revised August 15, 2002. This work was supported by Filtronic plc.

J.-P. Rooney, I. Hunter, and R. D. Pollard are with the Institute of Microwaves and Photonics, School of Electronic and Electrical Engineering, The University of Leeds, Leeds LS2 9JT, U.K. (e-mail: johnpaul@ieee.org).

R. Parry is with the Institute of Microwaves and Photonics, School of Electronic and Electrical Engineering, The University of Leeds, Leeds LS2 9JT, U.K. and also with Filtronic plc, West Yorkshire BD18 3TT, U.K.

Digital Object Identifier 10.1109/TMTT.2002.805156

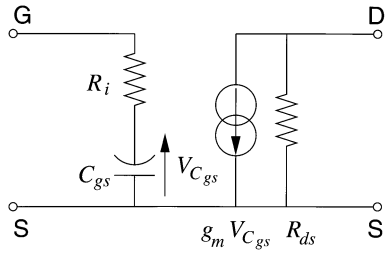

Fig. 1. Four-element MESFET ECM.

II. Prototype Analysis

A. Single-Stage Prototype

The schematic of a simple four-element equivalent-circuit model (ECM) for a GaAs MESFET is shown in Fig. 1. The transfer function in terms of the S-parameters is given when source and load are terminated in Z_0

$$S_{21}(p) = \frac{-2g_m R_T}{1 + pC_{\rm gs}R_s} \tag{1}$$

where $R_s = Z_0 + R_i$, $R_T = R_{\rm ds}Z_0/(R_{\rm ds} + Z_0)$, and the 3-dB cutoff frequency for the MESFET is, therefore,

$$\omega_{3\,\rm dB} = \frac{1}{C_{\rm gs}R_s}\ \text{rad/s}. \tag{2}$$

It is well known that the bandwidth may be extended and the gain flattened by adding a series inductor to the gate of the MESFET (Fig. 1), creating the single-stage prototype amplifier. The transfer function becomes second order with two complex conjugate transmission poles, i.e.,

$$S_{21}(p) = \frac{-2g_m R_T}{1 + pCR_s + p^2LC}. \tag{3}$$

The nomenclature has been altered, i.e., $C_{\rm gs}$ is referred to as C in (3), to save confusion between prototype amplifiers and

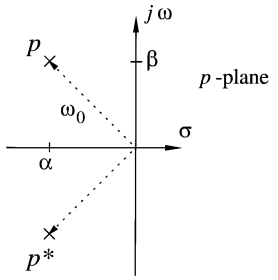

Fig. 2. Pole zero plot in the complex frequency plane for a second-order transfer function.

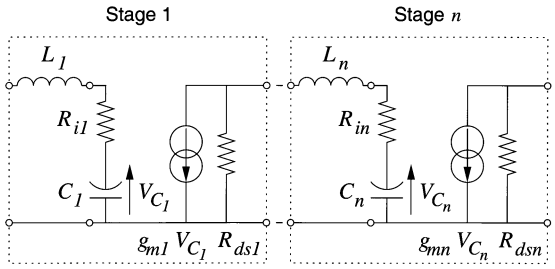

Fig. 3. Schematic of an n-stage prototype amplifier showing matching inductors L_i.

MESFET ECMs. The transmission-pole locations, as illustrated in Fig. 2, may be solved, where $p = -\alpha \pm j\beta$

$$\alpha = \frac{R_s}{2L} \tag{4}$$

$$\beta = \sqrt{\frac{1}{LC} - \left(\frac{R_s}{2L}\right)^2} \tag{5}$$

$$\omega_0 = \frac{1}{\sqrt{LC}}. \tag{6}$$

A Butterworth, Chebyshev, or other all-pole approximation to the ideal low-pass response may be synthesized from this second-order prototype amplifier. There are well-known general methods of synthesizing singly terminated networks to produce a given transfer function [9], [10]. The following considers second-order transfer functions only.

Solving (4) and (6) for L and C, respectively, yields the prototype circuit element values required for the chosen approximation

$$L = \frac{R_s}{2\alpha}\ \text{H} \tag{7}$$

$$C = \frac{2\alpha}{\omega_0^2 R_s}\ \text{F}. \tag{8}$$

The normalized cutoff frequency is then defined as the ratio of prototype to MESFET ECM gate–source capacitance *viz*.

$$\omega_c = \frac{C}{Z_0 C_{\text{gs}}} \tag{9}$$

with Z_0, which, in this case, is a necessary dimensionless scaling factor. Equation (9) ensures that when the prototype is scaled in frequency and impedance, the resulting scaled prototype may be realized using the chosen MESFET.

The sensitivity of the prototype response to component variations is fairly low. For example, a 10% variation in the value of R_i results in bandwidth shrinkage of approximately 1% if the amplifier is redesigned to account for this change. If the amplifier is not redesigned, then changes of $R_i < 10\%$ result in negligible deviations from the ideal response. The same may be said for L and C.

B. n-Stage Prototype

The n-stage prototype schematic is detailed in Fig. 3. A general transfer function was derived as follows:

$$S_{21}(p) = \frac{2(-1)^n R_T \prod_{i=1}^{n} g_{mi}}{\mathcal{F}_1(p) \prod_{i=2}^{n} \mathcal{F}_i(p)} \tag{10}$$

where

$$\mathcal{F}_1(p) = 1 + pC_1R_{s1} + p^2C_1L_1 \tag{11}$$

$$\mathcal{F}_i(p) = G_{\text{ds(i-1)}}\left(1 + pC_iR_{si} + p^2C_iL_i\right) \tag{12}$$

where $R_{si} = R_{\text{ds}i} + R_{ii}$ for $i = 2$ to n. $R_{s1} = Z_0 + R_{i1}$.

The denominator of the general transfer function in (10) contains n quadratic factors representing, in turn, the frequency response of each ith FET and matching inductor L_i. Each stage, therefore, contributes a pair of complex conjugate poles, whose positions are determined by the value of the circuit elements C_i, L_i and the source impedance R_{si}. This is possible as the FET model used is unilateral, i.e., there is no interaction between stages and isolated pole pairs may exist. One may, therefore, synthesize an n-stage prototype amplifier to exhibit a prescribed all-pole transfer function, firstly by isolating each complex conjugate transmission-pole pair of the prescribed transfer function, and then by administering individually their production to separate amplifier stages, as described in Section II-A. The overall desired response will be synthesized.

An n-stage amplifier contributes n pairs of complex conjugate transmission poles. For example, a two-stage design has two possible realizations, one of which results in a larger bandwidth due to the larger value of C_1 required [from (9)], but reduced gain if identical FETs are used due to the smaller value of C_2 required. In general, for n-stages, there are $(n-1)n$ permutations of which n provide unique gain-bandwidth variations. The order of a realizable approximation is $2n$, thus, for two stages, a fourth-order all-pole approximation is realizable.

For the case where $Z_0 = R_{\text{ds}i} = 1\ \Omega$, and $R_{ii} = 0\ \Omega$, pole positions and prototype element values are given (Table I) for a Butterworth amplifier. Sample permutations that provide unique gain-bandwidth solutions to the designer are tabulated. The prototype amplifier may be modified for the case where $R_{ii} \neq 0\ \Omega$ for $i = 1$ to n as follows:

$$L_i \Rightarrow L_iR_{s1} \tag{13}$$

$$C_i \Rightarrow \frac{C_i}{R_{s1}}. \tag{14}$$

TABLE I
POLE POSITIONS AND PROTOTYPE ELEMENT VALUES FOR BUTTERWORTH MULTISTAGE AMPLIFIERS ($Z_0 = R_{dsi} = 1\ \Omega$, $R_{ii} = 0\ \Omega$, AND $C_1 \neq C_i$)

Stages	Pole locations		Stage	Element Values	
(n)	α	β	(i)	C_i [F]	L_i [H]
1	-0.707	±0.707	1	1.414	0.707
2	-0.383	±0.924	1	0.765	1.307
			2	1.848	0.541
	-0.924	±0.383	1	1.848	0.541
			2	0.765	1.307
3	-0.259	±0.966	1	0.518	1.932
			2	1.414	0.707
			3	1.932	0.518
	-0.707	±0.707	1	1.414	0.707
			2	1.932	0.518
			3	0.518	1.932
	-0.966	±0.259	1	1.932	0.518
			2	0.518	1.932
			3	1.414	0.707
4	-0.195	±0.981	1	0.39	2.563
			2	1.111	0.9
			3	1.663	0.6
			4	1.962	0.51
	-0.556	±0.832	1	1.111	0.9
			2	1.663	0.6
			3	1.962	0.51
			4	0.39	2.563
	-0.832	±0.556	1	1.663	0.6
			2	1.962	0.51
			3	0.39	2.653
			4	1.111	0.9
	-0.981	±0.195	1	1.962	0.51
			2	0.39	2.653
			3	1.111	0.9
			4	1.663	0.6

TABLE II
ECM ELEMENT VALUES FOR A NORMALIZED FET ECM

Circuit element	Value
R_i	0 Ω
C_{gs}	1 F
g_m	1, 1.5 and 2 S
R_{ds}	1 Ω

III. PROTOTYPE PERFORMANCE COMPARISON

The gain-bandwidth product (GBP) is calculated for a restricted case of prototype amplifier where identical FETs are used to realize the design. An FET ECM is employed with element values (Table II) chosen to allow for simple comparisons between different amplifier topologies.

The FET ECM value of $C_{\rm gs}$ is fixed by the device and requires the gate–source capacitance of each prototype ith stage (Fig. 4) to be identical. To preserve the desired response, the total capacitance of the ith stage, i.e., C_{Ti}, must be made equal to the scaled prototype value C_i', where

$$C_i' = \frac{C_i}{Z_0 \omega_c} \tag{15}$$

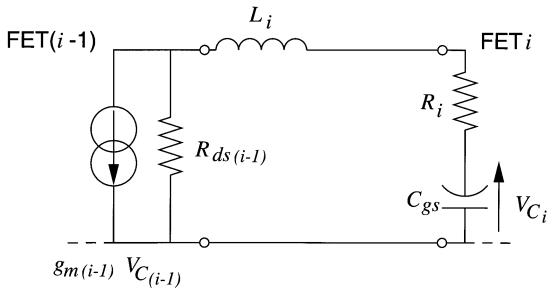

Fig. 4. Schematic of an ith stage with C_i fixed by $C_{\rm gs}$.

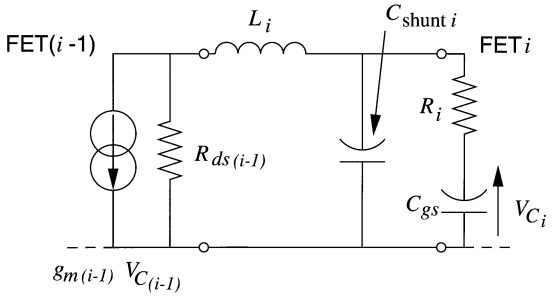

Fig. 5. Shunt capacitance employed to increase C_{Ti} to C_i'.

and substituting $\omega_{3\,\rm dB}$ from (9)

$$C_{Ti} = C_i' = \frac{C_i C_{\rm gs}}{C_1}. \tag{16}$$

To illustrate, a two-stage Butterworth prototype is developed (Table I). Three methods of realizing the restricted case prototype amplifier are discussed.

A. Using Shunt Capacitance

When $C_{Ti} > C_{\rm gs}$, i.e., $C_i > C_1$, shunt capacitance may be used to increase C_{Ti} (Fig. 5). The voltage across $C_{\rm gs}$ now behaves as though $C_{\rm gs} = C_{T2}$ under the condition $R_i = 0$, and the overall desired response is regained. In this case, the bandwidth, gain, and GBP are given as follows:

$$\omega_c = 0.765 \tag{17}$$

$$|S_{21}(0)| = 1 \tag{18}$$

$$\text{GBP} = 0.765. \tag{19}$$

B. Using Series Capacitance

When $C_{Ti} < C_{\rm gs}$, i.e., $C_i < C_1$, series capacitance may be used to lower C_{Ti} (Fig. 6). V_{C_2} is reduced and, thus, so is the overall gain of the amplifier. The bandwidth is proportionally larger, however, due to the larger value of C_1 and, therefore, the GBP remains constant as follows:

$$\omega_c = 1.848 \tag{20}$$

$$|S_{21}(0)| = 0.765/1.848 \tag{21}$$

$$\text{GBP} = 0.765. \tag{22}$$

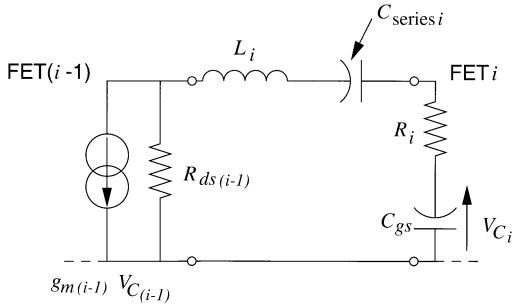

Fig. 6. Series capacitance employed to reduce C_{Ti} to C_i'.

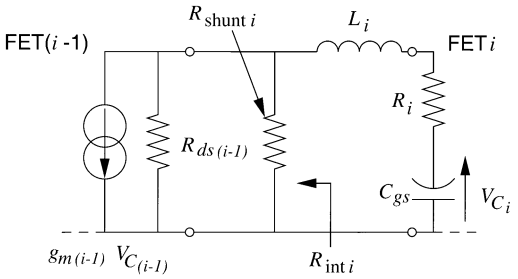

Fig. 7. Shunt resistance employed to modify C_{Ti} to C_i'.

C. Using Shunt Resistance

Another method is to use $R_{\text{ds}(i-1)}$ to scale the element values of stage i. For $C_{\text{gs}i} = C_{\text{gs1}}$

$$R_{\text{int}i} = \frac{\alpha_i \omega_{o1}^2}{\alpha_1 \omega_{oi}^2} R_s \tag{23}$$

where $R_{\text{int}i}$ is the source resistance seen by the ith stage looking back toward stage $i-1$ (Fig. 7). This method may be applied to both cases detailed in Sections III-A and III-B.

Examining the Butterworth example, where $C_2 > C_{\text{gs}}$ ($R_{\text{int}2} = 1.848/0.765$, BW $= 0.765$) and $C_2 < C_{\text{gs}}$ ($R_{\text{int}2} = 0.765/1.848$, $BW = 1.848$), it may be noted that the GBP remains constant at 0.765 for this case. $R_{\text{int}2} = 1.848/0.765$ cannot be realized as $R_{\text{ds}} = 1$ and, thus, series capacitance must be employed, reducing the gain to unity. This will not be the case for practical FETs, where $R_{\text{ds}} > 1$, but is useful, as this proves that the GBP remains constant for all three topologies detailed previously, assuming that identical FETs are employed.

The bandwidth and GBP for Butterworth amplifiers up to four stages are given in Table III.

IV. All-Pass Matching

The authors have found that an all-pass network may be used to improve the input match of the amplifier, as shown in Fig. 8. A 6-dB loss of power results as V_{C_1} is halved. Even- and odd-mode analysis was used to find the all-pass circuit element values for the matched condition $R_m = 1/R_i\ \Omega$, $C_m = (C_1/4) + L_1$ F, and $L_m = C_1/2$ H. Note that the values of C_1 and L_1 used are dimensionless. The transfer function of the first stage is straightforward to derive, and is given as follows:

$$\frac{V_{C_1}(p)}{V_i(p)} = \frac{1}{2 + pC_1(1+2R_i) + p^2 C_1(L_m + 2L_1)}. \tag{24}$$

TABLE III
Normalized Performance Indicators for Butterworth Multistage Amplifiers

Stages		GBP		
n	BW	$g_m = 1$	$g_m = 1.5$	$g_m = 2$
1	1.41	1.41	2.12	2.82
2	0.77	0.77	1.73	3.08
	1.85	0.77	1.73	3.08
3	0.52	0.52	1.76	4.16
	1.41	0.52	1.76	4.16
	1.93	0.38	1.28	3.04
4	0.39	0.39	1.98	6.24
	1.11	0.39	1.98	6.24
	1.66	0.26	1.32	4.16
	1.96	0.19	0.96	3.04

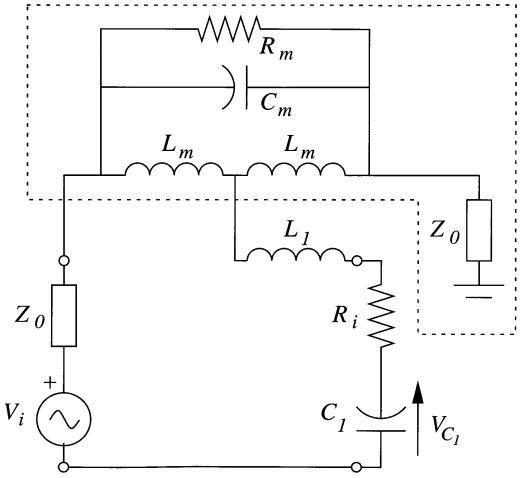

Fig. 8. Schematic of an all-pass network used to improve input match.

If the transmission poles of this second-order transfer function are located in a similar position in the p-plane to those required in Section II, then the overall desired response can be maintained, albeit with less gain and more bandwidth. The degree of freedom necessary to maneuver the poles to the required position is provided by the element L_1. A two-stage Butterworth prototype amplifier illustrates this. Table I yields the prototype element values with $R_i = 0\ \Omega$: $C_1 = 0.765$ F and $L_1 = 1.307$ H. In the matched case, $L_1 = 0.8$ H gives the flattest response, as shown in Fig. 9. Note that the prototype amplifier is normalized for unit gain. In practice, the prototype will exhibit more than unity power gain, and the matched amplifier will exhibit 6 dB less.

V. Comparison With CSSDA

The equations describing dc forward available gain, i.e., G_{av}, for each using ideal lossless n-stage devices are given in Table IV [8]–[12]. In order for the CSSDA to achieve higher gains than the DA, the following inequality [8]:

$$Z_{\text{int}} \geq \frac{\sqrt[n]{n}-1}{g_m} \tag{25}$$

must be satisfied. It has been demonstrated that the CSSDA provides more gain per device than the DA [3]. The synthesis method realizes 12 dB more gain than the CSSDA for identical

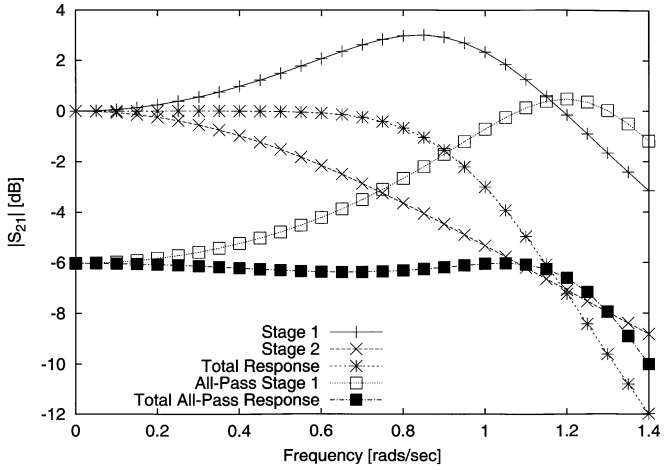

Fig. 9. Two-stage prototype Butterworth amplifier comparison of the matched versus unmatched gain response.

TABLE IV
COMPARISON OF FORWARD AVAILABLE GAIN ($G_{\rm av}$) FOR THREE AMPLIFIER TYPES

Amplifier Type	Available Gain, G_{av}
DA [11]	$\frac{n^2 g_m^2 Z_L Z_S}{4}$
CSSDA [8]	$\frac{g_m^{2n} Z_{\rm int}^{2(n-1)} Z_L Z_S}{4}$
n-stage low-pass [12]	$4 g_m^{2n} Z_L Z_S \prod_{i=1}^{n-1} R_{{\rm int}i}^2$

interstage impedances due to input and output matching. Input and output match can also be achieved in the synthesis design at a total cost of 12-dB gain. Input match has been demonstrated in principle using an all-pass filter in Section IV. The GBPs of the two amplifiers are now compared, accounting for the loss in gain due to matching. The radian cutoff frequency of the CSSDA is given by [6]

$$\omega_c = \frac{2}{C_{\rm gs} R_s} \tag{26}$$

and, therefore, the GBP product for the CSSDA is

$$\mathrm{GBP}_{\rm CSSDA} = \frac{g_m^{2n} Z_{\rm int}^{2(n-1)} Z_L Z_S}{2 C_{\rm gs} R_s} \tag{27}$$

and for the synthesis method from (9) and Table IV, the GBP product is

$$\mathrm{GBP}_{\rm synthesis} = \frac{8\alpha_1 g_m^{2n} Z_L Z_S \prod_{i=1}^{n-1} R_{{\rm int}i}^2}{\omega_0^2 C_{\rm gs} R_s}. \tag{28}$$

Comparing (27) and (28) and allowing for 12 dB more gain from the unmatched synthesized amplifier demonstrates that, for the CSSDA to have a larger GBP product than the synthesis amplifier, the following must hold:

$$Z_{\rm int} \geq \left(\frac{\alpha_1}{\omega_{o1}^2} \prod_{i=1}^{n-1} R_{{\rm int}i}^2 \right)^{1/(2(n-1))}. \tag{29}$$

TABLE V
MINIMUM $Z_{\rm int}$ REQUIRED FOR CSSDA TO MATCH GBP PRODUCT OF SYNTHESIS METHOD

	Z_{int}	
Stages	Butterworth	Chebyshev
2	$\geq 74.7\ \Omega$	$\geq 160.29\ \Omega$
3	$\geq 113\ \Omega$	$\geq 300.2\ \Omega$
4	$\geq 149.9\ \Omega$	$\geq 432\ \Omega$

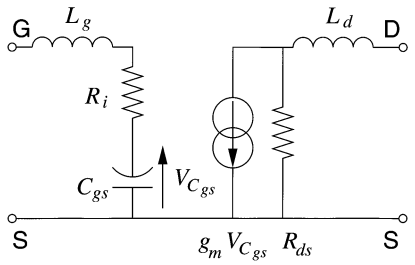

Fig. 10. Unilateral ECM used in the synthesis of a two-stage amplifier with gate and drain parasitic inductance.

TABLE VI
CIRCUIT ELEMENT VALUES FOR THE NE71083. $V_{\rm ds} = 3$ V, $I_{\rm ds} = 10$ mA

Circuit element	Value	
L_g	0.4	nH
R_i	7	Ω
C_{gs}	0.5	pF
g_m	43	mS
R_{ds}	250	Ω
L_d	0.3	nH

Table V indicates the GBP advantage of the synthesis amplifier when compared to the CSSDA and, therefore, the conventional distributed amplifier (CDA). The results are for Butterworth and Chebyshev amplifiers designed for a maximum GBP product. In practice, when $R_{\rm ds} \neq \infty$, some prototype amplifiers above two stages cannot be realized using shunt resistance and series capacitance must be used, reducing gain and limiting the GBP, as discussed in Section III-C.

VI. DESIGN EXAMPLE

An NE71083 GaAs MESFET was used as the active device in a Butterworth two-stage amplifier design. The first stage in the design is to characterize the MESFET using a very simple ECM. This can be determined from manufacturers or measured S-parameters of the device using well-known techniques [13], [14]. The ECM used is shown in Fig. 10 and the circuit element values are given in Table VI.

The prototype circuit is then determined using (7), (8), (23), and Table I ($R_{s1} = Z_0 + R_i$, $R_{si} = R_{{\rm int}i} + R_i$). The cutoff frequency is determined from (9), $f_{3\,\rm dB} = 4.27$ GHz, and the circuit elements are scaled in frequency and impedance. Table VII tabulates the prototype and scaled circuit element values.

The dc gain is given by (10), $|S_{21}(0)|_{\rm dB} = 26$ dB. In practice, parasitic elements and feedback will degrade the optimum performance.

TABLE VII
PROTOTYPE AND SCALED CIRCUIT ELEMENT VALUES FOR A BUTTERWORTH TWO-STAGE AMPLIFIER

Element	Prototype	Scaled
L_{g1}	1.489 H	2.77 nH
C_{gs1}	0.671 F	0.50 pF
L_{g2}	1.489 H	2.77 nH
C_{gs2}	0.671 F	0.50 pF
R_{ds1}	2.612 Ω	130.61 Ω

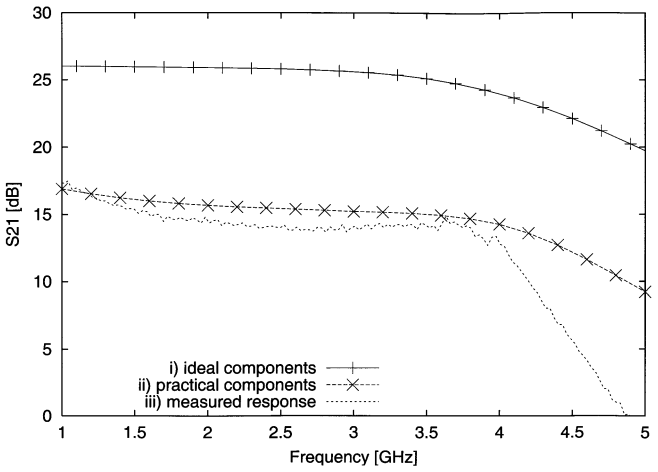

Fig. 11. Two-stage Butterworth amplifier using the NE71083 MESFET. Simulated responses using: i) ideal components and ii) practical components versus iii) measured response.

VII. SIMULATION RESULTS

The simple unilateral ECM, shown in Fig. 10, was used as the active device in an ideal simulation along with lumped matching components. This was then compared to the same design using measured FET S-parameters ($I_{\rm ds} = 10$ mA, $V_{\rm ds} = 3$ V) and nonideal matching components.

The measured FET exhibited series feedback inductance ($L_s = 0.3$ nH) when compared to the manufacturer's S-parameter data, as a result of the fixture used in this particular amplifier design. This explains the variation between the simulated and measured data presented earlier [12].

The synthesis technique in the ideal case produces a fourth-order Butterworth response with a gain of 26 dB, as predicted and a $\rm BW_{3\,dB}$ of 4.27 GHz. The response is degraded from the ideal when measured S-parameters, nonideal circuit elements, and FET bias are included in the simulation (see Fig. 11). This is to be expected as parasitic and feedback elements were not accounted for in the synthesis procedure, and neither were the practical realization of matching inductors and shunt resistance. However, the response exhibits a gain of 15 ± 1 dB over a $\rm BW_{3\,dB}$ of 1–4.2 GHz.

VIII. MEASUREMENT RESULTS

The amplifier gain was measured as 14.5 ± 1 dB over a $\rm BW_{3\,dB}$ of 1–4.1 GHz (see Fig. 11). Good correlation between simulated and measured results is obtained. No tuning was necessary to achieve this response.

Gain $\geq$20 dB was measured at low frequencies; this is explained by dc blocking capacitors increasing $R_{\rm int}$ by removing the effect of $R_{\rm shunt}$. An alternative bias topology should allow for low-frequency operation.

IX. CONCLUSION

The theoretical development of a simple filter synthesis technique applied to the design of multistage broad-band amplifiers has been presented. Prototype circuits have been developed, allowing for the straightforward design of amplifiers exhibiting low-pass responses. It has been shown that the GBP for the prototype amplifier may improve upon that achieved using the CSSDA.

The technique can, in theory, be extended to any bandwidth and gain required by the designer, provided suitable MESFETs are available. The technique is particularly suited to monolithic-microwave integrated-circuit (MMIC) amplifier design where associated parasitic components are minimal, resulting in a closer correlation between predicted and measured results, and large bandwidths are theoretically achievable.

Any all-pole transfer function may be realized using this technique, making it particularly useful in realizing amplifiers for digital optical communications where flat group delay is desired. Input and output matching may also be improved by utilizing all-pass networks at the input and output, although 6-dB loss will occur for each.

This method has been proven correct through simulated and measured results of a proof-of-concept Butterworth two-stage amplifier.

REFERENCES

[1] J. B. Beyer, S. N. Prasad, R. C. Becker, J. E. Nordman, and G. K. Hohenwarter, "MESFET distributed amplifier design guidelines," *IEEE Trans. Microwave Theory Tech.*, vol. MTT-32, pp. 268–275, Mar. 1984.

[2] R. C. Becker and J. B. Beyer, "On gain-bandwidth product for distributed amplifiers," *IEEE Trans. Microwave Theory Tech.*, vol. MTT-34, pp. 736–738, June 1986.

[3] B. Y. Banyamin and M. Berwick, "Analysis of the performance of four-cascaded single-stage distributed amplifiers," *IEEE Trans. Microwave Theory Tech.*, vol. 48, pp. 2657–2663, Dec. 2000.

[4] B. Banyamin and M. Berwick, "The gain advantages of four cascaded single stage distributed amplifier configurations," in *IEEE MTT-S Int. Microwave Symp. Dig.*, 2000, pp. 1325–1328.

[5] B. Y. Banyamin, J. Y. Liang, C. S. Aitchison, and M. Berwick, "Low noise high-gain distributed preamplifiers using cascaded single stage distributed amplifier configurations," *IEICE Trans. Electron.*, vol. E82-C, no. 7, pp. 1039–1046, July 1999.

[6] B. Y. Banyamin, J. Y. Liang, and C. S. Aitchison, "A new high gain-broadband amplifier using cascaded single stage distributed amplifiers," in *Proc. Asia–Pacific Microwave Conf.*, vol. 2, 1998, pp. 753–756.

[7] J. Y. Liang and C. S. Aithison, "A proposal of a broadband high gain block using cascaded single-stage distributed amplifiers," in *High-Performance Electron Devices for Microwave and Optoelectron. Applicat. Workshop*, Nov. 1995, pp. 173–178.

[8] ——, "Gain performance of cascade of single stage distributed amplifiers," *Electron. Lett.*, vol. 31, no. 15, pp. 1260–1261, July 1995.

[9] W. Cauer, "The realization of impedances with prescribed frequency dependence," *Arch. Elecktr. Uebertrag.*, vol. 15, pp. 355–388, 1926.

[10] O. Brune, "Synthesis of a finite two-terminal network whose driving-point impedance is a prescribed function of frequency," *J. Math. Phys.*, vol. 10, pp. 191–325, 1931.

[11] C. S. Aitchison, "The intrinsic noise figure of the MESFET distributed amplifier," *IEEE Trans. Microwave Theory Tech.*, vol. MTT-33, pp. 460–466, June 1985.

[12] J.-P. Rooney, R. Parry, I. Hunter, and R. D. Pollard, "A filter synthesis technique applied to the design of multistage broadband microwave amplifiers," in *IEEE MTT-S Int. Microwave Symp. Dig.*, June 2002, pp. 1915–1918.

[13] M. Berroth and R. Bosch, "Broad-band determination of the FET small-signal equivalent circuit," *IEEE Trans. Microwave Theory Tech.*, vol. 38, pp. 891–895, 1990.
[14] G. Dambrine, A. Cappy, F. Heliodone, and E. Playez, "A new method for determining the FET small-signal equivalent circuit," *IEEE Trans. Microwave Theory Tech.*, vol. 36, pp. 1151–1159, July 1988.

John-Paul Rooney (S'98) was born in Glasgow, U.K., in 1975. He received the B.Eng. degree (with honors) in electronic and electrical engineering from The University of Leeds, Leeds, U.K., in 1998, and is currently working toward the Ph.D. degree at The University of Leeds.

His research is currently conducted in association with Filtronic plc, and is focused on the development of new techniques for the design of multistage broad-band microwave amplifiers. In particular, his research is concerned with applying filter synthesis techniques to realizing amplifiers with predetermined transfer function responses.

Richard Parry (S'82–M'83–SM'01) received the B.Sc. degree (with first-class honors) in electrical and electronic engineering and Ph.D. degree from The University of Leeds, Leeds, U.K., in 1979 and 1984, respectively.

In 1982, he joined Filtronic Components Ltd., Leeds, U.K., where he was involved with microwave filters and multiplexers. In 1983, he was with K. W. Engineering Inc., San Diego, CA, prior to returning to Filtronic in 1985, where he was responsible for developing extensive computer-aided design (CAD) software for the design, simulation, and optimization of microwave filters and multiplexers realized in SSS, waveguide and combline structures. He is currently the Technical Director of Filtronic Components Ltd., which is currently part of the Electronic Warfare Division, Filtronic plc, West Yorkshire, U.K. In 1997, he joined the Institute of Microwaves and Photonics, The University of Leeds, where he is currently a Part-Time Senior Research Fellow.

Dr. Parry is a Fellow of the Institution of Electrical Engineers (IEE), U.K.

Ian Hunter (M'82–SM'94) was born in Fleetwood, Lancashire, U.K., in 1957. He was educated at the Barrow-in-Furness Grammar School. He received the B.Sc. (first-class honors) and Ph.D. degrees from The University of Leeds, Leeds, U.K., in 1978 and 1981, both in electrical engineering.

Upon graduation, he was a Microwave Engineer involved with broad-band microwave components and subsystems for EW applications with Aercom Industries Inc., Sunnyvale, CA, and with Filtronic Components Ltd., Leeds, U.K. From 1991 to 1995, he was with the University of Bradford, Bradford, U.K., where he was a Senior Lecturer. From 1995 to 2001, he was a Fellow Engineer with Filtronic Comtek, where he was involved with filters for cellular radio applications. He is currently a Reader with the Institute of Microwaves and Photonics, School of Electronic and Electrical Engineering, The University of Leeds. He also teaches courses on circuit theory, RF and microwave engineering, and RF systems. His research projects include tunable microwave filters using ferroelectric devices, dielectric resonators, wide-band amplifier design, power amplifiers, MMIC design, and EW receivers. He has authored and coauthored numerous papers in the IEEE TRANSACTIONS ON MICROWAVE THEORY AND TECHNIQUES and the PROCEEDINGS OF THE IEE. He also authored *Theory and Design of Microwave Filters* (London, U.K.: IEE Press, 2001).

Dr. Hunter is a Fellow of the Institution of Electrical Engineers (IEE), U.K.

Roger D. Pollard (M'77–SM'91–F'97) was born in London, U.K., in 1946. He received the B.Sc. and Ph.D. degrees in electrical and electronic engineering from The University of Leeds, Leeds, U.K.

He holds the Agilent Technologies Chair in High Frequency Measurements and is Head of the School of Electronic and Electrical Engineering, The University of Leeds, where he has been a faculty member since 1974. He is an active member of the Institute of Microwaves and Photonics, The University of Leeds, which has over 40 active researchers, a strong graduate program, and has made contributions to microwave passive and active device research. This activity has significant industrial collaboration, as well as a presence in continuing education. He has been a consultant to Agilent Technologies (previously Hewlett-Packard Company), Santa Rosa, CA, since 1981. He has authored or coauthored over 100 technical papers. He is an Editor for the IEEE Press RF and Microwave Technology Series. He holds three patents. His research interests are microwave network measurements, calibration and error correction, microwave and millimeter-wave circuits, terahertz technology, and large-signal and nonlinear characterization.

Roger Pollard is a Chartered Engineer. He is a Fellow of the Institution of Electrical Engineers (IEE), U.K. He is an active IEEE volunteer as an elected member of the Administrative Committee and 1998 President of the IEEE Microwave Theory and Techniques Society (IEEE MTT-S), the 2001/2002 chair of the Products Committee, a member of the IEEE Technical Activities Board and vice-chair of the Publications, Services and Products Board (PSPB). He was chair (1998–2000) of the Electronic Products Committee, which was responsible for the development and introduction of IEEEXplore. He has served as chair of the UKRI section and on many volunteer committees, groups, and working parties. He is a member of the Editorial Board of the IEEE TRANSACTIONS ON MICROWAVE THEORY AND TECHNIQUES and has been on the Technical Program Committee for the IEEE MTT-S International Microwave Symposium (IMS) since 1986.