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A Simple Model of EMI-Induced Timing Jitter in Digital Circuits, its Statistical Distribution and its Effect on Circuit Performance

Martin P. Robinson, Katharina Fischer, Ian D. Flintoft, *Member, IEEE*, and Andrew C. Marvin, *Member, IEEE*

Abstract—A simple model has been developed to characterize electromagnetic interference induced timing variations (jitter) in digital circuits. The model is based on measurable switching parameters of logic gates, and requires no knowledge of the internal workings of a device. It correctly predicts not only the dependence of jitter on the amplitude, modulation depth and frequency of the interfering signal, but also its statistical distribution. The model has been used to calculate the immunity level and bit error rate of a synchronous digital circuit subjected to radio frequency interference, and to compare the electromagnetic compatibility performance of fast and slow logic devices in such a circuit.

Index Terms—Digital circuits, immunity, jitter, radio frequency interference (RFI), statistical distribution, timing delays.

I. INTRODUCTION

ELECTROMAGNETIC interference (EMI) can cause random variations in the timing of digital circuits. This effect is known as EMI-induced jitter, and can occur at threat levels that are too low to lead to false switching [1], [2]. It is observed at all levels of integration up to very-large-scale-integration (VLSI) circuits [3]. Chappel and Zaky have proposed defining a *delay margin* that will help determine whether the jitter violates the timing constraints of a particular circuit [4].

Jitter is becoming increasingly important in the design of logic circuits as a result of rising clock frequencies, and a level of 'intrinsic' jitter (due both to deterministic effects in the link between transmitter and receiver and to stochastic effects within a digital device) exists even in the absence of EMI. We have recently shown that EMI-induced jitter correlates with the levels of cross-modulation products that are re-emitted when a digital circuit is subjected to a radiated threat field—behavior which enables us to tell which digital subsystems are affected by the interference, and to predict when circuit failure is imminent [5].

It would be useful to be able to predict the levels of jitter, and researchers have modeled the susceptibility of logic devices to EMI using circuit analysis tools such as SPICE [1], [6], [7]. Although these can give accurate results, they may be complicated to set up and SPICE simulations sometimes require knowledge of the internal workings of devices that manufacturers are unwilling to supply [8]. Our approach has therefore been to
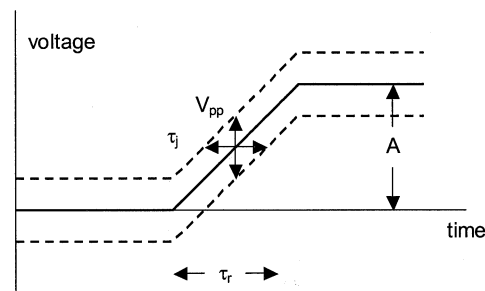
Fig. 1. Simple theory of RFI-induced jitter.

concentrate on "intermediate level tools": analytical or empirical design methods that are sufficiently accurate to be useful, while being simple enough to use at an early stage in the design process.

In this paper, we take a simple model of jitter that we have previously described [9], and show how the addition of an extra element, a low-pass filter, leads to improved predictions of both the level and the statistical distribution of timing variations. We then go on to investigate how such variations can lead to failure in a real circuit, and consider the relative merit of implementing the circuit with fast or slow logic families.

II. SIMPLE THEORY OF JITTER

Consider a nominally square-wave signal being passed between two logic inverters in a digital circuit. If some small amount of radio frequency interference (RFI) is coupled into the circuit then we begin by assuming that the signal at the input to the second gate is the sum of the logic waveform and the RFI.

Fig. 1 shows how this can lead to timing variations. If the instantaneous value of the RFI is positive at the moment of switching, then the input signal will cross the logic threshold a little earlier than usual, while if the RFI is negative, the switching will occur later. If there is no fixed phase relationship between the system clock and the interference, there will be a random distribution of switching times, whose envelope we can define as the level of jitter.

By further assuming the logic waveform to be trapezoidal, we can predict the jitter induced in a logic device with rise time τ_r and switching amplitude A. If the threat waveform is a modulated sine wave of root-mean-square voltage V_{RFI} and modulation depth m, then the peak-to-peak threat signal is

$$V_{\mathrm{pp}} = 2\sqrt{2}(1+m)V_{\mathrm{RFI}}. \qquad (1)$$

To obtain the maximum variation in delay, i.e, the jitter, we multiply this by the rate of change of the signal during the transition, i.e, by τ_r/A, giving

$$\tau_{\mathrm{j}} = 2\sqrt{2}(1+m)V_{\mathrm{RFI}}\frac{\tau_{\mathrm{r}}}{A}. \tag{2}$$

We have shown previously that this theory gives reasonable agreement with measurements for six different families of logic devices at threat frequencies of up to 100 MHz [9].

The simple theory outlined above assumes that the level of RFI is constant over the switching time of the gate. This assumption is valid if the period of the RFI is large compared to τ_r, and is likely to become untenable as the threat frequency increases. Indeed, we do see two discrepancies with measurements.

1) The observed level of jitter is not independent of threat frequency as the simple theory suggests.
2) The statistical distribution of timing variations is not symmetrical as might be expected from the theory.

Before explaining how the simple theory can be modified to account for these effects, it is first necessary to consider the statistical distribution of a modulated sine wave.

A. Statistical Distribution of the EMI

According to the simple theory outlined above, the changes in signal amplitude are converted to changes in timing by the rising (or falling) edge of the pulse. The statistical distribution of the timing variations can therefore be obtained from the probability density function (PDF) of the RFI. This is simply the likelihood of the RFI having some value x at a randomly chosen time. If the threat waveform is an unmodulated sine wave of unit amplitude, then, the PDF is obtained by differentiating the function $\sin^{-1}(x)$ and normalizing so that the integral of the PDF is unity. This gives

$$p(x) = \frac{1}{\pi\sqrt{1-x^2}}, \qquad \text{for} \quad |x| < 1. \tag{3}$$

This is illustrated in Fig. 2, where the peaks in the PDF occur because the sinusoidal waveform spends more time near its extremities than at the centre.

If the threat waveform is now amplitude modulated with another sine wave, the PDF is less straightforward to calculate. However, we may consider the PDF as a weighted average over all possible values of amplitude between $1-m$ and $1+m$ [which themselves have distribution similar in form to that of (3)]. By integrating these low-frequency PDFs, we obtain the following expression for the amplitude-modulated RFI:

$$p(x) = \int_{\max(|x|,1-m)}^{1+m} \frac{dA}{\sqrt{(A^2-x^2)\left(m^2-[A-1]^2\right)}},$$
$$\text{for} \quad |x| < 1+m \tag{4}$$

which, although not soluble analytically, can be evaluated numerically, giving PDFs such as those shown in Fig. 3, for various values of m.

Note the symmetry of the distribution, and the way that the range widens but the two peaks move closer together as the modulation depth increases.
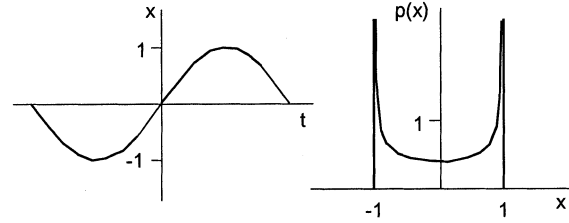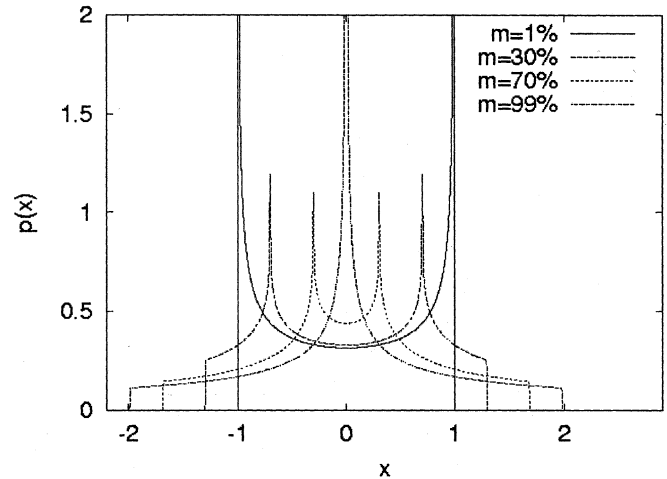

Fig. 2.   PDF of an unmodulated sine wave.

Fig. 3.   PDFs for amplitude-modulated sine waves of various modulation depths m.

We may briefly consider other forms of modulation. Frequency modulation and phase modulation should give the same PDF as an unmodulated sine wave, because the PDF does not depend on carrier frequency or phase. For pulse modulation, the PDF will have the same (unmodulated) form when the modulation is "on," but will be a delta function at $x = 0$ when the modulation is "off," the combined PDF being a weighted average depending on the duty cycle. Other types of interference such as Gaussian noise are not considered here but could be the subject of further research.

III. MEASUREMENTS

Simple digital circuits were used to investigate the envelope and the distribution of timing variations. Previous work had indicated that although jitter could be induced by applying RFI to any of the pins of a logic integrated circuit (IC), the greatest levels were seen when it was applied directly to the track connecting the output of one gate to the input of the next [9]. Fig. 4 shows a typical test circuit. RFI was applied in one of two ways: by coupling to a particular point in the circuit using a purpose-built injection circuit, or by irradiation of the circuit board in an anechoic chamber.

The injection circuit is shown in Fig. 5. The 3:1 transformer matches the 50-Ω threat source (a signal generator and amplifier) to the 5.6-Ω resistor. When plugged into the test circuit, it acts as an isolated RF source with an impedance of a few ohms.

To allow the signals on the test circuit to be monitored while the board was irradiated, digital optical-fiber links were connected to each IC. These have an intrinsic jitter of between 1
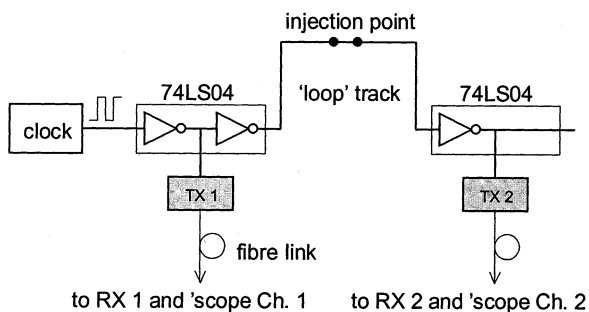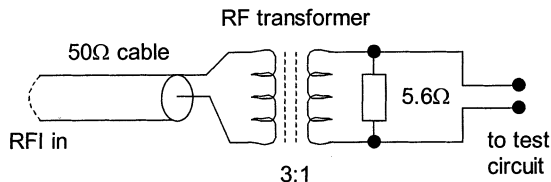
Fig. 4. Jitter test circuit.
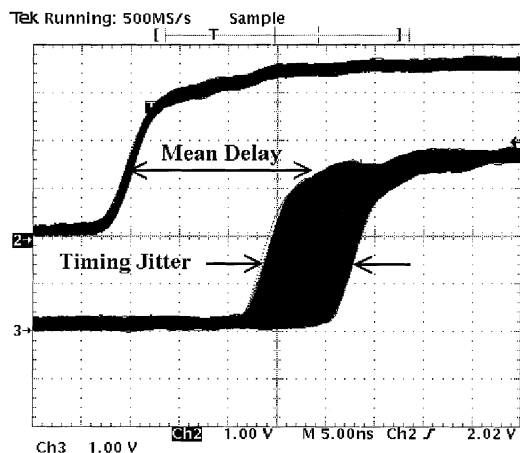

Fig. 5. RF injection circuit.

Fig. 6. Delay parameters obtained from the oscilloscope.

and 2 ns, which has an approximately Gaussian distribution, and which limits the lowest levels of jitter that can be measured.

The signals at various points in the circuit were displayed on a Tektronix TDS540 digital storage oscilloscope. This was interfaced to a computer, enabling us to acquire a large number of waveforms for statistical analysis. Fig. 6 shows how the jitter can be obtained as the difference between maximum and minimum delays.

Fig. 7 shows the variation of jitter with injected RFI voltage, measured at seven frequencies. The variation becomes nonlinear as the level of RFI increases, although the deviation from linearity is different for the high and low threat frequencies. Each curve stops at the point where the circuit fails as a result of false switching. At the higher frequencies, we see less induced jitter and higher immunity, an effect not predicted by the simple theory. This variation of jitter with frequency was also noted by Laurin *et al.* [2].

The statistical distribution of delay variations is shown in Fig. 8 for four different values of modulation depth (modulation frequency 1 kHz). There are peaks in the distribution whose positions are well predicted by the simple model. The peaks are
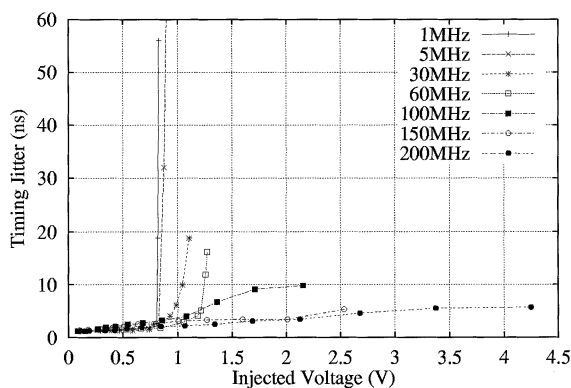

Fig. 7. Measured variation of jitter with threat level and frequency.
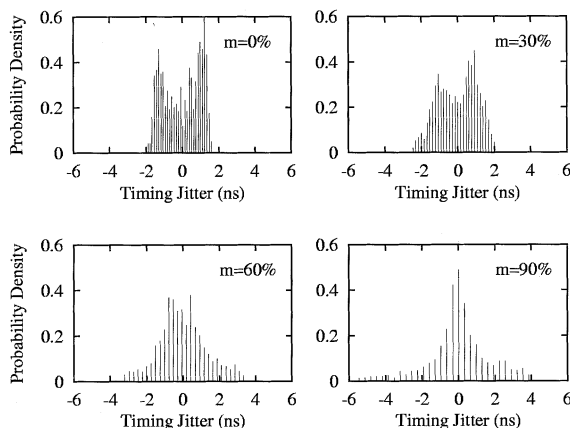
Fig. 8. Measured distributions of delay times for four different modulation depths of interfering RF signal.
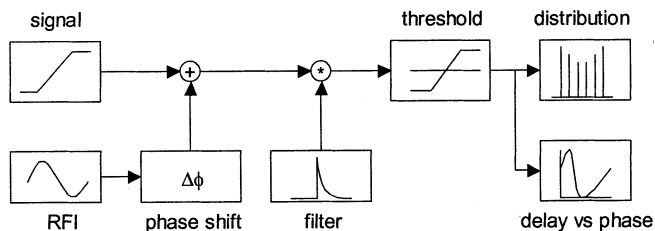
Fig. 9. Improved model for jitter including low-pass filtering.

not as sharp as those seen in Fig. 3, but this can be explained by considering the observed distribution as a convolution of the RFI-induced jitter with the intrinsic jitter of the measurement system. The distribution also shows some asymmetry, which becomes more pronounced as the threat level increases, and is not predicted by the simple theory.

IV. MODIFIED THEORY OF JITTER

We have seen that the simple theory fails to predict the reduction in jitter as the frequency of the RFI increases. It is also known that the immunity of logic devices to impulsive noise increases as the width of the pulse decreases. To account for this behavior, we have enhanced the theoretical model by introducing a low-pass filter element.

For convenience, we have implemented the modified theory using the program MATLAB [10], as illustrated in Fig. 9. In a

Fig. 10.   Variation of jitter with threat level and frequency, as predicted by the modified theory.

Fig. 11.   Calculated distribution of delay times, showing asymmetry.

practical situation, the phase of the RFI will generally be un-correlated with the logic signal. Rather than choosing random values for the phase, we introduce 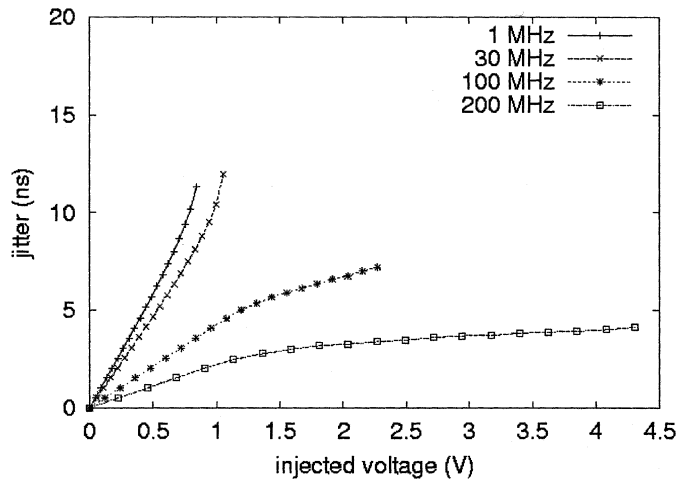a phase-shift block into the model and vary the phase in small steps from 0 to 2π. As before, the logic waveform is modeled in the time domain as a trapezoid. At each phase step, the RFI and logic waveforms are added, and the low-pass filtering is achieved by convolving the resulting waveform with the transfer function of the filter. This function is a decaying exponential $(1/\tau_{\text{filt}})\exp(-t/\tau_{\text{filt}})$ for $t \geq 0$, where τ_{filt} is the time constant of the filter. The propagation delay is then obtained from the time at which the filtered waveform crosses the logic threshold. After the phase-stepping is completed, the jitter is calculated as the difference between maximum and minimum delay, and the individual results can conveniently be presented either as a plot of delay versus the phase of the RFI, or as a statistical distribution of delay times.

Fig. 10 shows the calculated variation of jitter with threat voltage at several threat frequencies. The model used a rise time of 12 ns and a switching amplitude of 3.5 V. At present, the time constant of the low-pass filter τ_{filt} is determined empirically and a value of 4 ns (equal to a third of the rise time) was chosen to give the best fit to the measured data. Eventually, we hope either to be able to relate τ_{filt} to measurable switching parameters of a device, or to provide values of τ_{filt} for each available logic family. Faster logic families are expected to have shorter time constants. The plots in Fig. 10 end at the point where the RF amplitude would exceed the switching threshold, leading to static failure. A comparison of these plots with those in Fig. 7, shows that the modified theory successfully models the essential features of the variation of jitter with both amplitude and frequency of the RFI. There are discrepancies which may be due either to the presence of intrinsic jitter or to the fact that the logic waveform is not a perfect trapezoid. Nevertheless, the reduction in induced jitter with EMI frequency, and also the changes in the *gradients* of the plots with increasing EMI amplitude, are well predicted by the model.

Fig. 11 shows the statistical distribution of delay times as predicted by the modified theory. The threat signal was an unmodulated sine wave with an amplitude of 1.2 V. The calculated dis-
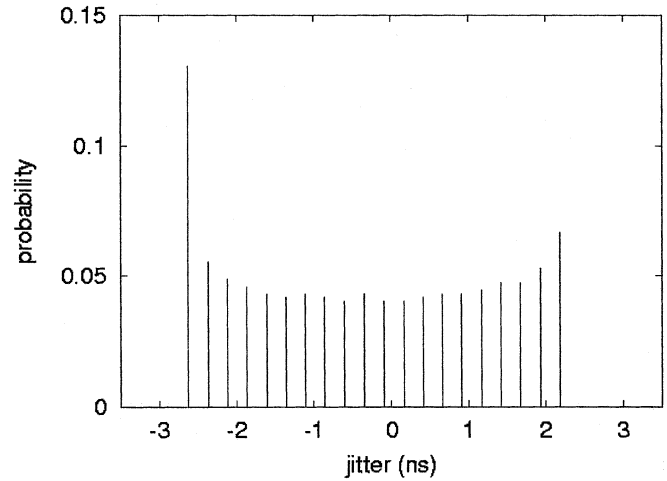
tribution is now asymmetric, because the filtered waveform is no longer linear (trapezoidal) as in Fig. 1. Increasing the level of RFI in the model increased the asymmetry of the distribution, again corresponding to our observations (Fig. 8).

The new model can also characterize the immunity of logic gates to impulsive (transient) noise. The dynamic immunity may be defined as the smallest pulse of a given width that will make the gate switch. If the input is a square pulse of width τ_w and amplitude A, then the voltage after filtering will reach a maximum value of $A[1 - \exp(-\tau_w/\tau_{\text{filt}})]$, before decaying exponentially to zero. On the assumption that interference will only be propagated when this maximum value exceeds the logic threshold V_{thresh}, the dynamic immunity will be given by

$$V_{\text{im}} = \frac{V_{\text{thresh}}}{1 - \exp\left(\frac{-\tau_w}{\tau_{\text{filt}}}\right)}. \tag{5}$$

Fig. 12 shows the calculated immunity as a function of pulse width. The model predicts that for shorter pulses, a greater amplitude is needed to cause switching, corresponding to the behavior observed in real logic devices [11].

V. EFFECT OF JITTER ON CIRCUIT PERFORMANCE

Can jitter lead to circuit failure? The effects of jitter will depend on the timing constraints of a particular circuit, and it may be that static failure (i.e, bit errors) occurs before the jitter becomes large enough to create problems. However we have constructed a simple circuit that does fail as a result of jitter, and this is shown in Fig. 13.

In normal operation, the propagation delays in the two branches will be closely matched, the two inputs to the exclusive-or (XOR) gate will be the same, and so the output will always be zero. However, any change in propagation delay in one branch will lead to the inputs' being different for a moment, and the appearance of a short pulse or 'glitch' at the output. We shall define 'circuit failure' as occurring when the amplitude of this glitch is greater than the switching threshold.

As expected, injecting sufficient RFI into one branch of the "XOR" circuit did cause glitches to appear at the output. Two aspects of this behavior will now be considered: the immunity
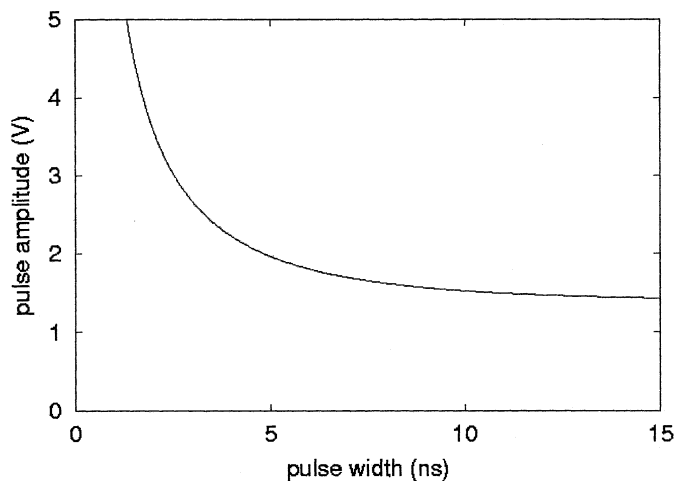
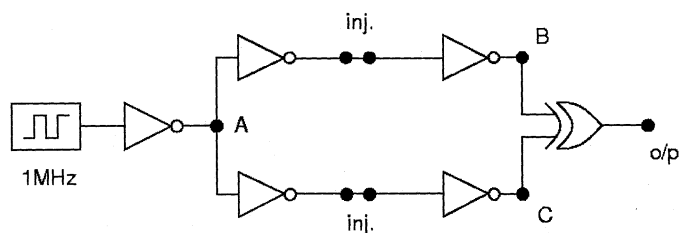Fig. 12. Calculated immunity of a logic gate to impulsive noise.

Fig. 13. "XOR" circuit for demonstrating effects of jitter.

TABLE I
IMMUNITY OF "XOR" CIRCUIT TO 80%
AMPLITUDE-MODULATED RFI

logic family	threshold (V)	immunity (V)	
		calculated	observed
4000B	2.5	0.98	0.75
74HC	2.2	0.86	0.68
74AC	2.2	0.86	0.67
74HCT	1.4	0.55	0.36
74ACT	1.4	0.55	0.46
74LS (i)	1.4	0.55	0.40
74LS (ii)	1.4	0.55	0.48
74ALS (i)	1.4	0.55	0.59
74ALS (ii)	1.4	0.55	0.34
74F	1.4	0.55	0.56

level of the circuit, and the bit error rate observed once this level has been exceeded.

A. Immunity Level of 'XOR' Circuit

Let us initially consider the case where the time period of the RFI is long compared to the rise and fall times of the logic gate, rendering the low-pass filter unnecessary, and allowing us to use the simple theory of Section II. Let us assume that to get a glitch from the output, the difference in timing of the inputs must be great enough to allow the output to rise to the logic threshold. For a trapezoidal waveform, the greatest allowable difference in times is then $V_{\text{thresh}}\tau_r/A$.

The simple theory predicts a symmetrical distribution of timing delays, and a maximum change in delay of $\tau_j/2$. Equating the two times, and substituting (2) gives

$$V_{\text{im}} = \frac{V_{\text{thresh}}}{\sqrt{2}(1+m)}. \tag{6}$$

Interestingly, this predicts that the immunity of the circuit will be independent of all switching parameters except for the logic threshold.

To test this prediction, the immunity of the circuit was measured by increasing the RFI in steps of 0.1 dB, until the output was able to trigger an oscilloscope at the switching threshold. The circuit was implemented using eight different logic families, with maximum operating frequencies ranging from less than 10 MHz for 4000B CMOS, to nearly 200 MHz for 74ACT. Table I shows the logic thresholds [12] and the predicted and measured immunity to 80% modulated RFI,

for the various types of logic. The "observed" values are the mean of measurements made by injecting RFI into the upper and lower branches of the circuit in Fig. 13. The two sets of data presented for 74LS and 74ALS refer to measurements performed on devices from different manufacturers. The interference frequency was 30 MHz for all logic families except 4000B, where it was 3 MHz.

The agreement is good, considering the simplicity of the model. As predicted, the differences in immunity are much less than the differences in the switching parameters of the different logic types.

B. Bit Error Rate of "XOR" Circuit

Once the RFI has reached the threshold of immunity, errors in the form of glitches will begin to appear at the circuit's output. However, not every switching transition will have its timing altered sufficiently to produce a glitch. To calculate the frequency of errors, we can refer to the statistical distribution of timing delays discussed in Section II-A.

Fig. 14 shows the PDF for the instantaneous value of amplitude-modulated, sinusoidal RFI. To create an error, the magnitude of the voltage must exceed the immunity level V_{im}, and the rate of errors is therefore proportional to the area of the shaded regions in Fig. 14.

As can be seen from Fig. 3, changing the modulation depth m alters the shape of the PDF, and should therefore lead to a different variation of error rate with RFI amplitude. To test this, we calculated the error rate for various value of m by numerically integrating the PDF, and also measured it by connecting a frequency counter to the output of the circuit. Fig. 15 shows the results for 74F logic, subjected to a carrier frequency of
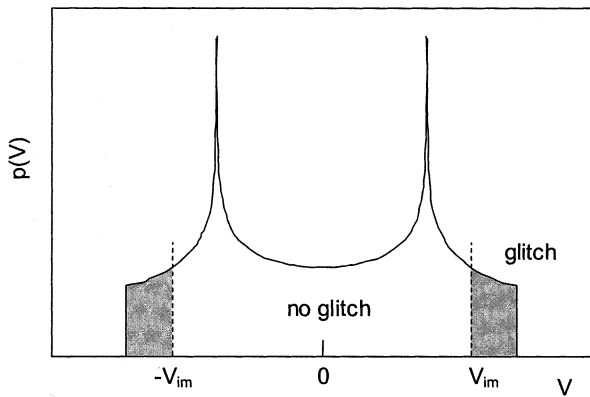
Fig. 14. Probability that instantaneous value of RFI exceeds immunity level.
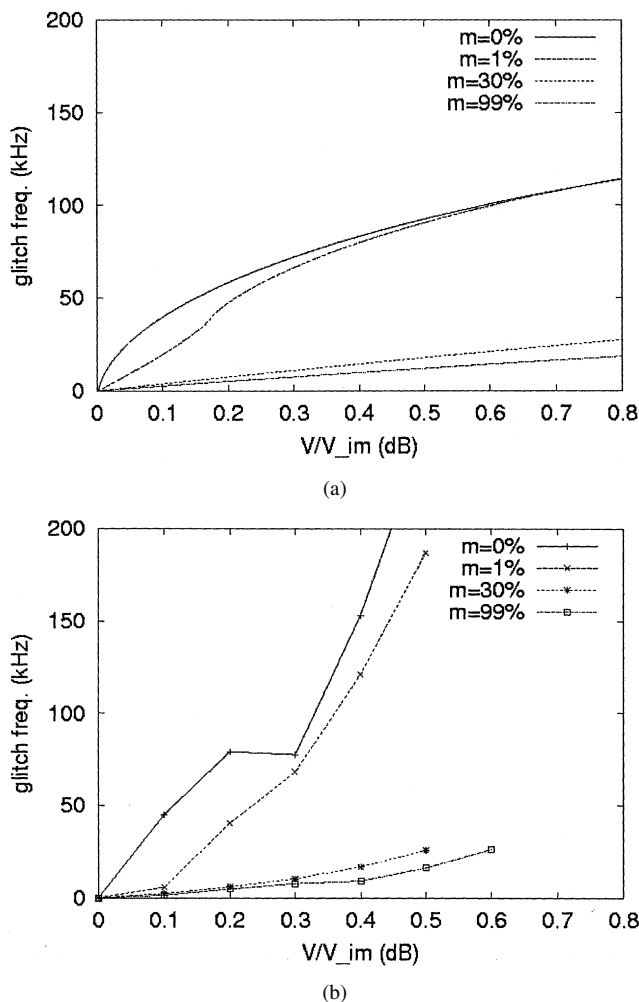

(a)

(b)

Fig. 15. Rate of errors produced by "XOR" circuit for threat voltages exceeding the immunity level (a) calculated (b) observed.

30 MHz and modulation frequency of 1 kHz. The model correctly predicts that the glitch frequency rises faster when m is smaller. This behavior can be understood by referring to Fig. 3: for smaller modulation depths, the peaks at $\pm(1-m)$ are closer to the edge of the PDF. The agreement between theory and measurement is worse at $m = 0\%$ and 1%, than at 30% and 99%. A possible explanation is that the small amount of intrinsic jitter

in the logic devices becomes convolved with the EMI-induced jitter, thus smoothing the peaks in the statistical distribution.

VI. DISCUSSION AND CONCLUSION

The model presented above successfully represents the dependence of jitter on the amplitude, frequency and modulation depth of the interfering signal. An advantage over more complex methods is that no knowledge is required of the internal workings of a logic device, but only measurable switching parameters such as the rise and fall times. The introduction of the low-pass filter into the model leads to predictions of lower jitter at higher frequencies, and higher dynamic immunity to shorter pulses. Both these effects are observed in practical measurements.

The model gives not just the maximum variation in delay times, i.e, the jitter, but also its statistical distribution. We have shown that this information can help us estimate the bit error rate that occurs when the EMI-induced jitter exceeds the delay margin in a digital circuit.

In addition to EMI-induced jitter a real circuit will have some level of intrinsic jitter. Generally, the two effects should be uncorrelated, so the distribution of the combined jitter can be found from the convolution of the individual distributions, and the envelope obtained by summing their maxima or minima. An interesting situation arises when jitter is induced in different parts of a digital circuit by the same source of EMI, as the distributions will no longer be uncorrelated. This is an area for possible further research.

The work described above enables us to consider the relative merits of fast and slow logic families in digital circuits. Faster logic types are known to emit higher levels of EMI than slow ones [13]. Slower types of logic are less susceptible to impulsive noise when the pulse width is less than the response time. On the other hand, the model predicts that a constant level of sinusoidal RFI will induce greater levels of jitter in a slow logic device than in a fast one, provided that the period of the interfering signal is long compared to the rise and fall times of the device.

The investigation into the immunity of a real circuit revealed that although more jitter was indeed induced in slower logic devices, circuits implemented with slower logic were also less susceptible to the glitches arising from timing errors. The two effects almost cancel each other, leading to an immunity level that depends only on the switching threshold. The work presented here supports this advice to circuit designers: use the slowest logic type possible without compromising circuit performance.

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Katharina Fischer, photograph and biography not available at the time of publication.

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