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Comparative Evaluation of Current Limiting Methods in Grid-Following and Grid-Forming Inverters

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Abstract—The increasing penetration of inverter-based resources (IBRs) has introduced new challenges in power system operation, particularly during grid faults. Unlike synchronous generators, which can supply fault currents of up to 5–10 p.u., IBRs are typically limited to 1.2–1.6 p.u. due to semiconductor device constraints. Consequently, effective current-limiting strategies are required to protect power converters while maintaining stable operation and fault ride-through (FRT) capability. This paper presents a comparative assessment of direct current-limiting strategies for grid-following (GFL) inverters and indirect current-limiting strategies for grid-forming (GFM) inverters under identical operating and fault conditions. For GFL inverters, magnitude limiter and d and q axis-priority current-limiting strategies with anti-windup compensation are investigated. Among the evaluated methods, magnitude current limiting provides the best overall performance with improved post-fault recovery. For GFM inverters, fixed virtual impedance (VI), adaptive virtual impedance (AVI), and low-voltage ride-through with AVI (LVRT+AVI) are evaluated under different fault impedances. The results show that LVRT+AVI strategy provides the best fault-current suppression and fastest post-fault recovery among the investigated GFM methods while preserving voltage-source characteristics. The performance of these methods is assessed in MATLAB/Simulink.

Keywords— *Grid Following Inverter, Grid Forming Inverter, Current Limiting strategies, fault ride-through capability.*

I. INTRODUCTION

The growing concerns over climate change and the depletion of fossil fuel resources have accelerated the integration of renewable energy sources into modern power systems via power electronic devices, these are called as inverter based resources (IBRs) [1]. However, the increasing penetration of IBRs changes power system dynamics and creates challenges in system stability, inertia support, and fault ride-through (FRT) capability. Therefore, maintaining stable and reliable power system operation has become a major concern in IBR dominated power system [2]. The most commonly utilized method for controlling IBRs is grid following (GFL) control in which IBR operates as a current source and depends on a phase-locked loop (PLL) for grid synchronization. However, their performance may deteriorate under weak-grid conditions. To address these limitations, grid forming (GFM) control has

emerged as a promising method [3]. Unlike GFL inverters, GFM inverters behave as voltage source and can establish grid voltage and frequency independently. Despite their different operating principles, ensuring FRT capability remains a critical challenge in both GFL and GFM [4]. To achieve FRT capability, various current limiting strategies have been proposed to limit fault currents during grid faults. However, their effectiveness in maintaining transient stability and ensuring post-fault recovery depends on their control architecture [1], [2], [4]–[6]. Current limitation can be implemented at different levels of inverter control. These levels range from the PWM stage and inner control layer to the outer control layer. The selected control layer determines how the inverter current is constrained. When it is done at the current control layer, it provides the direct means of current limiting. However, it can affect the interaction between the inner and outer control loops and also influence the post-fault recovery. In contrast, when its done at the outer layer, it limits the current indirectly through the voltage control action. This can provide better coordination with the overall control structure. However, transient current overshoots may occur. Based on the control mechanism, current-limiting methods are broadly classified into two categories in this work. The first category comprises direct current-limiting methods, which constrain the current at the current control layer. The second category comprises indirect current-limiting methods, which regulate the voltage control action to limit the current indirectly. While both direct and indirect methods can be applied to GFL and GFM, direct methods are preferred for GFL and indirect methods preferred for GFM [3]–[5]. Several current-limiting techniques have been developed using these two approaches in the literature as given in Table I. The majority of the existing studies are focused on GFM inverters [2], [5]–[7] and there is little attention paid to comparing current limiting strategies for both GFL and GFM control architectures and identify a better approach for a specific requirement. To address this gap, this paper presents a comparative assessment of GFL and GFM current-limiting strategies in terms of their rate of fault ride-through, transient stability and post-fault recovery. The main

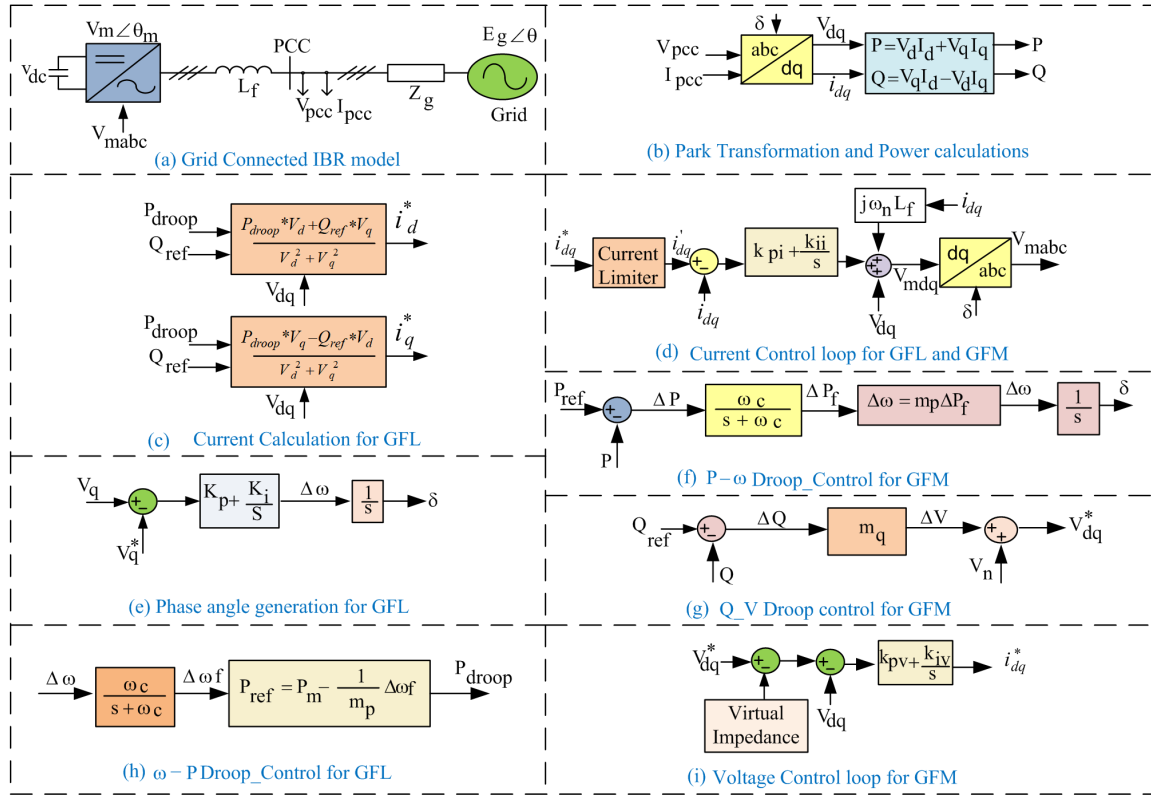


Fig. 1: Control structures of GFL and GFM inverters.

TABLE I: Comparison of Existing Studies on Current Limiting Strategies for IBRs

Reference	GFL	GFM	Direct Limiting	Indirect Limiting	FRT	Stability	Recovery	Fault Impedance
[1]	×	✓	✓	✓	✓	✓	✓	○
[2]	×	✓	✓	✓	✓	✓	○	○
[3]	×	✓	✓	✓	×	✓	○	○
[4]	×	✓	✓	✓	✓	✓	✓	○
[5]	×	✓	×	✓	✓	×	○	○
[6]	×	✓	×	✓	✓	✓	✓	○
This Paper	✓	✓	✓	✓	✓	✓	✓	✓

Note: ✓ indicates comprehensive coverage; ○ indicates limited consideration; and × indicates not covered.

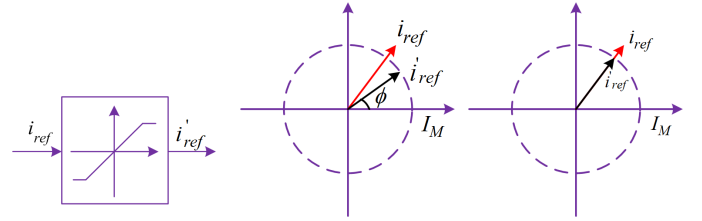
contributions of this work are summarized as follows:

- A comparative investigation of GFL (direct) and GFM (indirect) current limiting strategies under balanced three-phase faults, highlighting their stability and fault ride-through characteristics.
- To evaluate the influence of fault impedance on the fault-current suppression and post-fault recovery characteristics of GFL and GFM inverters under each method..

II. SYSTEM MODELING AND CURRENT-LIMITING METHODS

A. System Modelling

As shown in Fig. 1, the IBR is connected to the grid through a filter inductance L_f and grid impedance Z_g . The GFL controller employs a PLL for synchronization and a current limiter to constrain fault currents. In contrast, the GFM controller utilizes $P-\omega$ and $Q-V$ droop control for frequency



(a) Instantaneous (b) Magnitude-based (c) Priority-based
Fig. 2: Direct current-limiting strategies: (a) instantaneous limiter, (b) magnitude-based limiter, and (c) priority-based limiter.

and voltage regulation, while virtual impedance is incorporated to mitigate fault currents and enhance transient stability.

B. Classification of Current Limiting Strategies

Current limiters are categorized into two types i.e Direct current limiters and Indirect current limiters

1. Direct Current Limiters : In direct current limiting strategy, the reference currents i_{dref} and i_{qref} generated by the outer control loop are passed through a saturation block to ensure that the inverter current remains within the maximum allowable limit ($I_M \leq 1.2$ p.u.). During fault conditions, the reference currents are modified to the limited current references i'_{dref} and i'_{qref} based on the current limiting method as shown in Fig. 2. The commonly used direct current limiting strategies are described below.

a) Instantaneous Limiter [1], [2]: Instantaneous Limiter is the simplest form of current limiter. It applies an element-

wise saturation to each phase currents independently when the reference current exceeds the predefined limit as shown in Fig. 2a , The saturated current reference is given by (1).

$$i'_{\text{ref},x} = \text{sign}(i_{\text{ref},x}) \cdot \min(|i_{\text{ref},x}|, I_{M,x}), \quad x \in \{d, q, \alpha, \beta\} \quad (1)$$

where $i_{\text{ref},x}$ and $i'_{\text{ref},x}$ denote the reference and limited current, and $I_{M,x}$ represents the maximum allowable current limit. In the abc frame, $I_{M,x}$ is selected as I_M , whereas in the $\alpha\beta$ and dq frames, it is typically chosen as $I_M/\sqrt{2}$ to satisfy (2).

$$i_x'^2 + i_y'^2 \leq I_M^2, \quad x, y \in \{d, q\} \text{ or } \{\alpha, \beta\}. \quad (2)$$

To maintain the resultant current within the specified limit I_M , the d - and q -axis current components are individually limited to $I_M/\sqrt{2}$. This is because allowing both components to reach I_M simultaneously would make the total current magnitude as $\sqrt{2}I_M$, exceeding the prescribed current limit. This method is easy to implement and provides a fast response. However, independent saturation of each current component may introduce waveform distortion and reduce current utilization during severe faults.

b) Magnitude Limiter [1], [2]: Magnitude-based current limiter, also known as the circular limiter shown in Fig. 2b, restricts the current magnitude without affecting the current angle as given in (3). It is typically implemented in the $\alpha\beta$ and dq reference frames.

$$i'_{\text{ref},x} = i_{\text{ref},x} \min\left(1, \frac{I_M}{|i_{\text{ref}}|}\right), \quad x \in \{a, b, c, d, q, \alpha, \beta\} \quad (3)$$

When $I_{\text{ref}} > I_M$, the reference current vector is uniformly scaled by the factor I_M/I_{ref} , preserving its direction while reducing its magnitude to the maximum allowable value I_M . Otherwise, the reference current remains unchanged. Since all current components are scaled proportionally, this method preserves the current vector orientation but does not allow independent prioritization of active and reactive current injection during fault conditions.

c) Priority-Based Limiter [1], [2]: Priority-based limiter allocates the available current according to a predefined priority as shown in Fig. 2c . In the d -axis priority strategy, the active current is given priority and the remaining current capacity is assigned to the q -axis current defined by (4),(5). In the q -axis priority strategy, the reactive current is prioritized, while the remaining capacity is allocated to the d -axis current as given in (6),(7).

D-axis priority:

$$i'_{\text{dref}} = \text{sign}(i_{\text{dref}}) \min(|i_{\text{dref}}|, I_M) \quad (4)$$

$$i'_{\text{qref}} = \text{sign}(i_{\text{qref}}) \min(|i_{\text{qref}}|, \sqrt{I_M^2 - i_{\text{dref}}'^2}) \quad (5)$$

Q-axis priority:

$$i'_{\text{qref}} = \text{sign}(i_{\text{qref}}) \min(|i_{\text{qref}}|, I_M) \quad (6)$$

$$i'_{\text{dref}} = \text{sign}(i_{\text{dref}}) \min(|i_{\text{dref}}|, \sqrt{I_M^2 - i_{\text{qref}}'^2}) \quad (7)$$

d) Anti-Windup Compensation [8]:

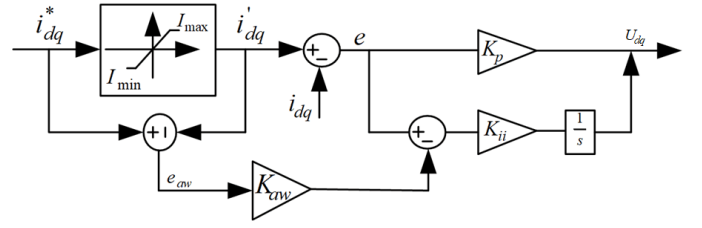


Fig. 3: Anti windup Compensation

During normal operation, the current limiter passes the reference current directly to the current controller. During a fault, when the current magnitude exceeds the specified limit, the reference is clamped and the limited value is sent to the controller. Since the clamped reference is applied during the fault, the PI controller continues to accumulate the tracking error, resulting in integrator windup. After fault clearance, the accumulated error causes a temporary current overshoot and oscillations. To overcome this issue, a back-calculation anti-windup mechanism is incorporated into the PI controller, as shown in Fig. 3. The saturation error is fed back through the anti-windup gain K_{aw} to reduce the accumulated integrator error. This helps suppress the post-fault current overshoot and improves the recovery response.

2. Indirect Current Limiters [1], [2], [4]–[6] : Indirect current limiters modify the inverter voltage reference through virtual impedance (VI) instead of directly limiting the current. VI was first applied to GFL inverters for smoother and more physics-based current limitation. It was extended to GFM inverters and has been widely adopted due to its ability to limit the fault current while preserving the voltage-source nature of the inverter. The current limiting methods based on VI can be divided into two types: fixed virtual impedance and adaptive virtual impedance.

a) Fixed Virtual Impedance (FVI): FVI limits the fault current to a pre-defined impedance value. However, fixed parameters may not provide optimal performance under varying grid strengths and fault conditions.

b) Adaptive Virtual Impedance (AVI): [5], [6], [9]: AVI dynamically regulates the virtual impedance according to the current threshold limit as shown in Fig. 4. The corresponding virtual reactance and virtual resistance are given by (8),(9),(10).

$$X_{VI} = k_{P_{RVI}}(I_s - I_n)\sigma_{X/R} \quad (8)$$

$$R_{VI} = \frac{X_{VI}}{\sigma_{X/R}} \quad (9)$$

$$I_s = \sqrt{i_d^2 + i_q^2} \quad (10)$$

where I_s denotes the inverter current, I_n is the current threshold limit, $k_{P_{RVI}}$ is the proportional gain of the AVI controller, and $\sigma_{X/R}$ represents the constant X/R ratio of the virtual impedance. The resulting virtual reactance X_{VI} and virtual resistance R_{VI} vary with the current deviation.

c) Low-Voltage Ride-Through-Adaptive Virtual Impedance (LVRT-AVI) Strategy [7], [10]: During voltage sags, the LVRT-AVI strategy is activated when the PCC voltage falls below 0.9

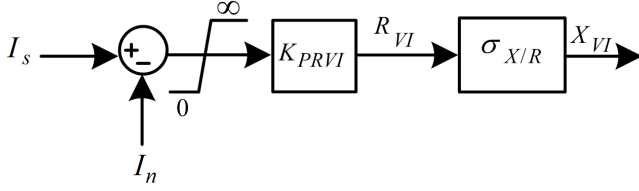


Fig. 4: Adaptive Virtual Impedance

p.u., as defined in (11). Under this condition, the strategy provides the required reactive power support to enhance voltage recovery. The controller updates the reactive current, reactive power, maximum active current, and active power references according to (11)–(14), thereby prioritizing reactive power support while ensuring compliance with the converter current limit. The controller changes the reactive current and power references to have enough current capacity to inject reactive current during the fault. If the inverter current exceeds the threshold limit, the AVI is activated according to (8),(9),(10) by introducing a virtual voltage drop. This limits the fault current and decreases transient oscillations.

$$I_q = \text{sat}[-KI_{\max}(V_0 - V_{PCC})] \quad (11)$$

$$Q_{ref} = -V_{PCC}I_q \quad (12)$$

$$I_{d\max} = \sqrt{I_{\max}^2 - I_q^2} \quad (13)$$

$$P_{ref} = \min(P_{set}, V_{PCC}I_{d\max}) \quad (14)$$

where V_{PCC} denotes the PCC voltage, V_0 is the nominal voltage, $I_{\max}$ is the maximum current limit, P_{set} is the pre-fault active power reference, I_q is the reactive current, Q_{ref} is the reactive power reference, $I_{d\max}$ is the maximum direct-axis current, and P_{ref} is the active power reference. The coefficient K in (11) represents the selected reactive current response to the PCC voltage deviation. In this work, $K = 2$ is selected based on the K -factor concept specified in VDE-AR-N 4120. After fault clearance, the PCC voltage returns toward its normal value, but small fluctuations may occur around the threshold. To avoid repeated switching, a narrow hysteresis band of 0.89–0.91 pu is used. The LVRT mode is removed only when $V_{pu} > 0.91$ pu, while the previous state is retained within the hysteresis band as given in (15).

$$S_{LVRT}(t) = \begin{cases} 1, & V_{pu}(t) < 0.89, \\ 0, & V_{pu}(t) > 0.91, \\ S_{LVRT}(t-1), & 0.89 \leq V_{pu}(t) \leq 0.91. \end{cases} \quad (15)$$

where V_{pu} is the PCC voltage in per unit, S_{LVRT} is the LVRT switching state, t is the continuous time variable, and $t-1$ denotes the state immediately before the switching instant.

The AVI is removed during fault recovery based on the current threshold $I_n = 1.05$ pu. As the inverter current decreases toward threshold, the required AVI is reduced gradually rather than being removed instantaneously. The current is passed through a saturation block with a lower limit of zero, which ensures that only positive virtual impedance values are applied. Hence, as the fault current returns to its normal value, the AVI

TABLE II: Test System Parameters

Parameter	Symbol	Value
Base power	S_b	10 MVA
Base voltage	V_b	20 kV
Nominal frequency	f_0	50 Hz
Filter inductance	L_f	0.2004 p.u.
Grid Resistance	R_g	0 p.u.
Grid inductance	L_g	0.2500 p.u.
Active power reference	P_{ref}	1 p.u.
Reactive power reference	Q_{ref}	0 p.u.
PLL proportional gain	k_p	1.25
PLL integral gain	k_i	1500
Current controller proportional gain	k_{pi}	1.25
Current controller integral gain	k_{ii}	10
Anti-windup gain	K_{aw}	0.1
Voltage controller proportional gain	k_{pv}	5
Voltage controller integral gain	k_{iv}	250
GFL droop gain	m_p	5%
GFM droop gains	m_p, m_q	2%, 3%
Current limit	$I_{\max}$	1.2 p.u.
Current threshold	I_n	1.05 p.u.
X/R ratio	$\sigma_{X/R}$	5.0
Short-circuit ratio	SCR	4.0

reduces to zero, allowing the converter to recover smoothly without introducing a negative impedance effect.

III. CASE STUDIES AND DISCUSSION

A. Case Study of GFL Inverter With Direct Current Limiters

The parameters chosen for the GFL Inverter are shown in Table II. The investigated direct current-limiting strategies, namely the magnitude-based limiter, d-axis priority limiter, and q-axis priority limiter exhibit similar fault-current limiting capability and maintained the fault current under the allowed limit (green dotted line in Fig. 5). However, their transient responses differ in terms of recovery time and post-fault current dynamics, as shown in Fig. 5 and Table III. The implemented anti-windup scheme reduced the post-fault current overshoot from approximately 1.22 pu to 1.19 pu. This resulted in faster transient recovery. The magnitude limiter achieved the highest fault-current reduction of 49.36% and 41.52% for the 10 Ω and 15 Ω fault cases, respectively. The fault-current reduction is calculated relative to the peak current of the baseline case without any current-limiting strategy. Moreover, it exhibited the shortest recovery time indicating faster restoration of the inverter current to its pre-fault steady-state value. The recovery time is measured from the fault-clearing instant until the inverter current returns to its pre-fault steady-state value. It is defined as

$$T_{\text{recovery}} = t_r - t_c, \quad (16)$$

where t_c denotes the fault-clearing instant and t_r denotes the instant at which the current returns to its pre-fault steady-state value and remains stable without significant oscillations. The d-axis and q-axis priority limiters showed longer recovery times than the magnitude limiter for both faults. For the 10 Ω fault, the recovery times were 0.50 s and 0.60 s, respectively. These increased to 0.62 s and 0.70 s for the 15 Ω fault. The longer recovery is mainly due to the unequal sharing of the available current between the d - and q -axis components. This

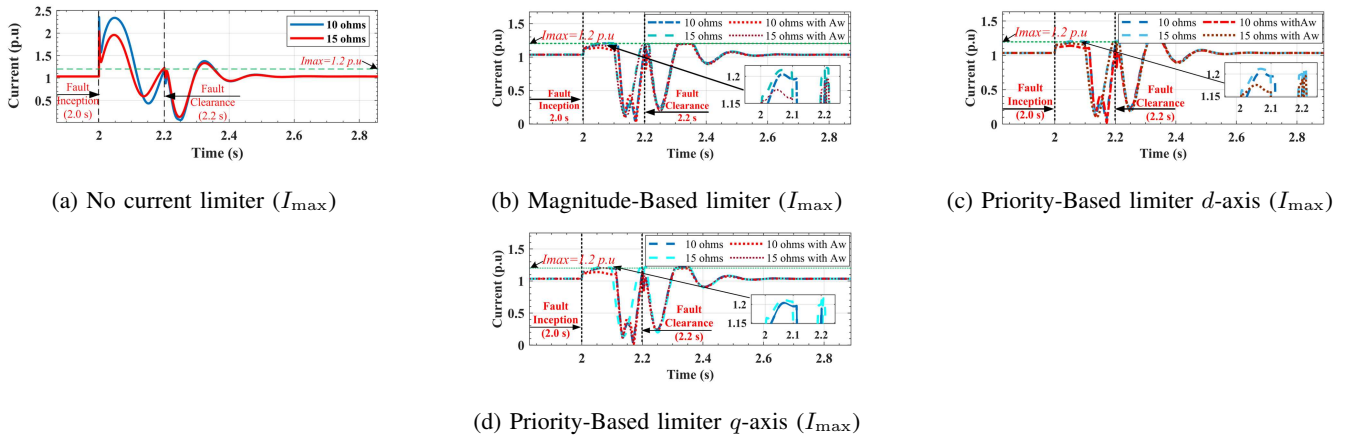


Fig. 5: Comparison of GFL inverter responses under 10 Ω and 15 Ω fault conditions. (a) No current limiter, (b) Magnitude-based limiter, (c) Priority-Based limiter (d -axis), and (d) Priority-Based limiter (q -axis).

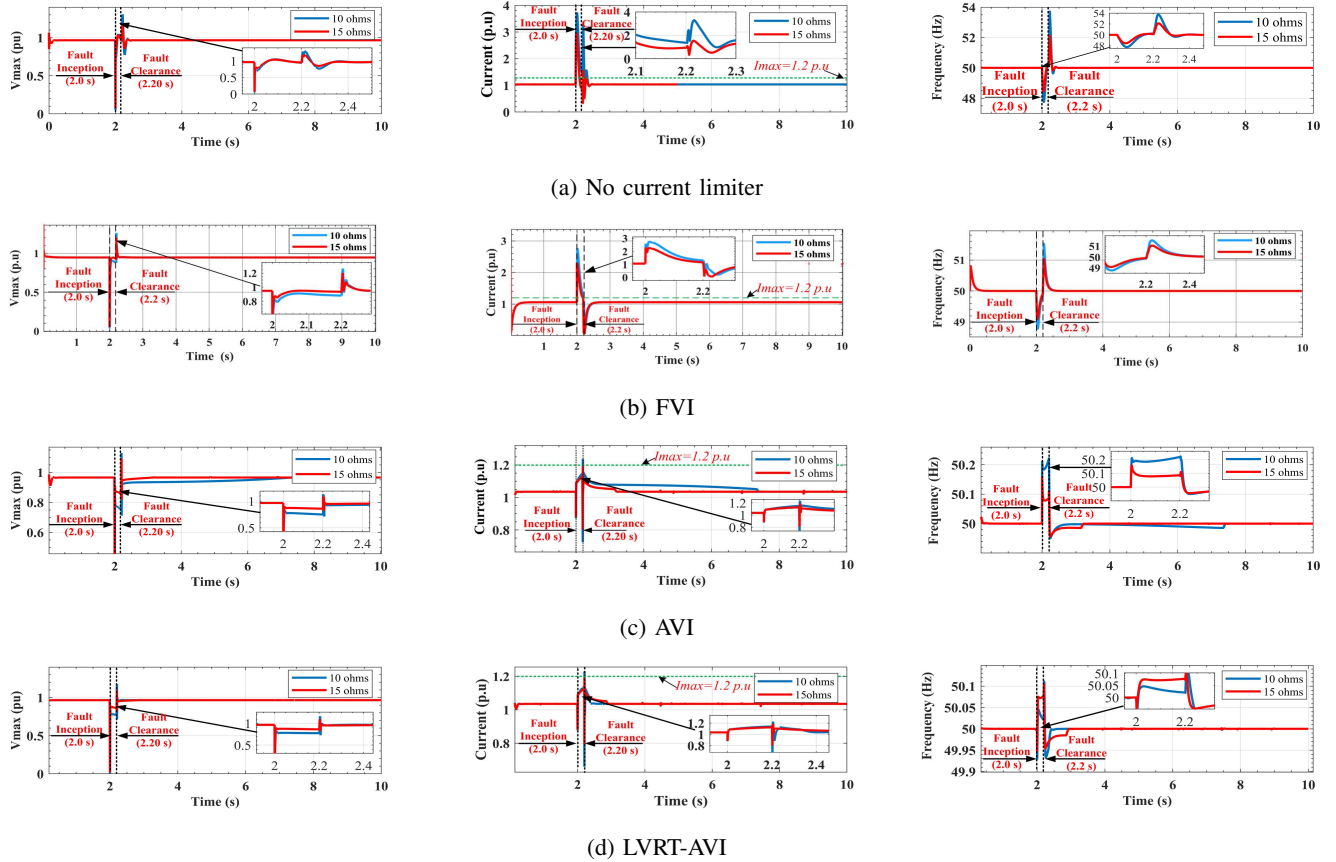


Fig. 6: Comparison of GFM inverter responses under 10 Ω and 15 Ω fault conditions: (a) No current limiter, (b) FVI, (c) AVI, and (d) LVRT-AVI.

causes the non-prioritized component to recover more slowly after fault clearance. The q -axis priority limiter showed the longest recovery time since the active-current component was more restricted during the fault. In comparison, the magnitude limiter maintained a more balanced current allocation and achieved faster recovery, with recovery times of 0.40 s and 0.55 s for the 10 Ω and 15 Ω faults, respectively. In contrast, the d - and q -axis priority-based methods offer greater

flexibility for active- and reactive-power control during faults, respectively, at the expense of relatively higher recovery times.

B. Case Study of GFM Inverter With Indirect Current Limiters

The parameters chosen for the GFM Inverter are shown in Table II. The investigated indirect current-limiting strategies FVI, AVI, and LVRT-AVI exhibit similar fault-current limiting capability but differ considerably in their transient recovery, as

TABLE III: Performance Comparison

Type	Method	Fault (Ω)	I_{peak} (p.u.)	Reduction (%)	Recovery time (s)
GFL	No current limiter	10	2.350	–	0.60
	Magnitude-based limiter	10	1.190	49.36	0.40
	Priority-based limiter (d-axis)	10	1.197	49.06	0.50
	Priority-based limiter (q-axis)	10	1.192	49.28	0.60
	No current limiter	15	2.035	–	0.50
	Magnitude-based limiter	15	1.190	41.52	0.55
	Priority-based limiter (d-axis)	15	1.197	41.18	0.62
	Priority-based limiter (q-axis)	15	1.210	40.54	0.70
GFM	No current limiter	10	3.740	–	0.45
	FVI	10	2.750	38.37	0.60
	AVI	10	1.230	67.11	5.20
	LVRT-AVI	10	1.220	67.38	0.80
	No current limiter	15	2.940	–	0.31
	FVI	15	2.310	21.43	0.50
	AVI	15	1.190	59.52	1.20
	LVRT-AVI	15	1.180	59.86	0.30

shown in Fig. 6 and Table III. The FVI strategy reduces the fault current by 38.37% for the 10 Ω fault and 21.43% for the 15 Ω fault. However, it does not guarantee that the fault current will remain below 1.2 pu. Since the virtual impedance is fixed from the initial stage, it also causes a voltage drop during normal operation. This affects the inverter voltage even before a fault occurs. Therefore, FVI is not suitable for maintaining normal operating conditions. Hence, the AVI strategy is preferred, as it introduces the virtual impedance only when needed during the fault. The AVI strategy reduced the peak fault current by 67.11% and 59.52% for 10 Ω and 15 Ω respectively, whereas for the same fault impedances the LVRT-AVI achieved slightly higher reductions of 67.38% and 59.86% respectively. In addition, the LVRT-AVI reduced the recovery time from 5.2 s to 0.8 s for the 10 Ω fault and from 1.2 s to 0.3 s for the 15 Ω fault as shown in Table III. The recovery time depends on the dynamic response of the AVI after fault clearance. During the fault, the virtual impedance increases to limit the current. After fault clearance, it is gradually reduced as the current returns to normal. This change causes a short transient in the inverter voltage and current. Hence, the recovery time depends on how quickly the virtual impedance and current return to their normal values. Overall, LVRT-AVI achieves effective current limiting with faster post-fault recovery than AVI.

IV. CONCLUSION

This study presented a comparative evaluation of current-limiting strategies for grid-following (GFL) and grid-forming (GFM) inverters under balanced three-phase fault conditions. The results show that the effectiveness of a limiter depends on the inverter control and its response during severe faults. For the GFL inverter, direct current-limiting methods with anti-windup successfully restricted the current to 1.2 p.u. Among the tested methods, the magnitude limiter achieved the highest fault-current reduction. The priority-based limiting methods also effectively limited the fault current while providing the flexibility to prioritize active or reactive power injection during faults according to the desired fault ride-through objective. However, the priority-based methods exhibited a relatively higher recovery time after fault clearance compared with the

magnitude limiter. The application of current limiting caused controller saturation and integrator windup during severe faults, leading to post-fault current overshoots. The use of anti-windup compensation reduced the effect of windup and suppressed post-fault current overshoots, resulting in smoother recovery. This shows that anti-windup is important for improving the fault ride-through performance of GFL inverters. For the GFM inverter, AVI reduced the fault current but resulted in slower recovery. The LVRT-AVI strategy achieves lower peak currents and faster recovery than AVI alone by injecting reactive power to support the PCC voltage during sags while simultaneously maintaining the inverter current within the specified limit. For both GFL and GFM inverters, reducing the fault impedance from 15 Ω to 10 Ω resulted in higher fault currents. Hence, greater fault-current reduction was required to maintain the current within the specified limit. The recovery time also increased with lower fault impedance. The results highlight the need to consider both current suppression and post-fault recovery when selecting current-limiting strategies. The future work focuses on the asymmetrical faults under a wide range of operating conditions with detailed analysis on inverter stability and critical clearing time.

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