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PLL-Synchronized PWM Rectifier: Cascaded In-Loop Low-Pass Filtering Approaches

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***Abstract*—Amplitude normalization schemes (ANSs) are essential for making PLL dynamics independent of grid amplitude - a critical feature for the stable control of grid-connected power converters. This article presents a comparative analysis of recently proposed low-pass filter (LPF)-based ANS-PLLs and introduces an improved demodulation-based PLL (dPLL) featuring an LPF in the feedforward path. Through small-signal modeling and the symmetric optimum method, we establish that while these architectures share similar open-loop characteristics, existing PLLs require a significantly higher LPF cut-off frequency to achieve an equivalent phase margin. This necessary compromise inherently degrades frequency tracking and harmonic robustness. The proposed dPLL simplifies implementation with one fewer tuning gain while maintaining real-time compatible computational complexity. Additionally, numerical phase-plane analysis demonstrates the global convergence of the dPLL under a wide initial phase estimation error range $(-\pi, \pi)$. Experimental validation on an AC-DC PWM rectifier confirms the superior performance of the proposed method in reducing source current harmonic distortion across diverse operating conditions.**

***Index Terms*—PLL, Amplitude Normalization, Filtering**

I. Introduction

POWER electronic converters (PECs), such as the AC-DC PWM rectifier, play a central role in linking loads to the power grid [1], [2], a task that depends heavily on accurate, real-time grid information. Within the PEC control structure, a phase-locked loop (PLL) acts as the key feedback mechanism, enabling stable operation that adapts to grid frequency variations [3]. The synchronous reference frame PLL (SRF-PLL) [4] remains the foundational and most widely adopted approach for three-phase PECs. Its phase detector (PD) converts stationary grid voltage signals into a rotating reference frame, where the amplitude-dependent q-axis component is processed through a proportional-integral (PI) loop filter (LF) and a voltage-controlled oscillator (VCO) (an integrator in the digital domain) to achieve phase locking. As a second-order system, the SRF-PLL exhibits well-known dynamic behaviour: the PI LF introduces a free integrator that ensures zero steady-state phase error under step changes in frequency, but this same integrator inherently creates a trade-off between transient response speed and disturbance rejection. Increasing the LF bandwidth improves tracking speed, yet at the same time reduces robustness to harmonics and grid noise, making the SRF-PLL not well suited to the increasingly polluted conditions of modern distribution networks.

Modern distribution networks are often affected by phase unbalance, harmonic distortion [5], and abrupt voltage magnitude variations due to grid faults, all of which significantly impair phase-locking accuracy. As a result, extensive research has focused on pre-loop filtering, where disturbance mitigation is handled by a signal-conditioning stage placed ahead of the PD, allowing the main loop dynamics to remain unchanged while suppressing specific frequency components. Among these approaches, the second-order generalized integrator (SOGI) [6] and its various variants act as orthogonal signal generators (OSGs), providing both band-pass filtering and quadrature signal generation [7]. Delayed signal cancellation (DSC) operators offer a computationally simple, though memory-intensive, alternative, removing selected harmonic orders through cascaded cancellation stages [8], [9]. DSC-based techniques can operate in either frequency-adaptive or fixed-frequency modes [10]. Adaptive notch filters (ANFs) dynamically track and suppress individual disturbance frequencies, making them particularly effective under grid frequency deviations [11]. The enhanced PLL (EPLL) integrates a self-tuning sinusoidal estimator capable of adaptively tracking amplitude, frequency, and phase simultaneously [12]. While these methods and the wider pre-filtering literature each address specific weaknesses of the basic SRF-PLL, they often share a common limitation: narrowing the pre-filter bandwidth to reject harmonics inevitably introduces additional phase lag and slower transient recovery and vice-versa.

An alternative viewpoint is that filtering does not have to be confined to the pre-loop stage; similar harmonic attenuation can be achieved by embedding low-pass or notch filters and their various variants directly within the PLL loop [13]–[16]. Although in-loop filtering directly alters the loop transfer function and therefore requires careful stability consideration, it enables tighter integration between filtering and control dynamics and supports more systematic tuning strategies. Additionally, pre-filtered PLLs are often tuned by obtaining their in-loop equivalent transfer function.

The performance limits of a PLL are fundamentally linked to its loop type, defined by the number of open-loop integrators in the forward path. A type-1 loop (with a single integrator) can track constant phase without error but exhibits steady-state error under constant frequency offsets. A type-2 loop

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(two integrators, as in the SRF-PLL with its PI LF and VCO) removes steady-state errors for step frequency changes, though it inherits the bandwidth-disturbance trade-off described earlier. A type-3 loop introduces an additional integrator, enabling error-free tracking of frequency ramps, but at the cost of significantly reduced stability margins [17]. In this context, the quasi-type-1 PLL [18] offers a practical compromise: by replacing the PI LF with a proportional controller, it behaves internally as a type-1 loop while recovering type-2 closed-loop characteristics through structural design. This simplifies tuning to a single gain parameter and eases the phase-bandwidth trade-off associated with the SRF-PLL, while preserving the robustness advantages of a lower-order filter.

For grid-connected applications, another key requirement is decoupling loop dynamics from variations in grid voltage amplitude, which is essential for fault-tolerant PEC operation. Amplitude normalization schemes (ANSs) address this by making the effective PD gain independent of amplitude. Common implementations include direct division by the estimated amplitude [19], the atan2-based demodulation PLL (dPLL) [18], the double-sine PLL (sPLL) [20], and the half-tangent PLL (hPLL) [21]. While amplitude normalization is beneficial in maintaining consistent loop gain, it introduces nonlinear effects that complicate stability. Division-based and trigonometric ANSs exhibit nonlinear gain behaviour that leads to multiple equilibrium points, only some of which correspond to the desired locked condition. As a result, assessing global convergence and identifying the basin of attraction requires nonlinear analysis beyond the standard small-signal methods applied to SRF-PLL variants. Within this group, the dPLL based on the atan2 function stands out for its clean normalization: it directly computes phase from the d-q components without needing an amplitude estimate, removing the extra tuning parameter required in division-based approaches. This independence from amplitude estimation, combined with the proportional LF of the quasi-type-1 structure, makes the dPLL well suited for in-loop LPF enhancement. Despite the wide range of ANS-based PLLs reported in the literature, a clear gap remains: there is still no rigorous and fair comparison that evaluates these architectures under consistent conditions. Existing studies typically rely on different tuning approaches, making it difficult to distinguish true structural benefits from differences caused by tuning choices. A benchmarking framework based on matched phase margins and crossover frequencies is therefore needed to reveal their actual performance differences. This article addresses that gap.

Motivated by these considerations, we propose a modified dPLL with a cascaded LPF in the feedforward (FF) path, effectively extending the quasi-type-1 structure to attenuate higher-frequency harmonics while preserving simplicity. Using small-signal modelling together with the symmetric optimum (SO) tuning method — ensuring all candidates share identical phase margins and crossover frequencies — we present the first systematic comparison of three existing ANS-PLLs [18], [20], [21] with the proposed dPLL. The results show that, under fair tuning, the methods are equivalent in their open-loop small-signal behaviour, yet the proposed dPLL achieves improved harmonic rejection by operating with a significantly lower LPF cut-off frequency at the same phase margin, thereby enhancing frequency tracking robustness. Furthermore, the modular nature of the proposed structure allows straightforward integration with pre-loop filtering techniques such as SOGI, DSC, or ANF, complementing the in-loop LPF. Experimental validation on an AC-DC PWM rectifier confirms the improved performance of the proposed approach in reducing source current harmonic distortion under a range of operating conditions.

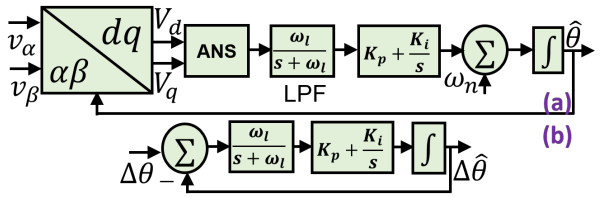


Fig. 1: LPF-Based ANS PLL: (a) Block diagram, (b): SSM.

The main contributions are as follows. First, the development of a modified dPLL with a cascaded LPF-based FF path, including small-signal modelling, phase-plane analysis for global stability and convergence, and a symmetric-optimum tuning framework. Second, a rigorous comparative study of the proposed dPLL and three existing ANS-based PLLs using a consistent benchmarking approach. Third, experimental validation on an AC-DC PWM rectifier, demonstrating clear improvements in harmonic distortion reduction and dynamic performance across diverse operating scenarios.

II. LPF-BASED THREE-PHASE PLLS

Generic block diagram and small-signal model (SSM) of the ANS-based PLL with in-loop LPF is shown in Fig 1. Outputs of the PD are given by for $\theta_e = \theta - \hat{\theta}$:

$$V_d = V\cos(\theta_e), V_q = -V\sin(\theta_e), \tag{1}$$

where amplitude and phase are denoted by V and θ with $\hat{}$ indicates estimated value. As the open-loop transfer function (OLTF) of this PLL has a pair of non-zero pole and zero, which makes the symmetric optimum (SO) method [22] a suitable gain tuning choice. For time-domain tuning for this transfer function, see [23]. Accordingly, optimal PLL parameters are:

$$k_p = \omega_c, k_i = \omega_c^2/b, \omega_l = b\omega_c, b > 0 \tag{2}$$

where ω_c is the desired cross-over frequency and b corresponds to $1+\sqrt{2}$ for a 45° phase margin (PM), which is often suggested for the PLL in the existing literature. Additionally, ω_c within $110 \leq \omega_c \leq 140$ rad/s is also recommended. Then, by taking the middle point, i.e., ω_c = 125 rad/s, results in the sPLL paramaters as: $k_p = 125; k_i = 6472.1, \omega_l = 301.7767$.

A. Proposed FF LPF-based Demodulation PLL

Conventional demodulation PLL [18] uses a proportional gain-only LF; however, it is a second-order system in the closed-loop same as the SRF-PLL using PI LF. This article modifies the conventional dPLL by adding another LPF in the FF path as shown in Fig. 2, whose PD outputs are given by:

$$V_d \approx V\cos(\phi), V_q \approx V\sin(\phi), \tag{3}$$

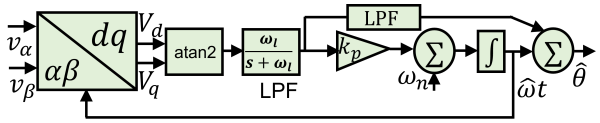


Fig. 2: Block diagram of the proposed PLL with FF LPF term.

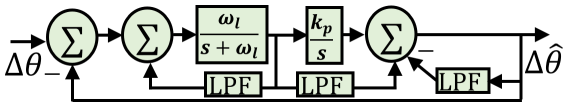


Fig. 3: Small-signal model of the proposed dPLL.

where the phase angle ϕ is estimated as $\hat{\phi} = \text{atan2}\,(V_q, V_d)$, where atan2 which also acts as an ANS and it provides intrinsic, parameter-independent normalization. The proposed modification is inspired by interleaved converter architecture, where multiple parallel lower-rated converters can achieve higher efficiency than a single full-rated stage. The proposed PLL does likewise, allowing a lower cutoff-frequency LPF and lower proportional gain in the LF, resulting in a suitable trade-off between dynamic performance and disturbance rejection. Note that setting the FF LPF to 1 recovers the PLL in [18].

1) Gain Tuning: The SSM of the proposed PLL is given in Fig. 3, from which the OLTF can be obtained as:

$$\mathcal{G}_{OL}(s) = \mathcal{K}\,(s+\omega_z)\,/\left(s^2\,(s+\omega_p)\right), \tag{4}$$

where $\mathcal{K} = 1/(\omega_l^2 + k_p\omega_l)$, $\omega_z = k_p\omega_l^2\mathcal{K}$, and $\omega_p = 2\omega_l$. According to SO, the optimal set of tuning parameters are:

$$\mathcal{K} = b\omega_c^2, \omega_p = b\omega_c, \omega_z = \omega_c/b. \tag{5}$$

From Eq. (5), tuning gains can be obtained as:

$$\omega_l = 0.5b\omega_c, k_p = (\omega_c\omega_l)\,/(b\omega_l - \omega_c)\,. \tag{6}$$

Here the same values for b and ω_c as that of the sPLL are selected to ensure fair gain tuning. Setting identical ω_l for both

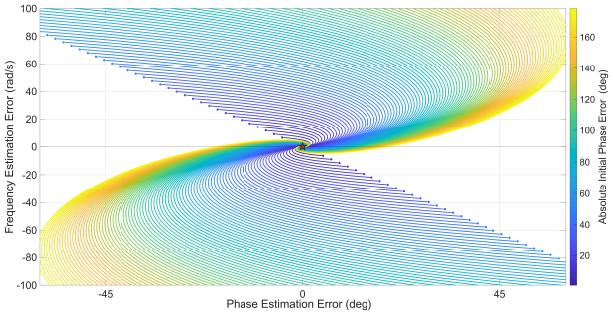


Fig. 4: Phase-plane plot of the proposed dPLL.

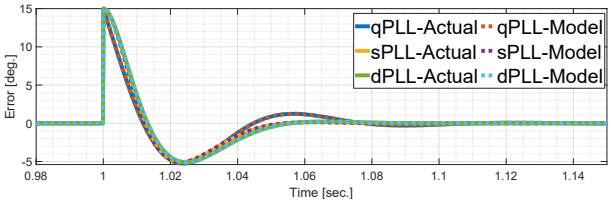


Fig. 5: SSM validation of the sPLL, qPLL and dPLL.

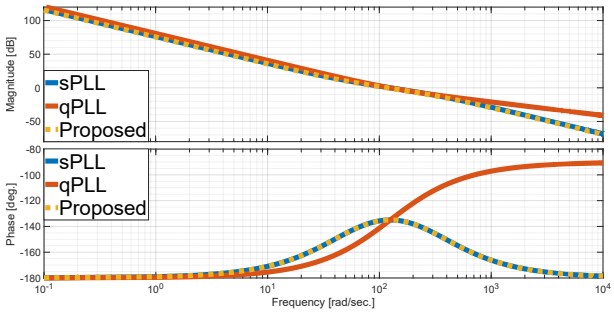


Fig. 6: Open-loop Bode magnitude and phase plots of the sPLL, qPLL and dPLL with paramaters listed in Sec. II.

the feedback and FF is a deliberate design choice to reduce tuning degrees of freedom; the two filters nonetheless serve distinct roles in the system operation. The selected gains are: $k_p = 78.8253; \omega_l = 150.8883$.

2) Global Stabaility Assessment: The results above were developed under small-signal conditions (i.e. $\theta_e \approx 0$). For global analysis, phase-plane portraits are popular tools obtained either numerically or analytically through a large-signal model (LSM). Because developing an analytical LSM is complex, we used a numerical approach. Figure. 4 shows that for initial phase errors within the range $(-\pi, \pi)$ as shown in the heatmap, the dPLL frequency and phase estimation errors converge to the point (0,0), establishing the global stability.

B. Small Signal Model Validation and Comparative Analysis

For subsequent analysis, we included the qPLL [18], upon which the proposed method is developed. The qPLL is tuned with $k_p = 125$ and $\omega_l = 88.39$ to achieve the same 45° PM. To validate the developed SSMs (Figs. 1(b) and 3) and the proposed tuning approach, the proposed PLL as well as the qPLL and SPLL were subjected to a $+15^\circ$ phase jump; the MATLAB/Simulink simulation results for phase estimation errors are shown in Fig. 5. Results obtained from the original nonlinear models for the sPLL and dPLL in Figs. 1(a) and 2 are presented alongside outputs from the linear models in Figs. 1(b) and 3. The same has been conducted for the qPLL following the figures presented in [18, Figs. 5 and 6]. The findings show that the developped SSMs for sPLL and dPLL accurately predict the behavior of the PLLs, validating the models. Additionally, both PLLs exhibit very similar time-domain behavior, demonstrating the consistency between the two methods. The qPLL closely follows the sPLL and dPLL, as all were tuned using the same phase PM; however, it has slightly worse transient performance (i.e., settling time) than the sPLL and dPLL. Bode magnitude plots of the PLLs are provided in Fig. 6. It demonstrates that, with fair tuning, the selected methods have almost identical frequency-domain characteristics. The LPF of the proposed dPLL has a much lower cut-off frequency than that of the sPLL, and it lies between those of the qPLL and the sPLL, offering a favorable trade-off. Any phase unbalance and/or harmonic in the grid will cause high-frequency oscillation at the PD output of the PLLs. As the sPLL has a much higher cut-off frequency, its

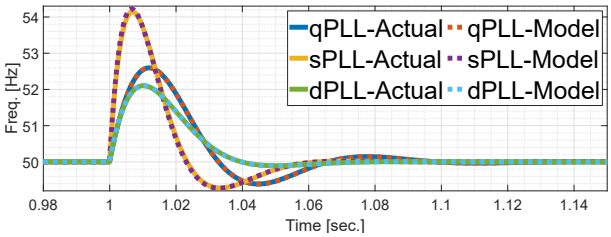


Fig. 7: PLL SSM validation: frequency estimation.

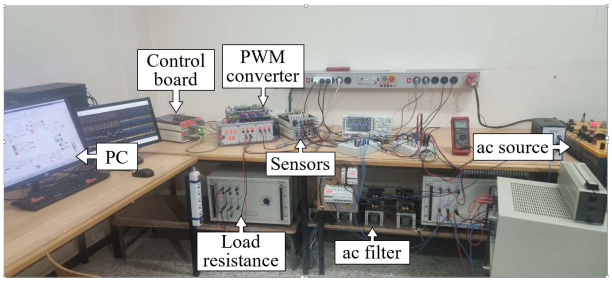


Fig. 8: Active rectifier experimental setup.

frequency tracking performance will be significantly deteriorated compared to the proposed dPLL. Additionally, the PI LF in the sPLL will also slow down its tracking response compared to the dPLL, which uses only a proportional LF. Compared to the proposed dPLL, the conventional qPLL's magnitude response shows lower attenuation of high-frequency components (Fig. 6), resulting in slightly worse performance under grid disturbances. Note that the SSM validation in Fig. 5 is presented only for the phase, following the wider PLL literature. However, this figure does not explain the frequency-estimation dynamics. Therefore, Fig. 7 shows the actual vs. model output for the frequency when the PLLs were subject to the same conditions as in Fig. 5. Results show that despite similar time-domain phase-estimation performance, the PLLs have very different frequency-estimation behavior. The proposed dPLL has the fastest error convergence with the lowest peak overshoot, followed by the qPLL and sPLL. This can be explained by the tuning of these PLLs: the proposed dPLL has the lowest proportional gain value, followed by the qPLL and sPLL, which is reflected in the peak-overshoot values (higher proportional gain correlates with higher overshoot). This is also reflected in the experimental results in the next section.

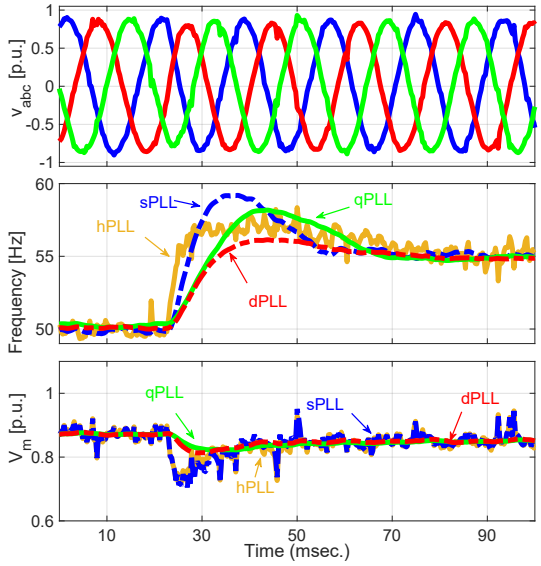


Fig. 9: Experimental results for frequency step change (T1).

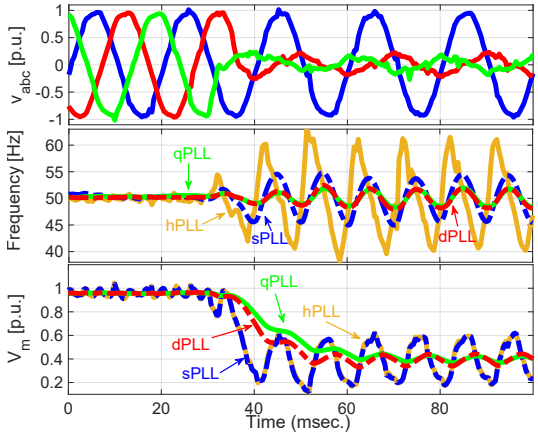


Fig. 10: Experimental results for 80% asymmetric sags (T2).

III. Experimental Results and Discussions

This section presents experimental validation using a 10 kHz PWM-controlled three-phase AC/DC rectifier setup with RL filter, as shown in Fig. 8. The AC-side filter (R and L), DC-link capacitor (C), and load (R_L) parameters are 1.5Ω, 19.4mH, 2.5mF, and 110Ω, respectively. The PLLs and control system were implemented with a 100μs sampling time-step in Matlab/Simulink, utilizing TI C2000 F28379D microcontroller for rapid control prototyping. For comparison, we selected the qPLL and sPLL with gains reported in Sec. II together with the hPLL [21]. Since this PLL does not have an in-loop LPF, we used the same gains ($k_p = 184, k_i = 8464$) as specified by the authors in [21]. For the reported experiments, the nominal phase voltage is 55V (r.m.s) and the frequency is 50Hz. To validate the methods, five challenging cases are considered, which are: (**T1**) +10% Frequency step; (**T2**) 80% Asymmetrical voltage sag in phase a and b; (**T3**) +90° Phase jump; (**T4**) Harmonic distortion (10% THD); (**T5**) Weak grid (SCR = 1.35) with Id_{ref} step change from 0.4 p.u. to 0.65 p.u. Tests results are shown in Figs. 9-13. The top figure shows the grid voltage, the middle figure shows the estimated grid frequency, and the bottom figure shows the estimated amplitude. As shown in Fig. 9 (T1), the proposed dPLL achieves the fastest frequency estimation (lowest settling time) and lowest overshoot under a frequency step change, followed by the hPLL, sPLL, and qPLL. This is also aligned with SSM validation in Fig. 7, where the dPLL had the fastest convergence with the lowest overshoot. Despite identical tuning, the dPLL and qPLL produce significantly smoother amplitude estimates than the sPLL and hPLL. This is a critical advantage since these estimates directly generate switching signals within the vector control framework. Regarding robustness to phase

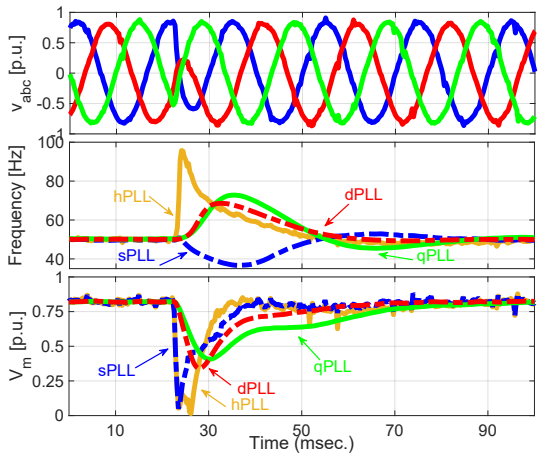


Fig. 11: Experimental results for 90° phase change (T3).

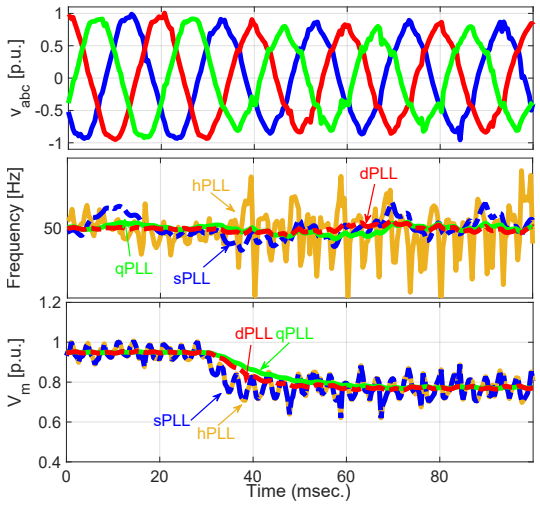


Fig. 12: Experimental results for 10% distortion (T4).

unbalance in Fig. 10 (T2), all tested PLLs exhibit steady-state oscillations as they lack sequence component extraction. However, the dPLL demonstrates the fastest convergence for amplitude estimation, followed by the qPLL. Results in Fig. 11 show that a 90° phase jump causes large overshoots in all PLLs. The proposed dPLL and its predecessor, the qPLL, have similar overshoots for both amplitude and frequency estimation, though the dPLL achieves faster convergence. Notably, both the sPLL and hPLL show very high overshoot in amplitude estimation. Results for T4 in Fig. 12 show that grid harmonic distortion causes noticeable oscillations in the amplitude estimated by the sPLL and hPLL, while the qPLL and dPLL remain more resilient. The dPLL in particular achieves faster amplitude convergence than the qPLL. Finally, the weak grid scenario in Fig. 13 shows a similar trend where the sPLL and hPLL are more sensitive, whereas the qPLL and dPLL are more robust. The comparative settling times validate the benchmarking framework, as the sPLL, qPLL, and dPLL were tuned with approximately identical phase margins and bandwidths. To further validate these results, Figs. 14 and 15, show the line current spectrum for two challenging cases: T2 and T4. Note that the THD is calculated over a 10-cycle window; however, only two-cycle data is presented for visual clarity. In T2, an asymmetrical sag causes large distortion in the current drawn by the rectifier under sPLL (7.97%) and hPLL (8.78%) control. Both exceed the IEEE 519-2022 limit of 5%. This standard is easily met by the proposed method, whose THD is roughly 25% lower than the next best method, the qPLL. Results in T4 show that all PLLs are resilient to a 10% voltage THD, though the proposed method achieves the lowest current THD. These THD results correlate with the Bode plot in Fig. 6, which shows the dPLL attenuates high-order harmonics more than the qPLL; the qPLL achieved the second-best THD reduction in Figs. 14 and 15.

All results above used vector control with a fixed DC-link. A final test applied a +10% step from 200 V to 220 V to show the adaptability of the PLL methods. Results are shown in Figs. 16-19 for qPLL, sPLL, hPLL, and the proposed dPLL, respectively. The results show that estimated frequency and voltage magnitude for the sPLL and hPLL are significantly noisier

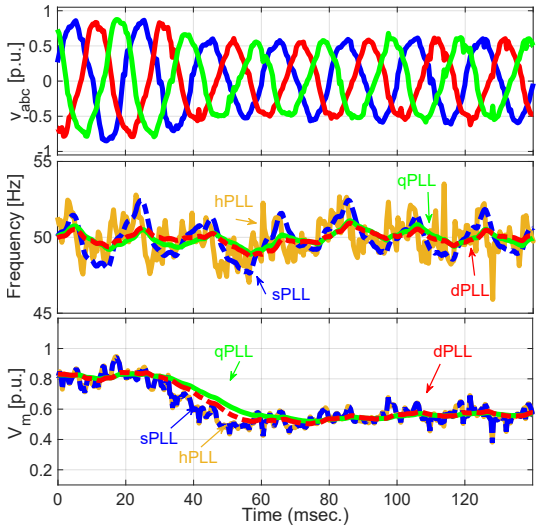
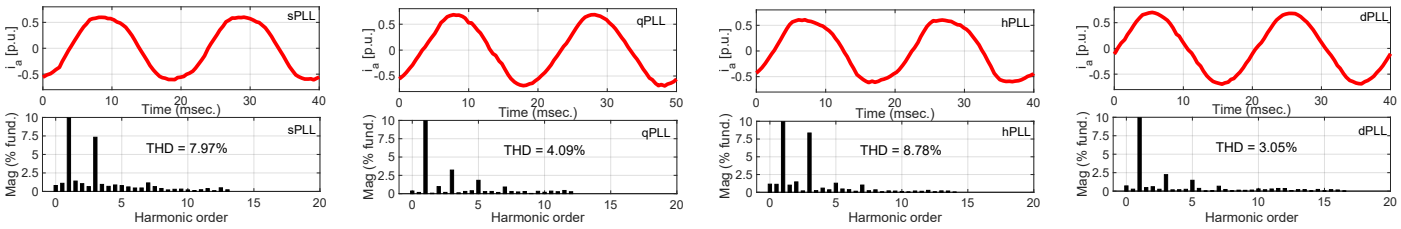


Fig. 13: Experimental results for weak grid condition (T5).

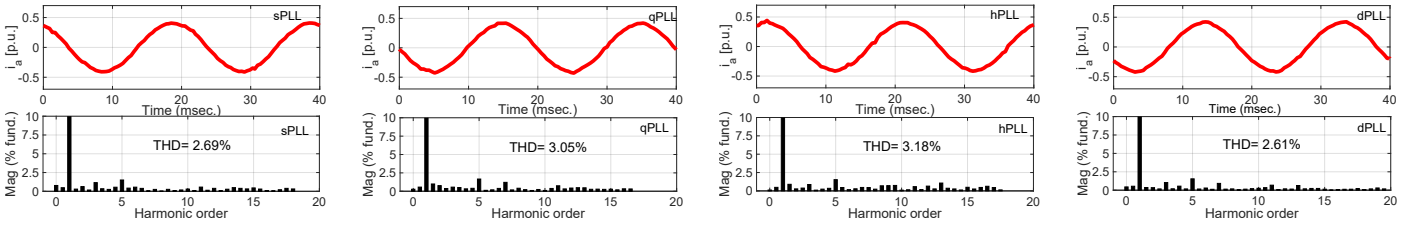
and more fluctuating than for QT1-type PLLs (qPLL and the proposed dPLL), which is consistent with prior findings that QT1-type PLLs are more robust to harmonics despite identical tuning. In terms of DC-link settling time, the proposed dPLL is fastest at approximately 100 ms, compared with approximately 110 ms for the qPLL and sPLL and approximately 120 ms for the hPLL. This demonstrates that the proposed dPLL achieves improved harmonic robustness without sacrificing dynamic response, thanks to the placement of the low-pass filter in both feedback and feedforward paths.

Finally, computational complexity was assessed by measuring the average execution times. While the dPLL (6.4 μs) and qPLL (6.3 μs) incur higher overhead than the sPLL (2.4 μs) and hPLL (2.4 μs) due to the atan2 function, the difference is negligible relative to the 100 μs sampling period. Over 90% of the control cycle remains available for auxiliary tasks, validating the dPLL for real-time implementation. A qualtitaive summary of the methods are given in Tab. I.



(a) sPLL (THD - 7.97%) (b) qPLL (THD - 4.09%) (c) hPLL (THD - 8.78%) (d) dPLL (THD - 3.05%)

Fig. 14: AC-line current spectra of phase *a* under T2 (80% asymmetric sag): top - phase current; bottom - FFT.



(a) sPLL (THD - 2.69%) (b) qPLL (THD - 3.05%) (c) hPLL (THD - 3.18%) (d) dPLL (THD - 2.61%)

Fig. 15: AC-line current spectra of phase *a* under T4 (10% THD): top - phase current; bottom - FFT.

TABLE I: QUALITATIVE SUMMARY OF THE METHODS.

Method	LF	In-Loop LPF	Tuning Gains	Dynamic Performance	Harmonic Robustness
sPLL [20]	PI	✓	3	Good	Moderate
hPLL [21]	PI	✗	2	Good	Low
qPLL [18]	P	✓	2	Good	Good
dPLL	P	✓	2	Very Good	Very Good

IV. CONCLUSION

This article presented a comparative study of ANS-based PLLs and a proposed modified demodulation PLL incorporating an LPF in the feedforward path. This architectural shift enables significant performance improvements while utilizing lower tuning gains. Through the SO method, it was established that although existing LPF-based ANS-PLLs share similar small-signal open-loop characteristics, they require significantly higher LPF cut-off frequencies to achieve the same phase margin as the proposed design. This necessary compromise inherently degrades frequency tracking and harmonic robustness. Experimental validation using an AC-DC PWM rectifier substantiated these findings that the proposed modification offers a more robust solution for high-precision control in grid-connected PECs. Future work will include adding a sequence-extraction technique to the proposed method to make it suitable for a double-decoupled vector control framework.

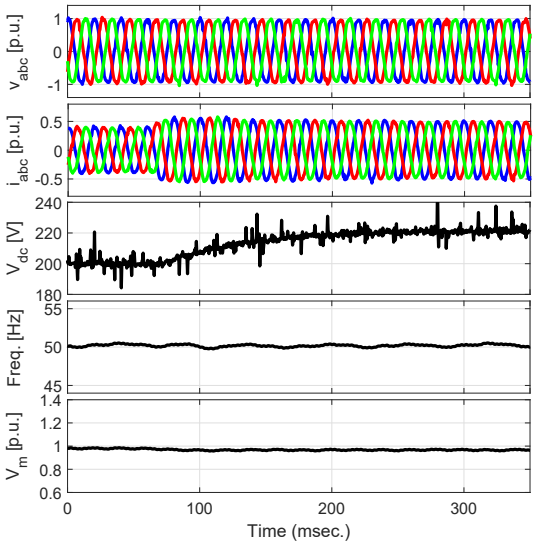


Fig. 16: DC-link voltage change under qPLL-based control.

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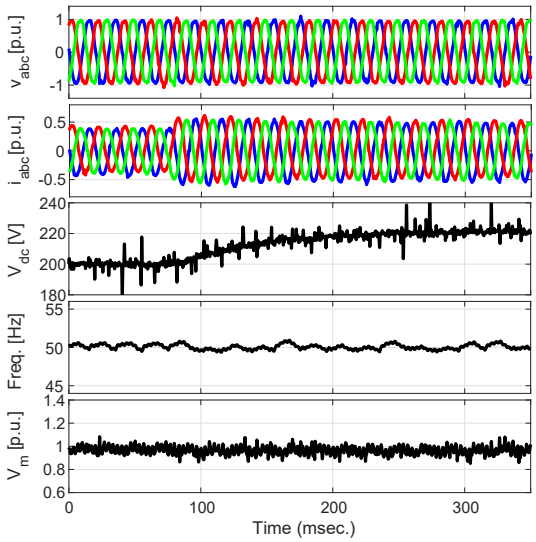

Fig. 17: DC-link voltage change under sPLL-based control.

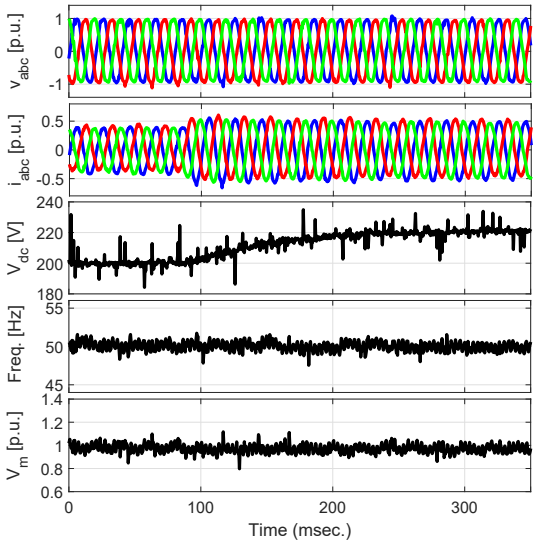

Fig. 18: DC-link voltage change under hPLL-based control.

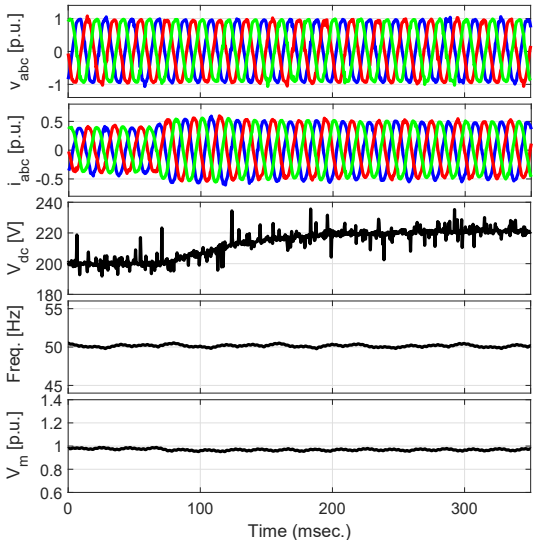

Fig. 19: DC-link voltage change under dPLL-based control.

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