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# Equivalence-Based Tuning of ADRC- and SRF-PLLs for Grid-Connected Systems

Hafiz Ahmed, *Senior Member, IEEE,* Adel Rahoui, and Saif Ahmad

***Abstract*—AC-DC power conversion is fundamental to grid-connected consumer technology, where phase-locked loops (PLLs) are typically used for real-time parameter estimation. This paper demonstrates that a linear active disturbance rejection control (ADRC)-based PLL is dynamically equivalent to a conventional synchronous reference frame (SRF)-PLL equipped with an in-loop low-pass filter (LPF). This equivalence is established analytically through small-signal modeling and parameter mapping. Using bandwidth-parameterization-based tuning for the ADRC-PLL, equivalent proportional-integral (PI) control gains and LPF cut-off frequency for the SRF-PLL are derived analytically, while the inverse mapping–including cases based on the symmetric optimum method–is performed numerically by solving a third-order polynomial equation. Theoretical findings are validated through experimental results using a grid-connected AC-DC PWM rectifier. When tuned under equivalent conditions, both PLLs exhibit nearly identical dynamic performance. Experimental tests under non-ideal grid conditions reveal a performance trade-off: the ADRC-PLL offers greater robustness to high-order harmonics, whereas the SRF-PLL demonstrates superior performance under low-order distortion and voltage unbalance. These results provide a unified framework linking ADRC and SRF-PLL formulations, supporting the design of advanced PLL architectures that combine the strengths of both approaches.**

***Index Terms*—Active disturbance rejection control, phase-locked loop, extended state observer, PLL tuning.**

## I. Introduction

POWER electronic converters (PECs) are central to modern consumer electronics, interfacing AC grids and consumer loads [1]–[3]. As PECs are inherently nonlinear, their switching dynamics introduce harmonic distortion and grid disturbances. Accurate estimation of grid parameters is therefore essential to maintain power quality. The literature identifies three principal real-time estimation algorithms: [a] **Phase-Locked Loops (PLLs)**, the most common method, which use a phase detector and loop filter to estimate frequency and phase in the synchronous reference frame [4]; [b] **Frequency-Locked Loops (FLLs)**, which estimate grid frequency directly in the stationary reference frame [5]; and [c] **Regression-Based Methods**, which utilize delay-based transformations to extract frequency as an explicit regressand [6].

The SRF-PLL remains dominant due to its simplicity and compatibility with voltage-oriented control (VOC) in PECs, as illustrated in Fig. 1. However, it faces a critical trade-off: increasing bandwidth improves response speed but degrades disturbance rejection. To address this, various modifications have been proposed, including delayed signal cancellation [7], moving-average filters [8], [9], orthogonal signal generators [10], and phase-lead compensation [11].

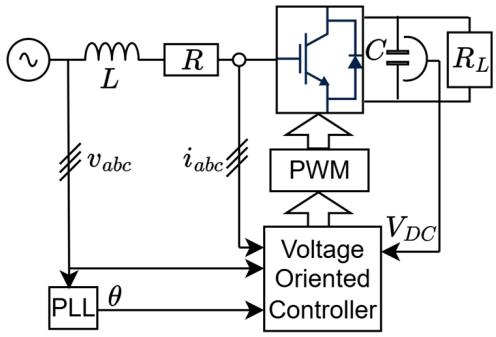


Fig. 1: PWM-controlled grid-connected AC/DC rectifier for consumer electronics application.

Recently, researchers have replaced the PI-type loop filter with an extended state observer (ESO) from the active disturbance rejection control (ADRC) framework [12]. Here, the LF is modeled as a first-order system where a linear ESO estimates and rejects lumped disturbances in real time, while proportional feedback ensures tracking. The ADRC-PLL has gained significant attention for its robustness, mirroring ADRC's broader adoption in power electronics.

While the link between ADRC and PID is known [13], the theoretical connection between ADRC-PLLs and the SRF-PLL remains largely unexplored. Establishing this equivalence is vital for the industrial adoption of ADRC-PLLs, given the current dominance of SRF-PLL practices. Our work bridges this gap by proving the structural equivalence between the linear ADRC-PLL and the conventional SRF-PLL with an in-loop LPF - a common enhancement for noise resilience. This is demonstrated through two primary contributions:

1) **Small-Signal Analysis**: Analytical derivation reveals for the first time that both PLLs can be represented as third-order closed-loop systems with equivalent parameter mappings.
2) **Tuning Equivalence**: Established SRF-PLL tuning rules, such as the symmetric optimum (SO) method [14], are mapped directly to the ADRC-PLL via the numerical solution of a cubic polynomial. This mapping addresses a significant gap in the existing literature.

Experimental validation on a grid-connected PWM rectifier confirms that both PLLs achieve nearly identical transient

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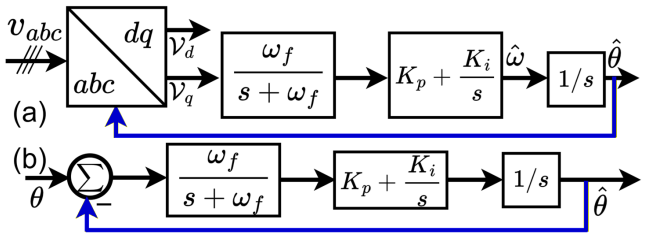



Fig. 2: Conventional SRF-PLL: (a) Block diagram; (b) SSM.

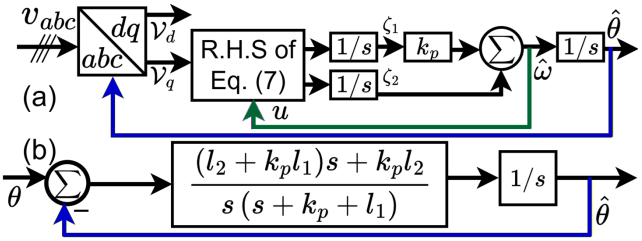



Fig. 3: ADRC-PLL: (a) Block diagram; (b) SSM.

behavior when tuned fairly. Under distorted grid conditions, the SRF-PLL handles low-order harmonics better, whereas the ADRC-PLL shows superior high-frequency noise resilience. This performance gap originates from their distinct tuning philosophies and optimization objectives: the SO method optimizes the phase margin, whereas the ADRC approach maintains a constant phase margin under specific conditions, primarily adjusting the crossover frequency. These findings are vital for advancing ADRC-PLL development. By incorporating targeted low-order harmonic mitigation, the ADRC-PLL can become a robust solution for commercial converters in various energy applications.

The rest of this paper is organized as follows. Section II reviews the SRF-PLL with in-loop LPF. Section III formulates the ADRC-PLL. Section IV derives their equivalence using analytical and numerical approach. Section V presents experimental validation, and Section VI concludes the paper.

## II. SRF-PLL With In-Loop Low-Pass Filter

The block diagram of a conventional three-phase SRF-PLL with an in-loop LPF is shown in Fig. 2(a). The phase detector (PD) outputs are expressed as functions of the actual ($\theta$) and estimated ($\hat{\theta}$) phase as [15]–[17]:

$$\mathcal{V}_d = V_m \cos\tilde{\theta} \approx 1, \mathcal{V}_q = V_m \sin\tilde{\theta} \approx \tilde{\theta}, \tag{1}$$

where $V_m$ is the magnitude and $\tilde{\theta} = \theta - \hat{\theta}$ is the phase error. Assuming $V_m = 1$ p.u. and using small-angle approximations ($\sin\tilde{\theta} \approx \tilde{\theta}$), (1) shows that $\mathcal{V}_q$ represents the instantaneous phase error. In the SRF-PLL, a LF with gains $K_p$ and $K_i$ processes this signal to estimate grid frequency and phase. While effective under ideal conditions, performance degrades with harmonic distortion or noise. To enhance disturbance rejection, an in-loop LPF with cutoff frequency $\omega_f$ is cascaded with the LF, though this increases tuning complexity and reduces transient speed. Based on the small-signal model in Fig. 2(b), the open-loop transfer function (OLTF) is:

$$\mathcal{G}(s) = K_p \omega_f \frac{s + K_i/K_p}{s^2\,(s + \omega_f)}. \tag{2}$$

This third-order system is typically tuned using the symmetric optimum (SO) method [14], which specifies:

$$K_p = \omega_c, K_i = \omega_c^2/b, \omega_f = b\omega_c, \tag{3}$$

where the crossover frequency ($\omega_c$) is the geometric mean of the OLTF corner frequencies, i.e., $\sqrt{\omega_f\,(K_i/K_p)}$, and $b$ is positive scaling parameter. Existing literature recommends a value for $\omega_c$ in the range of $110 \le \omega_c \le 140$ rad/sec. [18], while the value of $b$ can be selected as a function of the desired phase margin (PM) and is given by [14]:

$$\text{PM} = \tan^{-1}((b^2 - 1)/(2b)). \tag{4}$$

According to (4), a value of $b = 1 + \sqrt{2}$ corresponds to a PM $= 45°$, while $b = 2 + \sqrt{3}$ corresponds to a PM $= 60°$. A higher PM leads to a lower peak overshoot and a slower convergence time, while a lower PM results in the opposite.

## III. PLL based on Linear ADRC

ADRC provides an observer-based approach to estimate and reject disturbances in real time. In PLL applications, it replaces the PI loop filter with a linear ESO, eliminating the need for integral action. A proportional controller then ensures zero steady-state phase error. The ADRC-PLL structure is shown in Fig. 3(a) [12]. Its operation is described using the $q$-axis voltage $\mathcal{V}_q$ from (1) and the relation $\hat{\theta} = \hat{\omega}/s$ as:

$$\begin{aligned} \mathcal{V}_q &= \tilde{\theta} = \theta - \frac{\hat{\omega}}{s}, \\ \dot{\mathcal{V}}_q &= -\hat{\omega} + \dot{\theta}. \end{aligned} \tag{5}$$

Equation (5) can be written as a first-order system:

$$\dot{y} = b_0 u + f, \tag{6}$$

where $y = \mathcal{V}_q$ is the measured output, $u = \hat{\omega}$ is the control input, $b_0 = -1$ is the control gain, and $f = \dot{\theta}$ represents the total disturbance. Defining the observer states $x_1 = y$, $x_2 = f$, and estimates $\zeta_1, \zeta_2$, the linear ESO is formulated as [19]:

$$\begin{bmatrix} \dot{\zeta}_1 \\ \zeta_2 \end{bmatrix} = \begin{bmatrix} -l_1 & 1 \\ -l_2 & 0 \end{bmatrix} \begin{bmatrix} \zeta_1 \\ \zeta_2 \end{bmatrix} + \begin{bmatrix} b_0 \\ 0 \end{bmatrix} u + \begin{bmatrix} l_1 \\ l_2 \end{bmatrix} y, \tag{7}$$

$$u = b_0^{-1}\left(-k_p \zeta_1 - \zeta_2\right), \tag{8}$$

where $k_p > 0$ is the controller gain, and $l_1, l_2$ are ESO gains.

### A. Bandwidth-Parameterization-based Tuning

A common tuning method for ADRC systems is bandwidth parameterization (BP) [19], which selects gains as:

$$\begin{aligned} k_p \approx \omega_{\text{CL}} \approx 4/t_{\text{sett.}}, l_1 = 2\omega_{\text{obsv}}, l_2 = \omega_{\text{obsv}}^2, \\ \omega_{\text{obsv}} \approx (2, \ldots, 10) \cdot (\omega_{\text{CL}}), \end{aligned} \tag{9}$$

where $\omega_{\text{CL}}$ and $\omega_{\text{obsv}}$ are the desired closed-loop and observer bandwidth and $t_{\text{sett.}}$ the target settling time.

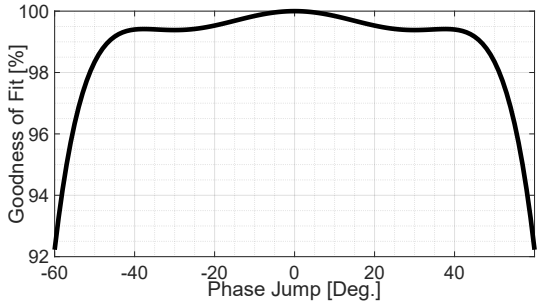
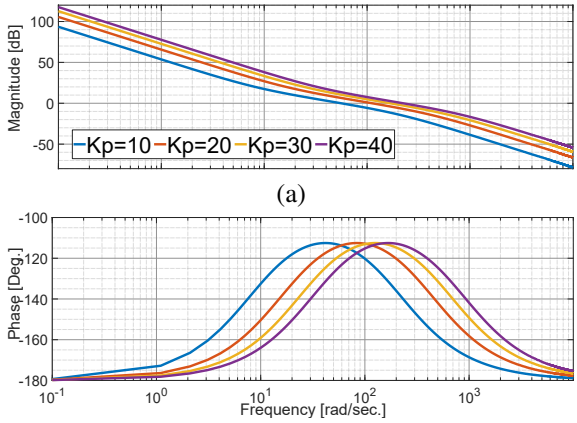



Fig. 4: ADRC-PLL's small-signal model validation result.




(a)

(b)

Fig. 5: OLTF Bode plot of the ADRC-PLL.

### B. Small-Signal Model and Stability Analysis

Following the same approach as in the SRF-PLL, a small-signal model of the ADRC-PLL can be derived, as shown in Fig. 3(b). The OLTF is obtained from (7) and (8) as:

$$G(s) = \frac{\hat{\theta}}{\tilde{\theta}}(s) = \frac{(l_2 + k_p l_1)\, s + k_p l_2}{s^2 (s + k_p + l_1)}. \tag{10}$$

To validate the proposed SSM, we evaluated the phase estimation error for both the actual nonlinear system ($e_a = \theta - \hat{\theta}_{\text{actual}}$) and the linearized model ($e_m = \theta - \hat{\theta}_{\text{model}}$), as shown in Fig. 3(a) and Fig. 3(b), respectively. The model's fidelity was quantified using the mean square error between $e_a$ and $e_m$ across a range of phase jumps. As illustrated in Fig. 4, the SSM maintains an accuracy of over 99% for phase errors up to $\pm 30°$. Beyond this threshold - specifically exceeding $\pm 50°$ - the fitting accuracy declines significantly as the nonlinearities of the PLL structure become dominant.

The corresponding closed-loop transfer function is:

$$C(s) = \frac{(l_2 + k_p l_1)\, s + k_p l_2}{s^3 + (k_p + l_1)\, s^2 + (l_2 + k_p l_1)\, s + k_p l_2}. \tag{11}$$

Poles of the transfer function (11) are:

$$s_1 = -k_p, s_{2,3} = \frac{-l_1 \pm \sqrt{l_1^2 - 4l_2}}{2}. \tag{12}$$

Since all gains are positive by design, the roots possess strictly negative real parts, ensuring closed-loop stability. Notably, the adaptive frequency feedback in the ESO is functionally equivalent to the tracking mechanism of a conventional SRF-PLL. This equivalence ensures that both systems share the same linearized dynamics. Because the roots of the closed-loop transfer function consistently maintain strictly negative real parts, the proposed equivalence-based tuning strategy ensures robust stability margins across both control frameworks.

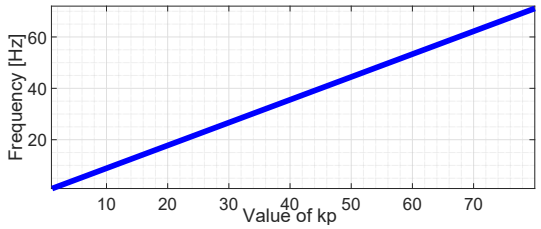



Fig. 6: Gain crossover frequency of the OLTF (10) as a function of the gain $k_p$.

### C. Discrete-Time Implementation

The linear ESO in (7) is not suitable for direct real-time implementation. Consequently, the ESO is discretized using the zero-order-hold method; the resulting formulas are:

$$\begin{aligned} \zeta_1(k+1) &= (1 - l_{1d})\zeta_1(k) + T_s\zeta_2(k) + \\ &\quad b_o T_s u(k) + l_{1d} y(k), \\ \zeta_2(k+1) &= -l_{2d}\zeta_1(k) + \zeta_2(k), \\ u(k) &= b_0^{-1}\left(-k_p\zeta_1(k) - \zeta_2(k)\right), \end{aligned} \tag{13}$$

where $T_s$ is the sampling period, $k$ is the discrete time step, and $l_{1d}$ and $l_{2d}$ are the discrete-time observer gains. These gains are defined as:

$$z = e^{-T_s \omega_{\text{obsv}}}, l_{1d} = 1 - z^2, l_{2d} = T_s^{-1}(1 - z)^2. \tag{14}$$

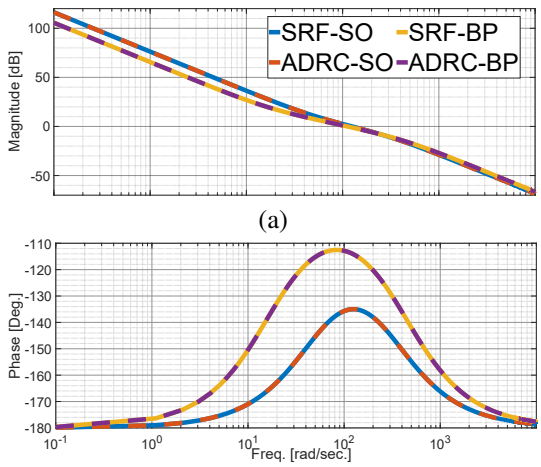
For further details on various discrete-time implementation methods, interested readers may consult [19, Chapter 8].

### D. Comment on ADRC Gain Selection

The ADRC gain $k_p$ (and consequently $l_1, l_2$) directly dictates the settling time. While higher $k_p$ values improve speed, they degrade disturbance rejection. In PLL literature, the open-loop PM is a standard metric for robustness, typically recommended between $30° - 60°$ [14]. Unlike the SRF-PLL, the ADRC-PLL maintains a fixed PM for a constant bandwidth ratio ($\omega_{\text{obsv}}/\omega_{\text{CL}}$). As shown in Fig. 5, $k_p$ shifts the magnitude and frequency response without altering the PM. Therefore, SO tuning method, which optimize for PM, is not directly applicable. Instead, $k_p$ must be selected based on the desired bandwidth. Fig. 6 confirms that the PM remains constant at $\approx 66°$ while the crossover frequency scales linearly with $k_p$, necessitating a balanced choice for optimal performance.

## IV. Equivalence Between the PLLs

The block diagrams of the two PLLs, shown in Figs. 2(a) and 3(a), illustrate their structural differences: one employs an LPF and a PI controller, whereas the other utilizes an ESO with a proportional controller. However, their SSMs (Figs. 2(b) and 3(b)) reveal that both are locally third-order systems with an equal number of tuning gains. Therefore, this section




(a)

(b)

Fig. 7: Bode plots of the OLTFs in (2) and (10) using gains tuned using the same baseline: (a) Magnitude; (b) Phase.

establishes the conditions under which the two PLLs are small-signal dynamically equivalent, specifically with respect to the linearized output measurement $\mathcal{V}_q$ via (1). To this end, we rewrite the ADRC-PLL's OLTF (10) as:

$$G(s) = (l_2 + k_p l_1)\,\frac{s + \frac{k_p l_2}{l_2 + k_p l_1}}{s^2\,(s + k_p + l_1)}. \tag{15}$$

By comparing the transfer function (2) with the one in (15), the following equality conditions are obtained:

$$K_p \omega_f = l_2 + k_p l_1, \tag{16}$$

$$K_i / K_p = \frac{k_p l_2}{l_2 + k_p l_1}, \tag{17}$$

$$\omega_f = k_p + l_1. \tag{18}$$

By solving (16)-(18), we can obtain the gain values of one PLL as a function of the other PLL. These gain values will establish the dynamic equivalence between the two PLLs. Therefore, two case studies are considered in the following:

### A. ADRC to SRF-PLL Gain Equivalence

First, let's consider the case where the parameter values of the ADRC-PLL are known, for example, through the BP tuning formulas given in (9). By substituting the value of $\omega_f$ from (18) into (16), we can obtain the gain $K_p$ from ADRC-PLL gains. Then, by substituting the expression for $K_p$ into (17), we can obtain the formula for $K_i$. The formuals for these gains are summarized below:

$$K_p = \frac{l_2 + k_p l_1}{k_p + l_1}, K_i = \frac{k_p l_2}{k_p + l_1}, \omega_f = k_p + l_1. \tag{19}$$

### B. SRF to ADRC-PLL Gain Equivalence

When the gains of the conventional SRF-PLL are known, calculating the equivalent ADRC-PLL gains isn't as simple. To demonstrate this, we start with (18), from which we obtain:

$$l_1 = \omega_f - k_p. \tag{20}$$

TABLE I: EQUIVALENT PLL GAINS SUMMARY.

| Method | Conventional | ADRC |
|---|---|---|
| Symmetric Optimum<br>PM $= 45°$, $\omega_c = 125$,<br>$b = 1 + \sqrt{2}$ | $\omega_l = 301.8$,<br>$K_p = \omega_c$,<br>$K_i = 6742.1$ | $k_p = 125.1$,<br>$l_1 = 176.8$,<br>$l_2 = 15624.1$ |
| Bandwidth<br>Parameterization<br>$\omega_{\text{obsv}} = 200$ | $\omega_f = 420$,<br>$K_p = 114.3$,<br>$K_i = 1904.8$ | $k_p = 20$,<br>$l_1 = 400$,<br>$l_2 = 40000$ |

Substituting this value into (16) yields the following:

$$l_2 = \omega_f\,(K_p - k_p) + k_p^2. \tag{21}$$

Next, by substituting the values of $l_1$ and $l_2$ into (17) and simplifying further, we can obtain the following:

$$k_p^3 - \omega_f k_p^2 + \omega_f K_p k_p - \omega_f K_i = 0. \tag{22}$$

The normalized version of the cubic equation (22) is:

$$x^3 - x^2 + \frac{K_p}{\omega_f} x - \frac{K_i}{\omega_f^2} = 0, k_p = \omega_f x. \tag{23}$$

An analytical solution to (23) can be complex or nonphysical, so we solve it numerically via Newton-Raphson. For physical consistency all gains must be positive; from (20) this requires $0 < k_p < \omega_f$, restricting the normalized search interval for $x$ to $(0, 1)$. If multiple real roots exist, we choose the root in $x \in (0, 1)$ that also yields $l_2 > 0$ via (21). Once $k_p$ is found, the remaining gains are computed from (20)-(21).

### C. Comparative Analysis

Gain formulas provided in eqs. (19)-(23) demonstrate that two PLLs are dynamically equivalent in the small-signal sense when tuned under the same baseline, despite their different structures. The tuning approach significantly impacts the PLL's dynamic behavior. The ADRC-PLL, when tuned using BP, maintains a fixed PM regardless of the gain value $k_p$, with only the crossover frequency changing. In contrast, the SO method allows the PM to vary as function of the gains $\omega_f$, $K_p$, and $K_i$. To validate the dynamic equivalence, two cases were examined:

- **Case 1 (SO-Dominant)**: The conventional PLL is tuned via (3) for a $45°$ PM, with the ADRC-PLL gains derived using the equivalent formulas (20)–(23).
- **Case 2 (BP Dominant)**: The ADRC-PLL is tuned using the BP method (9) with $t_{\text{sett.}} = 0.2$ and $\omega_{\text{obsv}} = 10\omega_{\text{CL}}$. The conventional PLL gains are then calculated via the equivalent mapping in (19).

Tuning parameters are selected to yield comparable crossover frequencies for a fair performance comparison, with gain values listed in Table I. The OLTF Bode plots in Fig. 7 confirm nearly identical frequency-domain characteristics, validating the gain equivalence. Notably, BP tuning results in a $\approx 66°$ PM, whereas SO tuning targets $45°$, explaining the phase plot differences in Fig. 7(b). While both PLLs exhibit similar magnitude behavior after the crossover frequency, the SO method shows a higher magnitude in the lower frequency region. This suggests a faster response but reduced

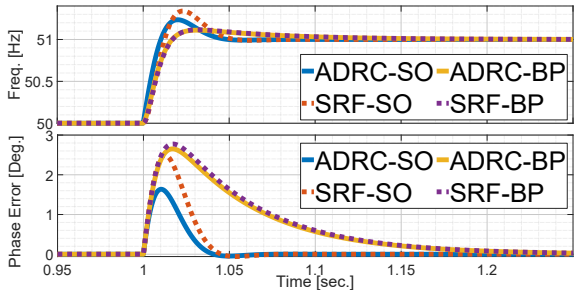



Fig. 8: Simulation verification of the gains in Table I: (top) estimated frequency and (bottom) phase estimation error.

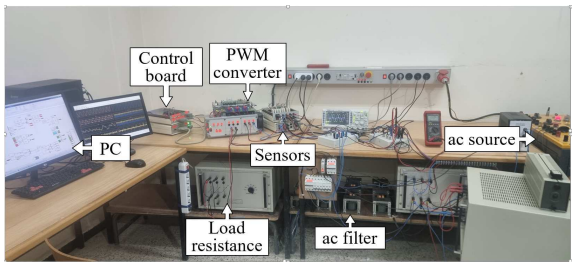



Fig. 9: Active rectifier experimental setup.

low-frequency disturbance rejection compared to BP tuning, highlighting the fundamental trade-off between speed and robustness dictated by the chosen tuning method. To validate the equivalence studies and the tuned gains, a simulation was conducted where the grid frequency suddenly experienced a $+1$ Hz change. The corresponding frequency and phase estimation errors are shown in Fig. 8. In this figure, ADRC tuned via BP (ADRC-BP) and SO (ADRC-SO) and SRF tuned via BP (SRF-BP) and SO (SRF-SO) are compared. The top panel shows the estimated frequency via SRF (Fig. 2(a)) and ADRC (Fig. 3(a)), while the bottom panel shows the phase estimation error, i.e., $\theta - \hat{\theta}$. Results indicate that BP tuning yields performance parity between both PLLs. However, despite the numerical equivalence (Sec. IV-B), the ADRC-PLL outperforms the conventional PLL with lower overshoot and faster convergence. This superiority stems from a significantly higher proportional gain ($k_p = 125.1$ vs. 20.0), which, per (9), directly reduces settling time and accelerates transient response.

Although the ADRC-PLL with ESO-equivalent tuning performed well in this specific scenario, it may have a deteriorating effect in more challenging situations, such as phase jumps, harmonics, or measurement offsets.

## V. Experimental Results and Discussions

This section presents experimental validation using a 10 kHz PWM-controlled three-phase AC/DC rectifier setup, as shown in Fig. 9. The hardware configuration follows the circuit diagram presented in Fig. 1. The AC-side filter ($R$ and $L$), DC-link capacitor ($C$), and load ($R_L$) parameters are $1.5\Omega$, 19.4mH, 2.5mF,and $110\Omega$, respectively. The PLLs and control system were implemented with a $100\mu$s sampling time-step in Matlab/Simulink, utilizing TI C2000 F28379D microcontroller for rapid control prototyping. Code profiling shows

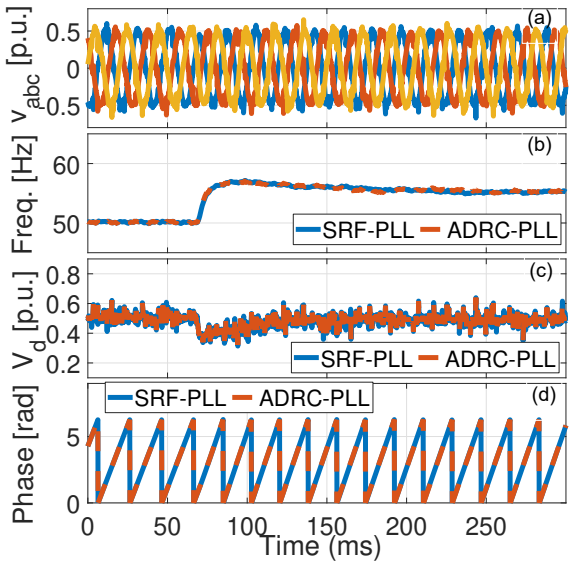



Fig. 10: Performance comparison of the SRF-PLL and ADRC-PLL under $+10\%$ frequency step (T1): (a) three-phase voltages; (b) estimated frequency; (c) estimated amplitude; and (d) estimated phase.

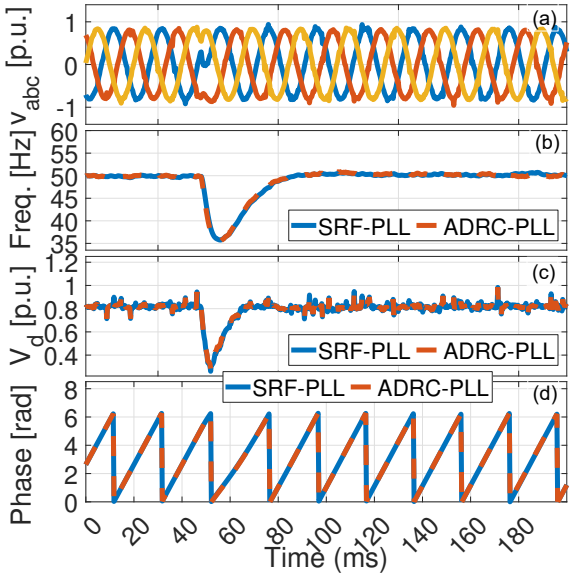



Fig. 11: Performance comparison of the SRF-PLL and ADRC-PLL under $+30^\circ$ phase jump (T2): (a) three-phase voltages; (b) estimated frequency; (c) estimated amplitude; and (d) estimated phase.

that the average execution time is $2.04\mu$s for the SRF-PLL and $2.23\mu$s for the ADRC-PLL, indicating that the ADRC-PLL has roughly 10% higher real-time complexity. For all experiments reported here, the nominal phase voltage is 55V (r.m.s) and the frequency is 50Hz. This comparison focuses strictly on conventional and ADRC-based SRF-PLLs to analyze their equivalent gain tuning. However, the proposed tuning results are directly applicable to other filtered PLL architectures, such as DSC, MAF, OSG, and PLC. To validate the methods, following challenging test cases are considered: (T1) $10\%$

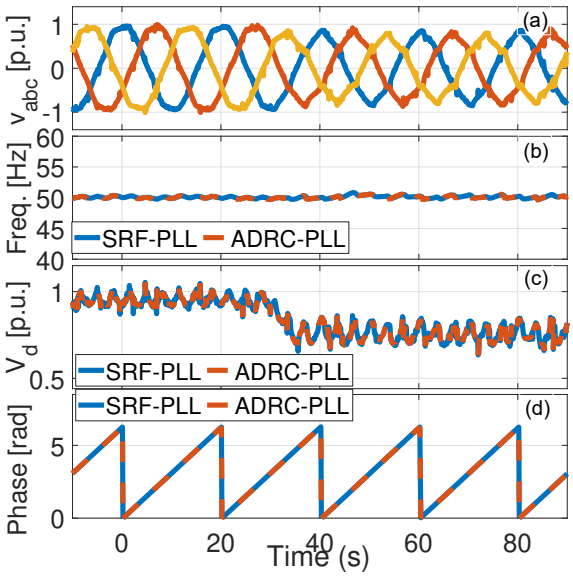



Fig. 12: Performance comparison of the SRF-PLL and ADCR-PLL under distorted grid voltages with 10% THD (T3): (a) three-phase voltages; (b) estimated frequency; (c) estimated amplitude; and (d) estimated phase.

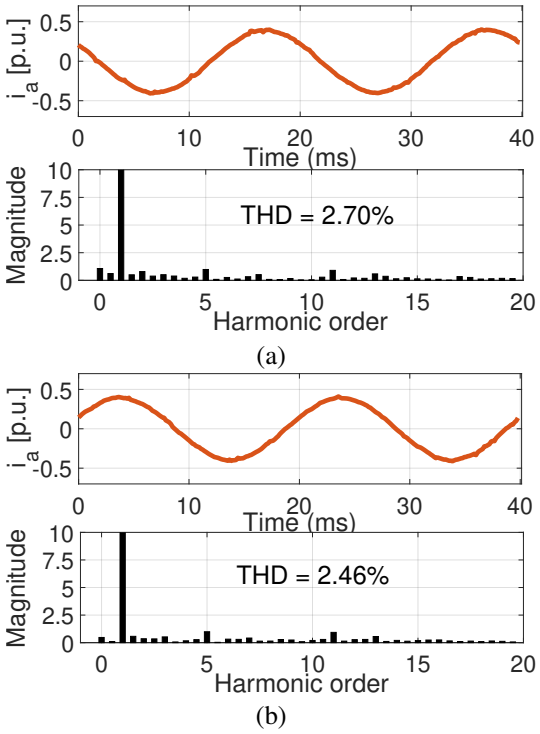



Fig. 13: The AC-line current spectrum for T3: (a) SRF-PLL-based VOC and (b) ADCR-PLL-based VOC.

frequency step change; (T2) $+30^\circ$ phase jump; (T3) Distorted grid with $10\%$ THD; (T4) $50\%$ Asymmetrical voltage sag in phase $a$ and $b$; and (T5) $10\%$ DC offset in phase $a$.

Results for T1 are shown in Fig. 10. Both PLLs exhibit nearly identical dynamic performance for frequency, amplitude, and phase estimation (Figs. 10(b)-(d)), experimentally validating the proposed equivalence-based tuning. Because the

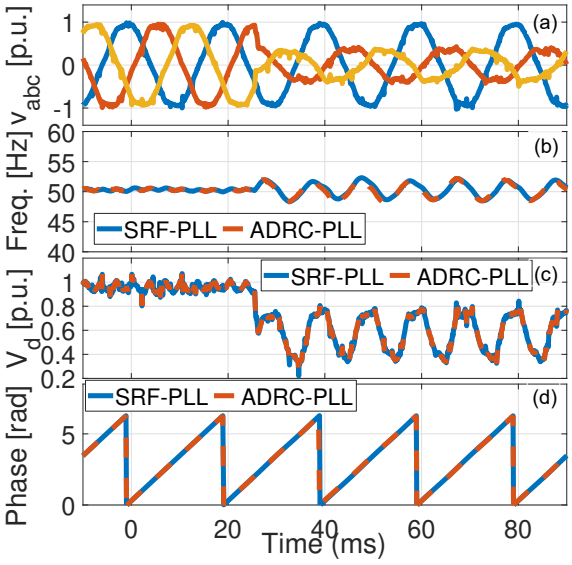



Fig. 14: Performance comparison of the SRF-PLL and ADRC-PLL under $50\%$ sag in phases $a$ and $b$ (T4): (a) three-phase voltages; (b) estimated frequency; (c) estimated amplitude; and (d) estimated phase.

tuning uses a nominal small-signal model and the voltage is near nominal, both PLLs are expected to perform identically. In T2, a similar near-ideal voltage profile is used with a phase jump; Fig. 11(b)-(d) shows both PLLs have identical dynamic responses that match the tuning goal. T3 introduces harmonic disturbance to test robustness against unmodeled effects. Fig. 12(b)-(d) shows equivalent dynamic performance, as in T1 and T2. Notably, identical time-domain performance does not guarantee identical frequency-domain performance (measured via THD), as a linear approximation was used to model the PD output, $\mathcal{V}_q$, for the PLLs. This distinction is evident in test case T3 (Fig. 13); while both methods show nearly identical dynamic responses, the ADRC-PLL achieves a $\approx$9% lower grid current THD, demonstrating superior robustness against harmonics compared to its conventional counterpart. Case T4 (Figs. 14 and 15) considers an unbalanced grid. Because unbalanced voltages induce double-frequency oscillations in $\mathcal{V}_q$, the small-angle approximation becomes less accurate. Consequently, the estimated frequency and phase exhibit steady-state oscillations around nominal values, indicating degraded performance. Surprisingly, unlike Case T3, the ADRC-PLL shows a $\approx$3% increase in grid current THD. This suggests the ADRC-PLL is sensitive to unmodeled low-order harmonics - such as 100 Hz oscillations caused by a 50 Hz unbalance - while remaining robust to high-order harmonics. The profiles in Fig. 15 confirm this sensitivity. Although these three-phase PLLs were not designed for unbalance, they can be adapted by applying a sequence extraction technique, such as a second-order generalized integrator (SOGI) [10], as a pre-filter. The current harmonic profile for Test T4 using a SOGI pre-filter (with tuning gain $k_s = \sqrt{2}$) is shown in Fig. 16. Results show that while the SOGI pre-filter immediately reduces the THD by roughly half, the ADRC method still maintains a slightly higher THD than the SRF-PLL. In the final test

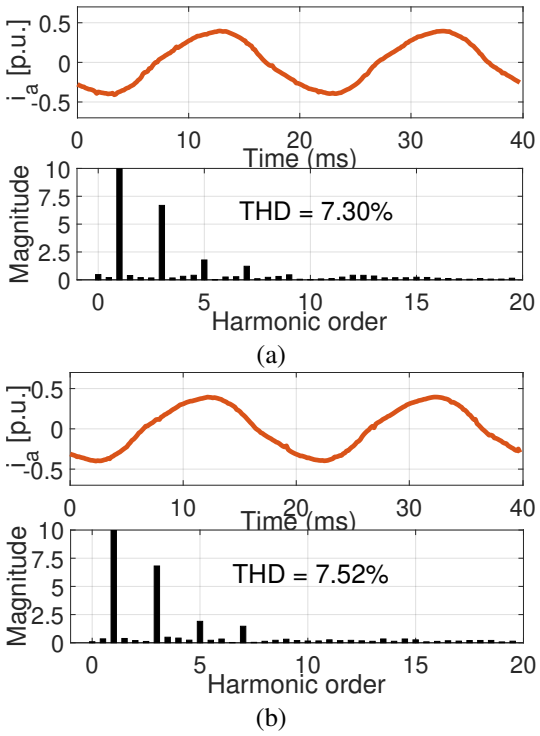



Fig. 15: The AC-line current spectrum for T4: (a) SRF-PLL-based VOC and (b) ADRC-PLL-based VOC.

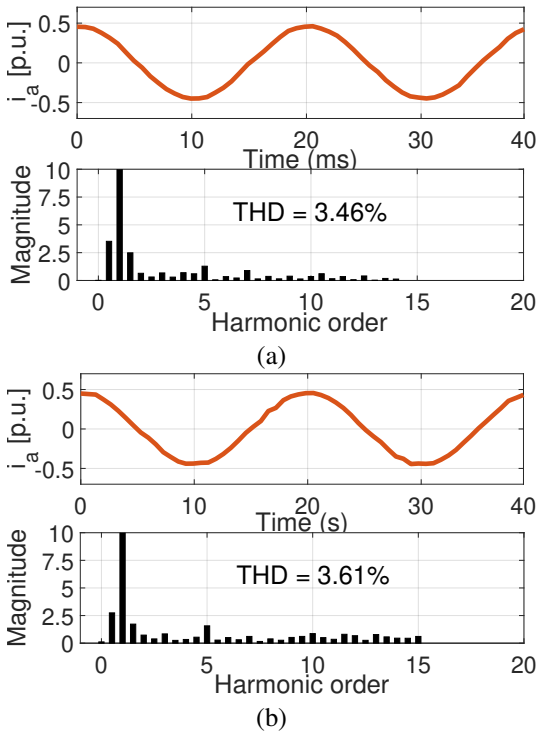



Fig. 16: The AC-line current spectrum for T4: (a) SOGI-SRF-PLL-based VOC and (b) SOGI-ADRC-PLL-based VOC.

(Figs. 17 and 18), a +10% DC offset is added to phase *a* to simulate common signal conversion issue. The results show nearly identical responses with only a +1% performance improvement in THD by the ADRC, further validating the proposed equivalent tuning.

The five test cases successfully validate the dynamic equivalence between the ADRC-PLL and an SRF-PLL utilizing an in-loop LPF. Using objective benchmarks (e.g., crossover frequency) for fair gain tuning, both PLLs achieve nearly identical dynamic performance. However, the results reveal a trade-off: the conventional method is more resilient to voltage unbalance, while the ADRC-PLL is more resilient to harmonics.

## VI. Conclusion

This paper establishes the analytical and experimental equivalence between the linear ESO-based ADRC-PLL and the conventional SRF-PLL with an in-loop LPF. Both systems share identical third-order dynamics and achieve matching performance through explicit gain-mapping relations derived here for the first time. This allows the SO method and BP-based tuning to be interchanged across frameworks. Experimental validation confirms that under matched tuning, both PLLs deliver virtually identical transient behavior. Performance divergence occurs only under non-ideal grid conditions: the SRF-PLL offers better immunity to low-order unbalance, while the ADRC-PLL demonstrates superior resilience to high-frequency noise. These differences originate from their distinct tuning philosophies; the SO method optimizes phase margin, whereas the ADRC approach maintains a constant

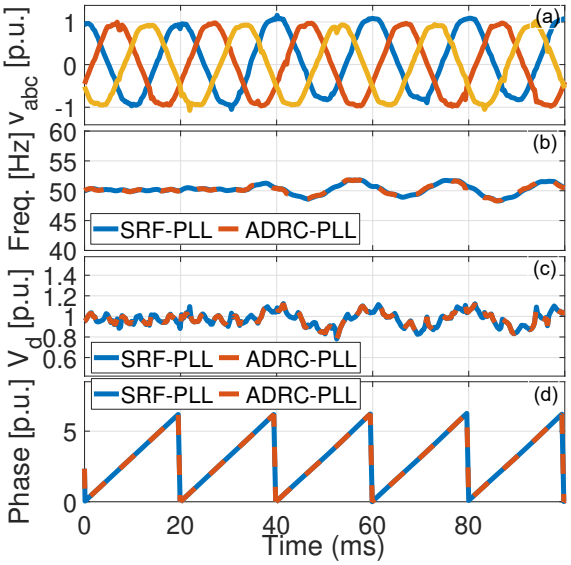



Fig. 17: Performance comparison of the SRF-PLL and ADRC-PLL under +10% DC offset in phase *a* (T5): (a) three-phase voltages; (b) estimated frequency; (c) estimated amplitude; and (d) estimated phase.

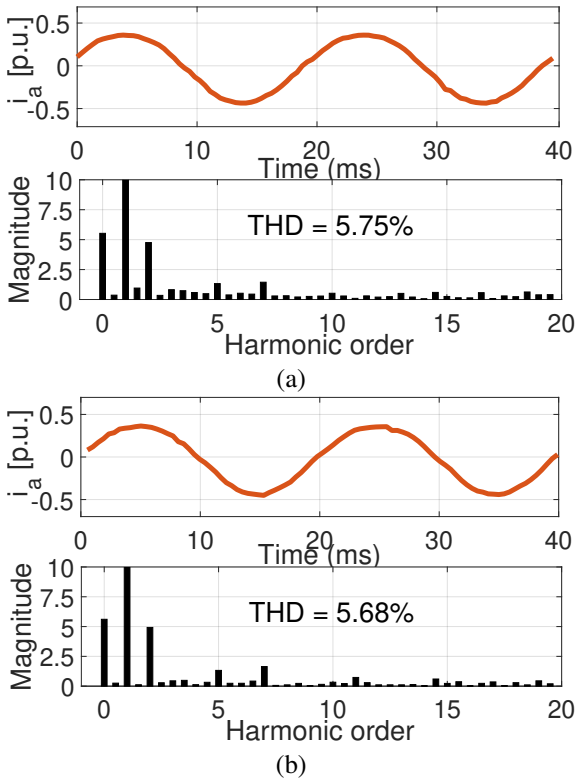



Fig. 18: The AC-line current spectrum for T5 in phase $a$: (a) SRF-PLL-based VOC and (b) ADRC-PLL-based VOC.

phase margin while scaling the crossover frequency. These results provide a unified theoretical foundation for ADRC and SRF-based synchronization, facilitating the industrial adoption of advanced ADRC schemes in grid-connected PECs. Future research may extend this equivalence to higher-order or cascaded ESO structures for enhanced robustness in complex environments.

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