
Proceedings Paper:
Ball, E.A. and David Joseph, S. (Accepted: 2026) A Quadrature Sampling RF Travelling Wave ADC architecture for QAM digitisation at mmWave. In: 2026 IEEE International Mediterranean Conference on Communications and Networking (MeditCom). IEEE MeditCom 2026, 06-09 Jul 2026, Cagliari, Italy. Institute of Electrical and Electronics Engineers (IEEE). (In Press)

A Quadrature Sampling RF Travelling Wave ADC Architecture for QAM Digitisation at mmWave

Edward A. Ball
School of Electrical & Electronic Engineering
The University of Sheffield
Sheffield, United Kingdom
e.a.ball@sheffield.ac.uk

Sumin David Joseph
School of Electrical & Electronic Engineering
The University of Sheffield
Sheffield, United Kingdom
s.d.joseph@sheffield.ac.uk

***Abstract*—We introduce a new concept in analogue to digital conversion: the Quadrature Sampling RF Travelling Wave ADC (QSTW-ADC). This samples an RF signal in quadrature at a mmWave carrier (or a high IF). The concept shares aspects of conventional data conversion (flash and pipeline) but now using RF circuit techniques to realise detection circuits that may work at much higher frequencies and are suitable for integration on MMIC processes. The proposed architecture is scalable, by cascading modules, to achieve a desired SNDR or dynamic range for a scenario. The architecture could be split between technologies, to make best use of materials (e.g. RF on GaAs and digital on CMOS). Simulations of a 28 GHz trial GaAs MMIC show an analogue front-end bandwidth of 750 MHz for the ADC. QSTW-ADC numerical models predict an RMS EVM of 5.9 % for 64QAM. The ADC has a simulated ENOB of 4.2 bits for I and 4.2 bits for Q. Suitability for multicarrier modulation is also considered. Initial lab test results from a PCB emulator confirm key system concepts.**

Keywords—Analogue to digital conversion, millimetre wave circuits, signal processing, software defined radio.

I. Introduction

Analogue to digital converters (ADCs) are a vital enabling component of modern software defined radio (SDR). SDR will remain pivotal and technology-defining in 6G systems and beyond. Today, there are many types of ADCs available, optimised for various use-cases, including [1]: flash, successive approximation, pipelined, dual-slope, delta-sigma, time to digital, etc. Of these, the most appropriate for high performance SDR RX applications are generally those having the fastest sampling rates and the highest analogue bandwidths. RX SDR implementations therefore usually focus on the Flash ADC and the Pipeline ADC.

The Flash ADC is a well-known and intuitive architecture, using a resistive reference divider chain and set of associated fast comparators and latches to digitise the analogue signal. However, the distribution of signals and design of the resistive divider chain limits the maximum number of comparison levels (hence, bits) practical at speed. Most flash ADCs are around 8 bits, though they are amongst the fastest. Artificial intelligence is incorporated into a Flash ADC, with 4 to 10-bit resolution and sampling at up to 3.6 GS/s in [2], with a reduced set of comparator stages. Interleaving multiple ADCs can improve the sampling speed, with a recent example at 32 GS/s reported in [3]. In [4] a 5-bit Flash ADC operating at 18.5 GS/s in 22nm FD-SOI CMOS is described, without needing a low-valued resistive reference ladder.

The pipeline ADC is also an important high-speed digitisation architecture, using a cascade architecture to partially digitise the input in stages. Very fast pipeline ADCs have now been reported, such as a 1.125 GHz bandwidth (BW) example requiring 9 GS/s [5]. A 0.18 µm SiGe BiCMOS 12-bit 2 GS/s example is reported in [6]. In [7] a hybrid voltage-time domain approach is presented, with recent voltage-time domain pipeline ADCs reported operating to beyond 10 GS/s. In [8] a self-calibration method is presented for an 11-bit pipelined ADC, using digitally controlled capacitors. In [9] a 12-bit 10 GS/s pipelined ADC using pre-sampling is presented in 28 nm CMOS. In [10] a continuous-time pipelined ADC sampling at 6.4 GS/s and using time interleaving to achieving a BW of 1 GHz is introduced.

More generally, high performance commercial RF ADCs currently available are now often incorporated into a system on chip, or module, such as an FPGA. An example is the Intel Stratix 10 FPGA with a 10 bits 64 GS/s ADC and 36 GHz analogue BW. However, these systems are often very power intensive and not suitable for low power mobile systems. Separate ADCs operating at mmWave carriers are rare. The EV10AS940 [11] is a unique example, sampling at 12.8 GS/s and accepting an RF input up to 40 GHz.

An ADC is usually considered separately from the RF strip in a receiver and designed from an analogue electronics viewpoint. Therefore, it is interesting to consider how the data conversion process may be realised differently and more directly incorporating the function within the RF RX chain. It is also interesting to consider how the ADC could benefit from incorporating RF design techniques and signal processing techniques in its realisation. As a further stimulus for our work, operation of ADCs at much higher carrier frequencies than currently seen, such as high mmWave, and designed for modulation formats relevant to these carriers, becomes a useful step. At present, SDRs working at high mmWave frequencies usually require a downconverting mixer and local oscillator stage, before a conventional commercial ADC.

At high mmWave frequencies, channels are often sparse and rely on direct line of sight signals. This means that simpler single carrier modulation schemes (e.g. QAM) are highly relevant and allow a simplification in transceiver design, compared to microwave OFDM and similar technologies.

From the above perspectives, we propose in this paper our new concept, initial analysis and results of a *Quadrature Sampling RF Travelling Wave ADC* (QSTW-ADC) that uses aspects of RF design and digital signal processing to provide a direct digitisation approach for RX mmWave QAM signals. We present the expected symbol constellation performance of a proposed 16 tap QSTW-ADC for various QAM constellation orders.

This work was supported by U.K. Research and Innovation (UKRI) Future Leaders Fellowship under Grant UKRI1064.

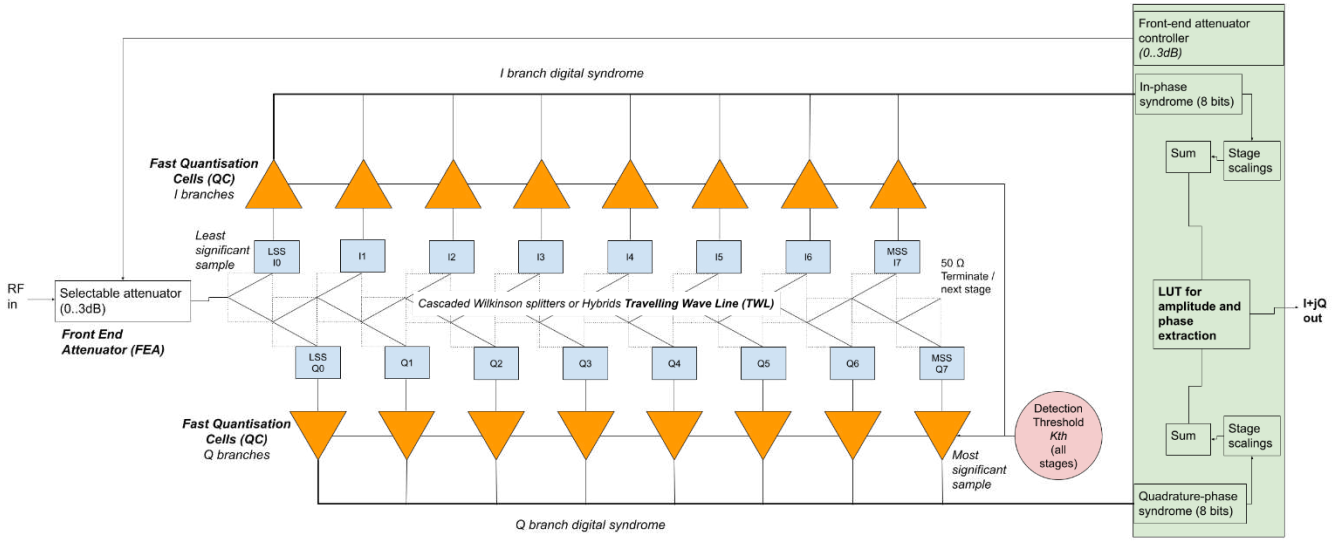


Fig. 1. Quadrature Sampling RF Travelling Wave ADC (QSTW-ADC): simplified concept showing key stages for a 16 tap system.

We then present a trial chip design architecture for the system. Finally, we present initial results from a lab emulator.

II. Architecture Concept

The architectural concept of the QSTW-ADC is illustrated in Fig. 1. The architecture uses a cascade of RF power splitters/dividers that are based on 90-degree phase lines: forming a travelling wave line (TWL) that also attenuates the signal as it progresses. The TWL can be implemented using cascades of Wilkinson power dividers or branch line hybrids. As the RF signal travels down the TWL it is attenuated by 3 dB at each node, as well as experiencing a 90-degree phase shift. This means that the TWL will provide quadrature samples at its outputs, with reducing amplitudes along the line. This allows a simple comparator based on a 1-bit Quantisation Cell (QC) digitiser to be used at the tap outputs. Overall, this enables efficient IQ extraction at the operating frequency of the TWL, which could be directly at the RF carrier (Fc), or a down converted high IF.

In our trial concept, there are sixteen taps ($M = 16$) in the TWL, giving 8 slices on I and 8 slices on Q. It can be extended to achieve a greater dynamic range, by cascading more TWL stages. Also, the number of active digitising stages required can be enabled or disabled to suit a particular operational scenario – allowing selectable performance or power savings in operation.

The $M = 16$ tap system will have a theoretical dynamic range defined as the maximum detectable signal reaching the far end of line, compared to the minimum detectable at the start of line. Hence the dynamic range is 3 dB x(M-1) = 45 dB. This is comparable to a conventional 8-bit ADC system. If the carrier signal travelling down the TWL is modulated, then the modulation symbol must remain unchanged for 1 full line propagation delay, to be properly demodulated, since all digitising cells need to see the same signal. If Wilkinson splitters are used (i.e. 90-degree phase shift per TWL tap point) this corresponds to $M / 4 = 4$ cycles of the RF carrier must exist along the TWL during a symbol demodulation.

The 3 dB attenuation experienced as the signal moves down the TWL between tap nodes represents a quantisation step at each sampling location, defining the ADCs quantisation noise. This uncertainty can be reduced through use of an adjustable front-end attenuator (FEA). The FEA can be used to sweep the input attenuation during ADC operation until some of the QC stages just change their output states. This change in state represents that we are on the slicing boundary of a digitiser- and hence at the best slicing point accuracy. However, this process requires the signal along the TWL to be at a constant amplitude during the assessment – imposing a limit on the modulation rate. The FEA could be implemented using conventional RF circuit, switchable attenuator, techniques. The FEA could also be implemented using an RF switch that is duty cycled as per time modulated array concepts [12], which would allow an RX phased array to be directly realised via multiple QSTW-ADCs.

Each QC of the QSTW-ADC consists of amplification and slicing of the analogue signal compared to a set threshold, which is common to many ADC processes. The digitised output can be one of 3 states: 0 / QC input > Kth / QC input < -Kth. The Kth threshold can be common to all QC stages: for example, chosen as the minimum level that allows the stages to detect a signal without triggering on noise. In practice, two separate detection circuits are used to compare the TWL tap RF signal. One to compare it to Kth and another to compare it to -Kth, each with their own sliced output per QC stage n: *tap_pos[n]* and *tap_neg[n]* respectively. We define this sliced set of digital signals from the QSTW-ADC QCs as the *syndrome*. The syndrome is then subject to simple signal processing to obtain the final symbol IQ value, as will be discussed.

The sliced output of the QSTW-ADC QCs can be converted to a weighted IQ signal using (1) and (2), where *tap[n]* is the state of circuit's digitised output (0 or 1) at tap n. The progression down the TWL corresponds to a phase rotation of 90 degrees per tap and a 3 dB signal reduction, both of which must be accounted for when forming the composite IQ signal. The resulting IQ signal reconstruction from QC syndrome results directly from (1) and (2).

$$I_{out} = Kth.A.(tap\_pos[0] - tap\_neg[0])\cos\left(\frac{2\pi 0}{4}\right) + Kth.A.\left(\sqrt{2}\right)^2(tap\_pos[2] - tap\_neg[2])\cos\left(\frac{2\pi 2}{4}\right) + Kth.A.\left(\sqrt{2}\right)^4(tap\_pos[4] - tap\_neg[4])\cos\left(\frac{2\pi 4}{4}\right) + \cdots \quad (1)$$

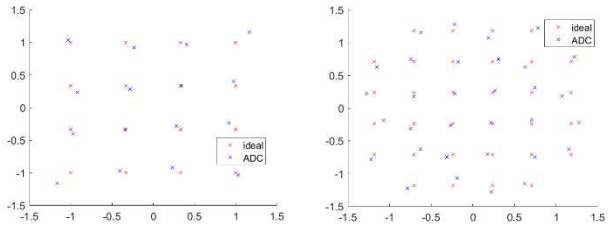
$$Q_{out} = Kth.A.(\sqrt{2})(tap\_pos[1] - tap\_neg[1])\sin\left(\frac{2\pi 1}{4}\right) +$$
$$Kth.A.(\sqrt{2})^3(tap\_pos[3] - tap\_neg[3])\sin\left(\frac{2\pi 3}{4}\right) +$$
$$Kth.A.(\sqrt{2})^5(tap\_pos[5] - tap\_neg[5])\sin\left(\frac{2\pi 5}{4}\right) + \cdots \quad (2)$$

Parameter *Kth* is found using (3), based on the length of the TWL and the maximum acceptable input signal amplitude Vin_{peak}. Parameter *A* is the linear attenuation of the FEA at the sampling assessment point.

$$Kth = \frac{Vin_{Peak}}{(\sqrt{2})^{[M-1]}} \quad (3)$$

The step size of the FEA defines the granularity of amplitude detection (and hence signal to quantisation noise ratio) and thus the constellation size that can be demodulated. Considering constellation point symbol spacing and using *M* = 16 with no FEA reveals QPSK can be demodulated. With a 1 dB FEA step size 32QAM can be supported, and a 0.5 dB FEA step size attenuator can support 64QAM. If *Kth* and *A* are fixed, a Look Up Table (LUT) can be used to map from the sliced syndromes (*tap_pos* and *tap_neg*) from the QSTW-ADC QCs to a composite reconstructed IQ signal. This maximises speed of conversion and avoids a direct mathematical implementation of (1) and (2) at run time. The LUT coefficients can be tuned, if required, during an initial ADC calibration phase. This could also include compensation for manufacturing tolerances, or amplitude imbalance at each tap. The LUT coefficients can be fixed-point.

The ADC's maximum effective number of bits (ENOB) can be predicted, since the TWL's 16 taps (8 I / 8 Q) each have 3 states (-/0/+), i.e. 24 states in I and Q: which requires 4.6 bits without the FEA. The 0.5 dB step FEA has 6 states (2.6 bits required) applied to both I and Q. Hence, the theoretical max I or Q ENOB is 7.2 bits.



(a) (b)

Fig. 2. Constellations of detected QAM signals: a) QAM16 (RMS EVM = 8.1%), b) QAM32 signal detected (RMS EVM = 6.2%).

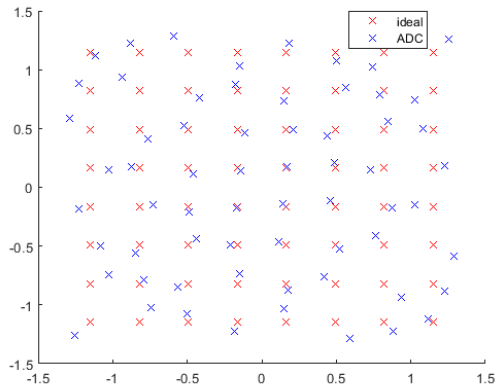


Fig. 3. Constellation of QAM64 signal detected (RMS EVM = 5.9%).

TABLE I. SIMULATED EVM VS. INPUT SNR.

Input SNR (dB)	QPSK RMS EVM (%)	QAM16 RMS EVM (%)	QAM32 RMS EVM (%)	QAM64 RMS EVM (%)
60	5.9	8.1	6.2	5.9
30	8.2	8.6	7.9	6.6
20	13.9	13.2	14.4	14.1
10	33	28.9	34.1	26.1

III. IQ CONSTELLATION AND ENOB SIMULATION

We now present an assessment of the QSTW-ADC concept with QAM modulated carriers. A Matlab full time domain implementation of a QAM QSTW-ADC system was created, implementing (1) - (3) and with a 0.5 dB step FEA. We present example results as QAM constellations and associated error vector magnitude (EVM) in Fig. 2 and Fig. 3. Initially, we assumed a thermal noise free operation in the simulations, with signal degradation therefore only from quantisation of the QSTW-ADC. Subsequently, the effect of input white noise defined SNR was tested, with recovered RMS EVMs presented in Table 1.

The results of the constellation tests suggest that the practical limit of the 16-tap system is 64QAM. The 0.5 dB FEA steps used to mitigate the 3 dB quantisation uncertainty implies the TWL would need 4 cycles of the RF signal to evaluate the constellation point for each FEA step. This implies the worst-case delay to identifying a constellation point is 4x(3/0.5) = 24 cycles of the carrier and so defines the maximum symbol rate for a modulation type.

The ENOB was evaluated using a system numerical simulation of the QSTW algorithms. This showed that the SFDR was 33 dB, SNDR was 27 dB and ENOB was 4.2 bits, for both the I and Q outputs. If the harmonic distortion terms are ignored, the ENOB improves to 5.5 bits, per output.

IV. EXPLORATORY CIRCUIT DESIGN FOR A QSTW-ADC ON A GAAS MMIC AT 28 GHZ

We will now outline an initial integrated circuit (IC) hardware design at 28 GHz for a GaAs MMIC concept and discuss an overview of key circuit architectures. Since the QSTW-ADC uses a 50-ohm cascaded set of power dividers and RF circuitry, the concept suits commercial IC implementation. We have created a set of subsystems for a GaAs MMIC, using the UMS Ltd PH10 pHEMT process and designed the IC using Keysight ADS. We have made certain necessary simplifying architectural decisions during this trial implementation, which we will also discuss in this section.

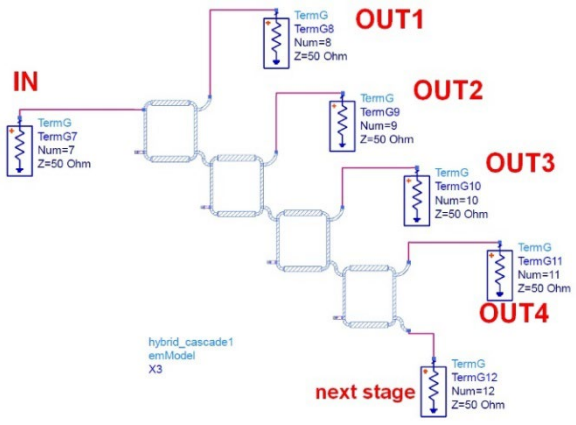


Fig. 4. Cascaded Hybrids in a TWL. RF input is on the far left and each of the outputs 1-4 will connect to a 1 bit QC stage.

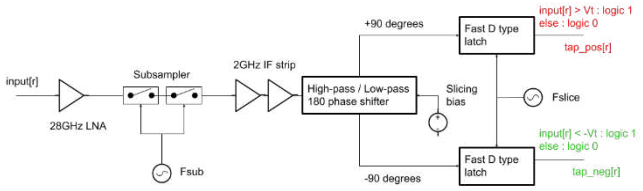


Fig. 5. Simplified QSTW-ADC QC architecture: concept cell at 28 GHz. One QC per TWL tap is required.

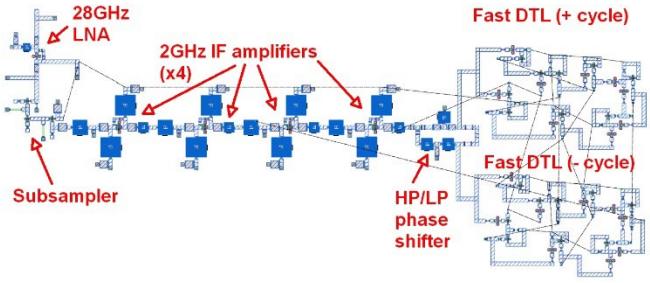


Fig. 6. Resulting QSTW-ADC QC layout (left to right: 28 GHz LNA, subsampler, quad-stage 2 GHz IF strip, twin DTLs. (Full layout including DTLs: 8.8mm x 3.6mm, RF only part of layout: 6mm x 1.5mm).

Although the Wilkinson power divider is a simple conceptual approach to implement the TWL, other power dividers can be beneficial for a practical layout. We now adopt a 90-degree branch line hybrid power divider. This allows a more compact IC layout and can help improve the impedance matching between stages. The layout for a 4 tap TWL is shown in Fig. 4. The TWL can be cascaded to extend the number of taps. A digitising QC is required at each TWL output tap point, as illustrated in Fig. 1, with tap locations as shown in Fig. 4.

The RF design of the QC is complex and needs to ultimately balance multiple criteria – power efficiency, gain, bandwidth, carrier frequency, sampling frequency and circuit complexity. The proposed simplified architecture for a cell is shown in Fig. 5. The QC IC design consists of an input low noise amplifier (LNA), with 9.6 dB gain and 3.2 dB noise figure (NF). The LNA helps to lower ADC system NF and is followed by a twin cold-FET subsampler [13]. An LNA could also be added to the RF input of the TWL, though compression here must be avoided, since it would affect all the QCs. The subsampler converts the 28 GHz signal down to a 2 GHz IF, using *Fsub* frequency source (shared by all QCs). We use a sinusoid-controlled sampler, as per our earlier work [13], as this simplifies clock source requirements. The resulting IF at 2 GHz is then amplified. The IC implements a cascade of 4 IF amplifiers (each having 13.5 dB gain and 2.7 dB NF) to drive the quantising logic circuits. The output of the IF amplifier stage is then passed through a high-pass / low-pass phase shifter circuit to generate dual +90 degree and -90 degree phase outputs. This approach allows positive and negative parts of the RF cycle to be handled by dedicated logic subsystems, to detect *tap_pos* and *tap_neg* states.

The IF analogue signal is then compared to a fixed reference voltage (defining *Kth*) using a pair of fast D-type latches (DTLs), which are edge triggered by a second frequency source, *Fslice* (common to all QCs). *Fslice* can be at the IF, or a lower frequency and thus subsample the IF signal. The DTL is implemented using resistor-transistor logic techniques, since the PH10 GaAs process only includes N channel transistors. The DTL is a key area for future research into implementation options.

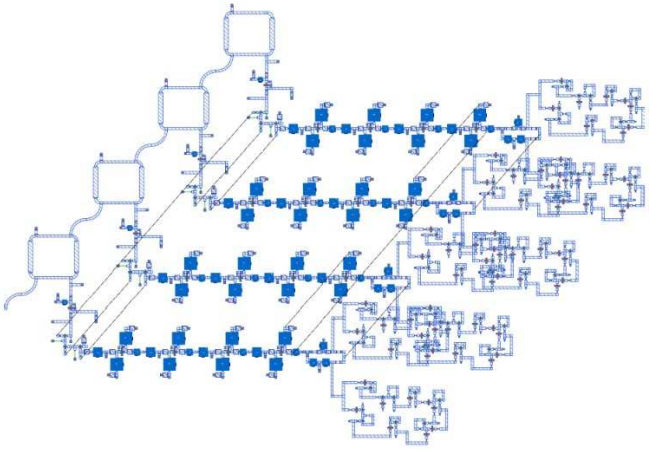


Fig. 7. Trial IC layout based on QCs and Cascaded Hybrids TWL. (14mm x 9.8mm GaAs) –further optimisation of layout is possible.

TABLE II. TWL HYBRIDS ADS SIMULATION RESULTS AT 28 GHZ.

Tap location	Expected tap IL (dB)	Measured tap IL (dB)	Expected tap phase (deg)	Measured tap phase (deg)
1	-3	-3.7	-90	-89.5
2	-6	-6.6	0	1.3
3	-9	-9.4	90	90
4	-12	-12.2	-180	178.5
output to next stage	*-12*	*-11.2*	*0*	*-5.9*

In this IC, we have designed the system to work at 28 GHz, with a 2 GHz IF and *Fsub* = 6.5 GHz (hence a Nyquist zone at 4th sampling harmonic is used in subsampling) and *Fslice* triggers a digitisation of the symbol.

The QSTW-ADC concept is frequency agnostic. Other frequency combinations are possible, depending on the RF capabilities of available foundry processes and subsampling objectives. The layout of the QC is shown in Fig. 6. Fig. 7 shows the MMIC layout for a 4 tap QSTW-ADC, using 4 QCs and the TWL cascaded hybrids.

V. INITIAL RF TRIALS OF A QSTW-ADC

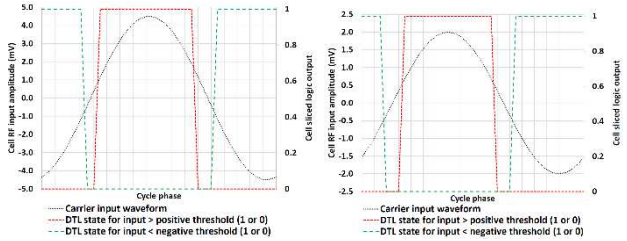
A. GaAs MMIC trial simulation results of a QSTW-ADC

We have performed full circuit simulations of a concept 4 stage QSTW-ADC. The TWL hybrid cascade gives good results, with Table 2 showing the insertion loss (IL) and tap phase agrees with expectations. The 0.5 dB IL BW is 2 GHz and 3 degrees phase delta BW (between taps) is 510 MHz. Amplitude imbalance from IL spread could be compensated using a per-tap *Kth*, if needed or incorporated into the LUT. The band-centre, peak IL imbalance error across the 4 taps is 0.7 dB and the peak phase imbalance error is 1.5 deg. We then applied this tolerance as a normal distribution across all taps in the system model. Compared to Table 1, the resulting EVMs degrade by circa 1 %, at 30 dB input SNR.

Circuit simulation results of the QC cell at 28 GHz have been obtained. The assessment evaluated the RF-in to digital-out performance of a single QC stage, as shown in Fig. 7. Fig. 8 and Fig. 9 present the digitised outputs at various input carrier phases of an RF input cycle, for various RF input levels. As expected for a 1-bit digitiser, a correctly sliced digital output is seen. The portion of the wave with digitised outputs at zero is seen to increases as expected as the amplitude decreases, and proportionally more of a cycle is spent in between *-Kth* and *Kth*. From simulation, the QC

detection threshold is 0.4 mV pk, i.e. a theoretical detection floor of -58 dBm in 50 ohms. The last cell in a 16 sample TWL would have a triggering sensitivity 45 dB higher, i.e. 71 mV. This could be increased by cascading more TWLs and QCs.

If the *Kth* is constant and common for all QCs, the system operates as a logarithmic ADC. Other profiles are possible, by changing *Kth* at each cell (e.g. allowing focusing in on a narrow range of amplitudes). The RX sensitivity of a QSTW-ADC is potentially much lower than conventional ADCs, due to the use of low noise amplifiers and IF amplifier stages in each QC. Then including the IL of the first hybrid means the ADC minimum detectable signal (MDS) input sensitivity is -55 dBm. Assuming a 30 dB SNR is required for thermal noise, suggests the signal input BW at this sensitivity could be up to 794 MHz (ignoring SNDR limitations).



(a) (b)

Fig. 8. Outputs for 1 QC with 28 GHz input of: a) 4.5 mV pk, b) 2 mV pk.

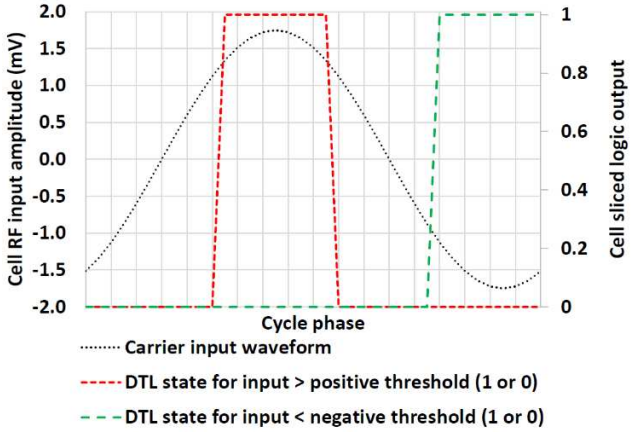


Fig. 9. Outputs for 1 QC with an RF input at 28 GHz of 1.75 mV pk.

We then evaluated the 3 dB operational bandwidth of the RF analogue active circuit (not including the DTL), with results shown in Fig. 10.

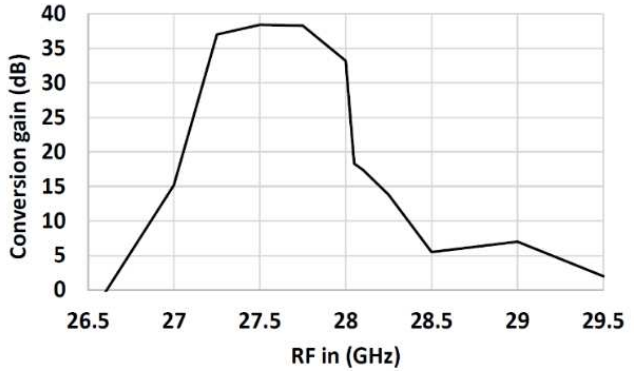


Fig. 10. QC RF front end conversion gain and bandwidth (28 GHz RF input to 2 GHz DTL IF input).

Fig. 10 shows a potential operational range of 27.25 GHz to 28 GHz is achieved, which could thus support a demodulation BW of 750 MHz. The symbol BW will also be constrained by the Nyquist BW of the subsampler (6.5 GHz *Fsub*) and the DTL digitising subsampler *Fslice*.

The digitising capability of the DTL was also investigated. Full circuit simulation showed it is capable of correctly tracking and slicing an analogue signal with frequency of up to 5 GHz, using a latching pulse width of 2 ns. Though a simple implementation, a DTL in the RF MMIC process could be viable as 1-bit quantiser with an *Fslice* of 500 MHz. This would allow it to also subsample the 2 GHz IF and support an IF BW of up to 500 MHz. However, the power consumption of the present GaAs DTL is significant.

Table 3 compares key performance simulation results for the 16-stage QSTW-ADC to other relevant recent works in Flash and Pipelined ADCs. The simulated system ENOB of 4.2 bits per I and Q channels is comparable to other mmWave ADCs. The minimum detectable signal (MDS) is estimated for all devices, assuming a 500 MHz signal BW and then applying processing gains for the prior works with higher sampling frequencies. The simulated power draw of the present concept system is dominated by the 2 GHz IF stage (112mW/cell) and DTL (110mW/cell). In contrast, 19 mW is drawn by the LNA and subsampler cell. The IF and DTL modules are suitable for implementation in more power-efficient SiGe or CMOS technologies. This could employ a heterogeneous integration approach.

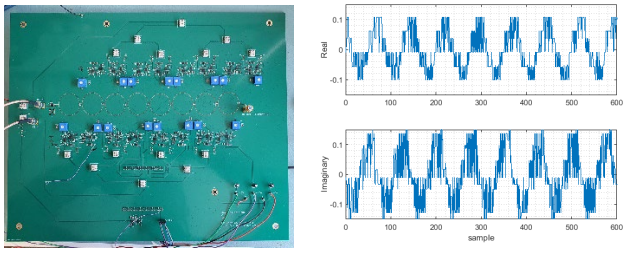
Table 3 shows that the simulated QSTW-ADC, as a new theoretical concept, is competitive and could be useful at mmWave. It may be possible to use the LUT to help improve the ENOB, by applying syndrome state-specific corrections.

B. Applicability to multicarrier modulation

Although the QSTW-ADC has been proposed for single carrier modulation, it is interesting to consider its viability for multicarrier systems, such as CP-OFDM used in 5G FR2. In general, OFDM symbols have a noise-like time domain waveform with a high peak to average. The QSTW-ADC requires the modulating signal to be unchanging in phase and magnitude at the instant of TWL tap sampling.

TABLE III. THE QSTW-ADC AND PRIOR WORKS (CT = CONTINUOUS TIME, TI = TIME INTERLEAVED, DDC = DIGITAL DOWN CONVERTER).

Ref.	Fc (GHz) / Fs (GHz)	Total chip DC power (mW)	SNDR (dB) / SFDR (dB)	ENOB / MDS (dBm)	Architecture
This work (circuit & numeric simulations)	*28 / Fs = 6.5 Fslice = 0.5*	*(M = 16) 3862 (IF: 1792 DTL: 1760)*	*27 / 33*	*I: 4.2 Q: 4.2 / -40*	*QSTW GaAs PH10*
[4]	- / 18.5	270	25 / 33.6	3.9 / -41	22nm CMOS Flash
[9]	4.8 / 10	495	50.8 / 60.7	8.1 / -59	28nm CMOS TI-pipelined
[10]	- / 6.4	240	61.6 / 68	9.9 / -66	16nm finFET CT-pipeline
[11]	40.5, 28.3 / 12.8	2.5	30.5, 36 / 33.6, 40.6	4.8, 5.7 / -44, -49	ADC & DDC & high speed serial interface



(a) (b)

Fig. 11. PCB QSTW-ADC concept test emulator: a) 8 stage PCB test system, b) produced IQ waveforms after applying the sliced data from the PCB.

This requires an OFDM time domain signal sample to be unchanging over a period of 24 cycles of the carrier *Fc,* in our concept, to achieve a 0.5 dB amplitude uncertainty, as discussed earlier. To explore this further, a numerical simulation of a 28 GHz OFDM signal, with 1000 subchannels each of BW 240 kHz, was used. This produced an OFDM occupied BW of 240 MHz, and an OFDM fractional symbol time sample duration equal to 116.7 cycles of *Fc*: representing 4.9 TWL delays. A full symbol is 116.7 thousand cycles of *Fc*. The availability of the 4.9 TWL 'OFDM sample' evaluation events suggests oversampling could possibly be used to improve the ENOB by 1 bit, to 5.2 bits. Higher mmWave frequencies, or lower OFDM BW, also increase the number of *Fc* cycles present per OFDM time sample - enabling further oversampling.

C. PCB emulator demonstrator – initial test results

A 1 GHz PCB based 8 stage QSTW emulator system has been created, using a cascade of Wilkinson 3 dB power splitters and commercial fast comparators with latched outputs (Analog Devices ADCMP580). This system has allowed us to test concepts in a lab setting, primarily to investigate the digitisation algorithm using (1) - (3), prior to more detailed IC design. This system is still being commissioned, but initial tests confirm expected operation of the QSTW concept. Fig. 11a shows the PCB platform and Fig. 11b shows an example extracted reconstructed raw IQ waveform, showing the subsampled quadrature signal is obtained as expected.

VI. Conclusion

The QSTW-ADC concept has been introduced and key aspects simulated. The concept blurs the distinction between ADCs and the conventional RF RX chain, bringing the digitisation into the RF hardware domain and thus potentially enabling digitisation at higher carriers or IFs. A trial 28 GHz GaAs IC design has been discussed, as a first exploratory hardware concept.

An ENOB of 4.2 is found by simulation, from the 16-tap system. This ENOB is available in both I and Q outputs. Performance for a range of QAM formats is discussed, up to 64QAM. OFDM may also be viable, notably where low ENOB is acceptable. The present analogue circuits support a modulation BW of up to 750 MHz.

The limiting factor in reaching higher data rates is the realisation of a fast DTL. Though our simple DTL pHEMT implementation simulation predicts good performance, we propose that this aspect of the circuit architecture requires more optimisation. The IF amplifiers could also benefit from low power implementations. The QSTW-ADC could be realised as a hybrid integration of III-V (GaAs, GaN, InP) circuits for the TWL and RF processing, transferring the IF signals to other appropriate implementations for DTL circuits and associated syndrome interpreter LUT.

The QSTW-ADC is modular and can be cascaded to obtain a desired dynamic range or ENOB, within noise limitations. Further study will investigate a full theoretical model of the ADC's performance, architecture considerations relating to the number of taps and number of IF stages, threshold profiles, IC implementation choice proposals and techniques for handling manufacturing tolerances. Concepts will then be further verified in test hardware.

References

[1] Tertulien. Ndjountche, Data Converters, Phase-Locked Loops, And Their Applications. CRC Press, 2019.

[2] N. Kandpal, A. Singh, and A. Agarwal, "An artificial intelligence-based 4-to-10-bit variable resolution flash ADC with 3.6 to 1.04 GS/s sampling rate," International Journal of Circuit Theory and Applications, vol. 52, no. 8, pp. 4067–4085, Aug. 2024, doi: 10.1002/cta.3948.

[3] D. Wang, P. Miao, H. Wang, J. Guo, F. Li, and Y. Yu, "An 8-Bit 32-GS/s time-interleaved two-step flash ADC with common-mode compensated buffer in 40-nm CMOS," International Journal of Circuit Theory and Applications, Oct. 2025, doi: 10.1002/cta.70170.

[4] N. Lotfi, P. Scholz, and F. Gerfers, "The Fastest CMOS Single-Channel 5-bit Flash ADC Operating at 18.5 GSs in 22 nm FD-SOI," in 2023 18th European Microwave Integrated Circuits Conference (EuMIC), Berlin, Sep. 2023, pp. 121–124. doi: 10.23919/EuMIC58042.2023.10289098.

[5] H. Shibata *et al.*, "A 9-GS/s 1.125-GHz BW oversampling continuous-time pipeline ADC achieving -164dBFS/Hz NSD," IEEE Journal of Solid-State Circuits, vol. 52, no. 12, pp. 3219–3234, Dec. 2017, doi: 10.1109/JSSC.2017.2747128.

[6] J. Sun and J. Wu, "A 12-bit 1.0/2.0 GS/s pipeline ADC in 0.18 µm SiGe BiCMOS," International Journal of Electronics, vol. 105, no. 12, pp. 2114–2127, Dec. 2018, doi: 10.1080/00207217.2018.1494335.

[7] J. G. Lim *et al.*, "A hybrid voltage-time domain pipelined ADC with reference-embedded time-domain residues," IEEE Journal of Solid-State Circuits, vol. 61, no. 2, pp. 566–577, Feb. 2026, doi: 10.1109/JSSC.2025.3579913.

[8] S. Chatterjee and S. Roy, "A self-calibration method of a pipeline ADC based on dynamic capacitance allotment," IEEE Trans. Very Large Scale Integr. VLSI Syst., vol. 30, no. 5, pp. 666–670, May 2022, doi: 10.1109/TVLSI.2022.3151479.

[9] Y. Liu *et al.*, "A 12-bit 10 GS/s Pre-Sampling Pipelined ADC With Split-Capacitor-Based Parasitic Compensation Technique," IEEE Transactions on Circuits and Systems II: Express Briefs, vol. 73, no. 4, pp. 388–392, Apr. 2026, doi: 10.1109/TCSII.2026.3666826.

[10] R. Mittal *et al.*, "A 6.4 GS/s 1 GHz BW Continuous-Time Pipelined ADC With Time-Interleaved Sub-ADC-DAC Achieving 61.7 dB SNDR in 16 nm FinFET," IEEE J. Solid-State Circuits, vol. 59, no. 4, pp. 1158–1170, Apr. 2024, doi: 10.1109/JSSC.2023.3338686.

[11] Teledyne EV10AS940 datasheet [Online]. Available: https://semiconductors.teledyne-e2v.com/products/adc/?model=EV10AS940

[12] E. A. Ball, S. D. Joseph, and A. Tennant, "Receive mode time modulated antenna array incorporating subsampling - theoretical concept and laboratory investigation," IEEE Open Journal of Antennas and Propagation, vol. 4, pp. 626–640, Aug. 2023, doi: 10.1109/OJAP.2023.3293123.

[13] E. A. Ball and S. D. Joseph, "Microwave subsampler using cascaded cold pHEMTs," in 2025 50th International Conference on Infrared, Millimeter, and Terahertz Waves (IRMMW-THz), Helsinki, Aug. 2025, pp. 1–2. doi: 10.1109/irmmw-thz61557.2025.11319821.