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Impact of Via Placement on Reflection Coefficient in Reflective Metasurfaces

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***Abstract*—This paper investigates the impact of via placement on the reflection coefficient of a reflective patch metasurface, initially designed with resonate frequency of 4.59 GHz and a reflection magnitude of -3.7 dB. Simulations were conducted for 36 different via locations within the unit cell across a frequency range of 4.60 GHz to 4.72 GHz. The results show that specific via placements can significantly reduce the reflection magnitude, with reductions up to -35 dB at 4.60 GHz. At higher frequencies, the region of maximum absorption shifts within the unit cell. Increasing the number of vias per unit cell also shifts the resonant frequency, reaching approximately 6.25 GHz with four vias. Three Surfaces was fabricated and tested at the coordinates of interest. The findings offer insights into optimizing metasurface designs for improved control over reflection coefficient.**

***Index Terms*—Reflective Metasurface, patch arrays, Sub-6GHz**

I. Introduction

Reconfigurable Intelligent Surfaces (RIS), also known as Programmable Metasurface [1], have emerged as a prominent research focus in wireless communication due to their ability to dynamically modify the wireless environment in a cost-efficient and energy-effective manner [2]. The functionality of RIS can be classified into two primary categories, based on distinct design methodologies: Electromagnetic (EM)-based design and communication-based design [3]. EM-based designs are concerned with the fundamental transformation and manipulation of electromagnetic waves. In contrast, communication-based designs treat the surface as an integral component of the information processing system [4].

Regardless of the design approach, precise control over the reflection coefficient of each unit cell, or groups of unit cells, is essential to achieving the desired functionalities. A widely adopted method involves the integration of electronic components, such as PIN [5] or varactor diodes [6], onto resonant structures. In this configuration, the reflection coefficient is controlled by varying the surface impedance, which is determined by the operating state of the diodes. This can be accomplished through the digital control of PIN diodes' ON and OFF states, as demonstrated in [5], or by tuning the capacitance of varactor diodes via different bias voltages, as shown in [6]. Incident wave manipulation and modulation are then achieved by configuring the surface either in the spatial domain, the time domain, or both, an approach referred to as space-time digital coding surfaces as demonstrated in [7].

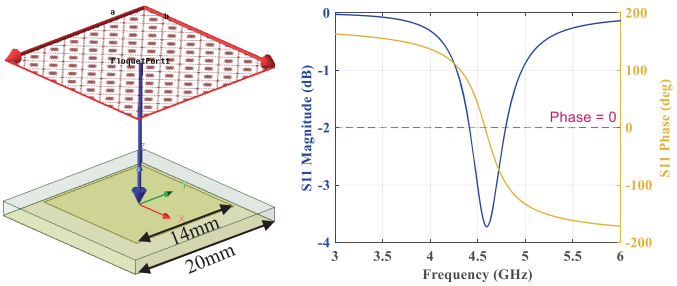
Research on intelligent surfaces has primarily focused on achieving multi-phase quantization [8] states, multi-functionality [9], and real-time control [10]. From a scalability perspective, higher phase states provide greater flexibility in controlling scattered waves. Works such as [11] and [12] have demonstrated multi-bit phase states by integrating additional PIN diodes onto resonant structures or adjusting more bias levels of varactor diodes. An alternative approach, proposed in [13] and [14], is the guided-wave method. Unlike conventional techniques, which directly modify surface impedance through PIN or varactor diodes, this approach adjusts the reflection coefficient by switching between different impedance control networks connected to the resonant structure through the vertical interconnect access (via).

This guided-wave approach simplifies design by eliminating the need for complex biasing circuits, as required in multi-bit PIN diode configurations, or the use of digital-to-analog converters (DACs) in varactor designs. By moving the control circuitry beneath the ground plane, this method offers greater flexibility in control circuit design, enabling more efficient multi-bit surface implementations.

This paper aims to investigate the impact of via placement on the reflection coefficient in a reflective patch surface based on the guided-wave architecture. In the study, the via is either connected to the ground plane or left unconnected to simulate the ideal behaviour of a PIN diode in its ON state (zero impedance) and OFF state (infinite impedance).

II. Via Location Analysis

A. Initial Concept and Simulation Setup



(a) (b)

Fig. 1. Patch Characteristic: (a) Unit cell size, (b) reflection magnitude and phase under normal incidence

The designed reflective patch operates at a resonant frequency of approximately 4.59 GHz, achieving a reflection magnitude of -3.7 dB under normal incidence. The patch was simulated using FR4 dielectric material, characterized by a relative permittivity of $\epsilon_r = 4.4$, loss tangent $\delta = 0.02$ and

a thickness of 1.6 mm. All simulation results were obtained using Ansys HFSS 2023.

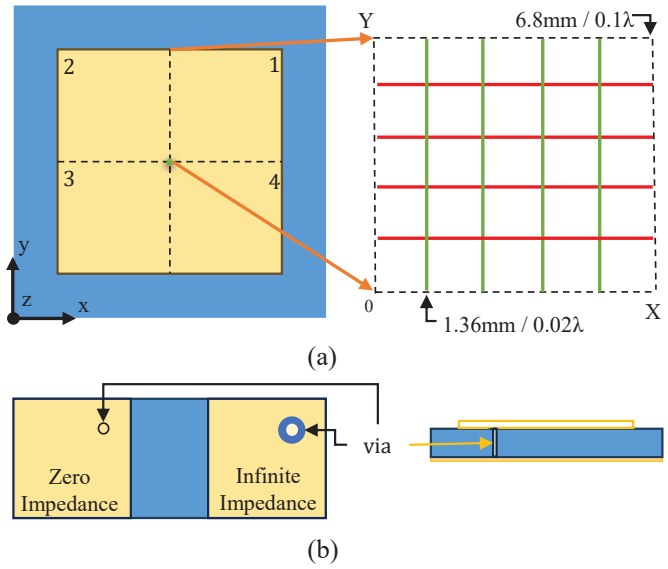


Fig. 2. Top and bottom views of the concept (not to scale): (a) Top view of the unit cell with the VIA location layout, the unit cell is divided into four quadrants, labeled 1 to 4, (b) Bottom transparent view showing zero and infinite impedance with a specific via location on two individual patches

The patch is divided into four quadrants, and via locations are defined relative to the centre (0,0) of the unit cell in quadrant 1, as shown in Fig. 2(a). The x and y coordinates range from 0 to 6.8 mm (0.1λ), with increments of 1.36 mm (0.02λ), where λ is the wavelength at the resonant frequency. A total of 36 via locations are defined for the study.

In the initial simulations, no external loads are connected, and the ideal PIN diode is modelled with two impedance states: zero impedance (ON state) and infinite impedance (OFF state). These states are represented by a via connected to the ground plane (zero impedance) and a via with clearance (no connection, simulating infinite impedance), shown in Fig. 2(b).

B. Simulation Results

The reflection coefficient remains constant across all simulations conducted in the infinite impedance state, as no electrical connection is established. Consequently, only the 36 sets of S_{11} data corresponding to the grounded state are analysed. The resonant frequency with the grounded via positioned at the centre of the unit cell is approximately 4.64 GHz.

Fig. 3 presents the variation in reflection magnitude as the via location shifts along the x and y coordinates at four frequency points. Grounded via placements near the x and y axes show minimal impact on the reflection magnitude across all frequencies, as illustrated by the red colour, with a maximum reduction of -0.75 dB compared to the default patch response. Among the 36 via locations, the via placement at (5.44, 4.08) achieves the lowest reflection magnitudes of -35 dB at 4.60 GHz and -18 dB at 4.64 GHz shown in Fig. 3 (a)-(b). At 4.64 GHz, positioning the via within the

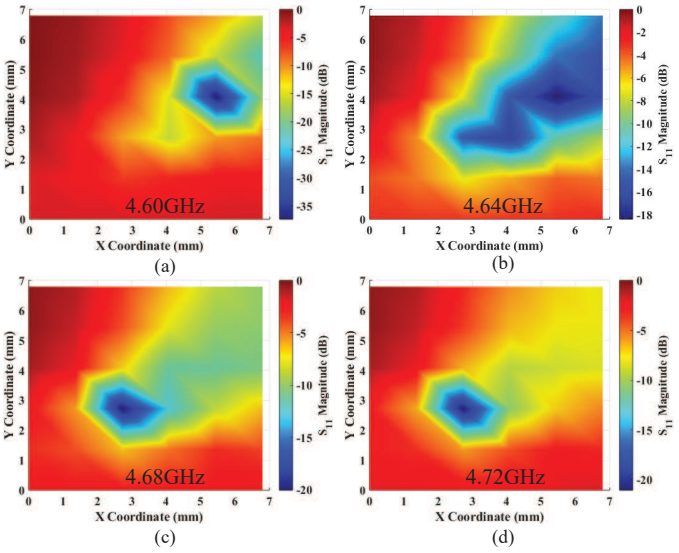


Fig. 3. Colourmap of reflection magnitude based on different ground via positions in quadrant 1 at varying frequencies: (a) 4.60 GHz, (b) 4.64 GHz, (c) 4.68 GHz, and (d) 4.72 GHz

area enclosed by the yellow region leads to a significant reduction in reflection magnitude, ranging from -8 dB to -18 dB. However, at higher frequencies, such as 4.68 GHz and 4.72 GHz, the location of the lowest reflection shifts to location (2.72, 2.72), and the area showing absorptive response shrinks compared to that at 4.64 GHz and 4.68 GHz.

Further simulations revealed that placing a single via in any quadrant yields the same effect if the reference distance is consistent. The reflection coefficient remains unchanged regardless of quadrant. Fig. 4 presents the analytical results of the reflection coefficient when multiple vias are placed on a single unit cell, with one via per quadrant, increasing up to four vias on individual quadrant. The vias are positioned at a reference distance of $x = 5.44$ mm and $y = 4.08$ mm from the centre, in reference to Fig. 2(a).

As the number of vias increases, the resonant frequency increases up to approximately 6.25 GHz with four vias, as observed in the S_{11} magnitude and phase graphs in Fig. 4. Notably, only the single via configuration exhibits an absorptive response. Additionally, placing two vias either vertically or horizontally across quadrants (in reference to Fig. 2(a)) results in a similar frequency shift without significantly impacting the reflection magnitude. However, when two vias are placed diagonally in quadrants 1 and 3, or 2 and 4, in reference to Fig. 2(a), the surface reverts to absorptive properties, matching the amplitude and phase response of a single via placed in any quadrant, illustrated in Fig. 4, where a single via is located in quadrant 1.

III. System Verification and Analysis

The analytical study of via simulation was validated through prototype fabrication and reflectivity measurements. Three surface prototypes were fabricated using 1.6 mm FR4 with $\epsilon_r = 4.4$, each featuring a 10×10 unit cell array ($3.28\lambda \times 3.28\lambda$).

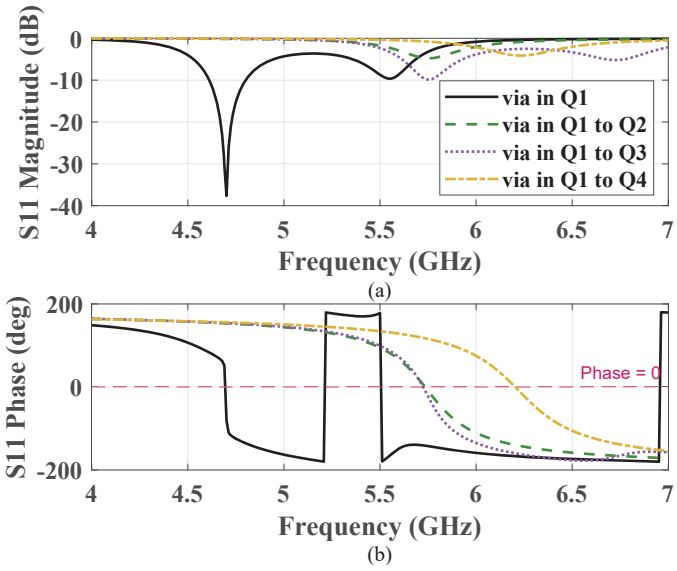


Fig. 4. Effect of multiple grounded vias at a reference distance of (5.44 mm, 4.08 mm) within a single unit cell, with one via per quadrant: (a) S_{11} magnitude response as the number of vias increases from 1 to 4, (b) S_{11} phase response as the number of vias increases from 1 to 4.

The prototypes included an original surface, and two surfaces with VIAs representing infinite impedance and zero impedance states. The via of interest was positioned at (5.44 mm, 4.08 mm) or $(0.06\lambda, 0.04\lambda)$ from the centre in quadrant 1, as shown in Fig. 5.

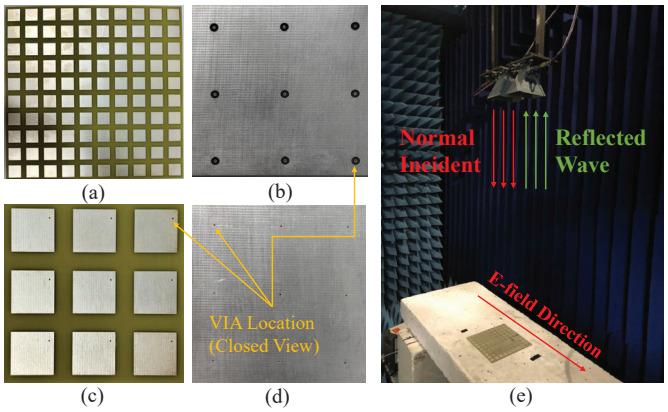


Fig. 5. Close View on fabricated surface: (a) Full surface top view. (b)via corresponds to infinite impedance bottom view. (c) via location top view (d) via corresponds to zero impedance bottom view. (e) Surface under test environment

Measurements were performed for both Transverse Electric (TE) and Transverse Magnetic (TM) modes, with the electric field polarized along the Y-axis for TE and the X-axis for TM. The measured reflection magnitude for the original surface closely matched simulation results, with measured values of -2.5 dB compared to -3.73 dB in simulation, as demonstrated in Fig. 6. However, the measured phase response shown in Fig. 6 exhibited a shorter transition than predicted in the simulations, although the overall bandwidth remained consistent.

Reflectivity measurements for the surfaces in both the open (infinite impedance) and ground (zero impedance) states are shown in Fig. 7. In the infinite impedance state, the reflection magnitude exhibited minor fluctuations, with a difference of -1 dB for TE incidence and -5 dB for TM incidence, while the reflected phase remained nearly identical for both modes. In the zero impedance state, the variation in reflected magnitude was minimal, and an absorptive response was successfully confirmed through both simulation and measurement results at the target frequency of 4.64 GHz.

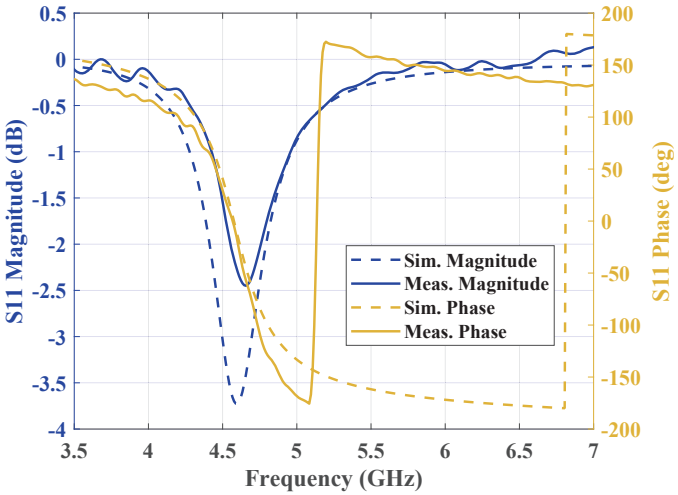


Fig. 6. Simulated and measured S_{11} data of original surface

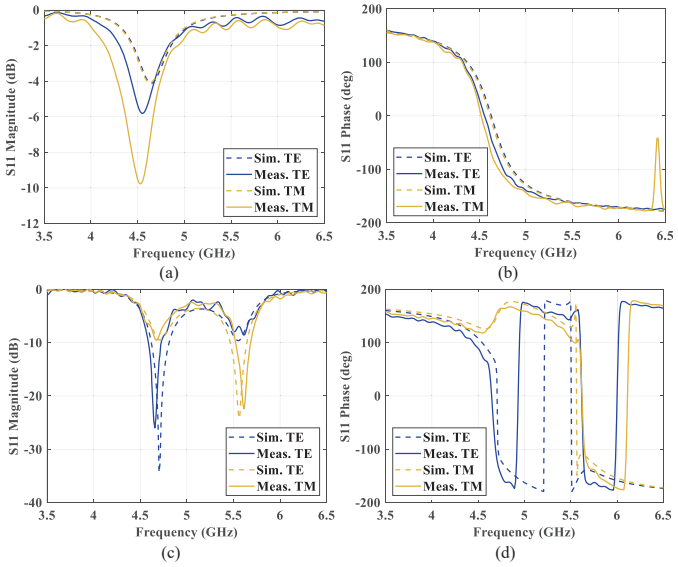


Fig. 7. Simulated and measured S_{11} data at via location (5.44,4.08): (a) S_{11} magnitude of infinity impedance state, (a) S_{11} phase of infinity impedance state, (c) S_{11} magnitude of zero impedance state, (d) S_{11} phase of zero impedance state

IV. Conclusion

In this paper, the behaviour of a reflective patch array with 36 via locations has been investigated. Simulating the ideal

performance of PIN diodes in both zero and infinite impedance states. The results demonstrated that specific via placements within the unit cell significantly influence the performance of the reflective surface, with reductions of up to -35 dB at 4.60 GHz. At higher frequencies (4.68 GHz and 4.72 GHz), the absorptive region shifted to different locations within the unit cell. Additionally, increasing the number of VIAs per unit cell resulted in a resonant frequency shift, reaching approximately 6.25 GHz with four vias.

Furthermore, the work has been supported by measurements from three fabricated prototypes, confirming the simulated S_{11} magnitude and phase responses, and verifying the surface's absorptive behaviour. These findings suggest that precise via placement can provide effective control over the reflection coefficient. Future work could focus on integrating actual PIN diodes or other tuneable elements to optimize the design for dynamic control over multiple phase states and expanded functionalities. The controllable surface could serve as a reflective shield, enabling the incident signal at 4.64 GHz to be either reflected or suppressed. Additionally, beam manipulation could be achieved through the implementation of a full impedance control network.

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