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An RF-Switch-Enabled Low-Power Dual-Mode Reconfigurable Reflective Surface

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ABSTRACT

This paper presents a novel reconfigurable reflective surface capable of selective magnitude control at sub-6 GHz frequencies. Each unit cell integrates a low-power single-pole double-throw (SPDT) RF switch beneath the ground plane, providing two distinct impedance states that govern the reflection coefficient of the unit cell. The proposed configuration enables dynamic switching between reflective and absorptive modes at 5.50 GHz. A full system prototype comprising an 8×8 unit cells was fabricated and tested, the measured results exhibit good agreement with full-wave simulations, with the 1-bit (0°-180°) reflection phase control at 5.05 GHz and reflection magnitude switching between -2.4 dB and -26 dB at 5.50 GHz under TE-polarized excitation. In addition, various geometric coding patterns were explored and implemented to further assess the surface's capability for a thinned reconfigurability and improved power efficiency. Three sets of ring-based surface configurations were investigated in detail, demonstrating that the surface is capable of selective magnitude control at both 5.05 GHz and 5.50 GHz under these pattern configurations. Specifically, these configurations enable quantized reflection magnitude control at 5.05 GHz, with an average step size of circa 5 dB. The results confirm the surface's flexible reconfigurability and reveal that activating only 75% of the available switches achieves performance comparable to full-surface operation, effectively reducing control complexity and overall power consumption.

INDEX TERMS Reconfigurable intelligent surface, Power Efficiency, RF-switch, Sub-6GHz

I. INTRODUCTION

THE future generations of wireless communication systems, including sixth-generation (6G) and beyond, are expected to be highly programmable, reconfigurable, and capable of supporting precise localization, in addition to offering high data rates and low latency [1]. Promising technologies such as millimetre-wave and terahertz communications, as well as the integration of artificial intelligence (AI) and machine learning (ML), have been widely explored and developed. However, these approaches often rely on expensive and complex hardware platforms and exhibit increasingly high-power consumption. Among the emerging solutions, reconfigurable intelligent surfaces (RIS) have gained significant attention for their potential to provide energy-efficient and cost-effective enhancements to wireless networks [2]. A RIS can be conceptualized as a thin, planar composite sheet composed of periodic or quasi-periodic unit-cell structures with sub-wavelength dimensions [3]. By dynamically adjusting these unit cells, the surface can manipulate incident electromagnetic (EM) waves in a programmable and controllable manner. It can be strategically deployed in diverse indoor and outdoor environments to enable functionalities such as signal redirection for virtual line-of-sight (VLOS) communication, physical-layer security enhancement, shielding, and sensing [4], [5], [6]. In addition to EM control, RIS can also participate in data processing [7], [8], enabling time-domain digital coding or space–time

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coding metasurface that support advanced modulation and coding schemes [9], [10], [11].

A fundamental design consideration in RIS development is the integration of tuneable elements, which enable dynamic control of the reflection coefficient to achieve multifunctionality. The choice of tuning element directly influences the overall architecture, control complexity, and performance of the RIS. A widely adopted practice is employing electronic components with external voltage control, such as varactor diodes [12], [13], [14], and PIN diodes [15], [16], [17], due to their compact size, low-cost and compatibility with hardware platforms such as microcontrollers and FPGAs. These works typically integrate one or more tuneable components within each unit cell to achieve multi-level phase quantization or multifunctional operation. By controlling the operating state of the tuneable elements, the reflection magnitude or phase of individual or group of unit cells can be dynamically reconfigured, enabling precise manipulation of the incident EM waves.

In practical implementations, the performance, cost, and power consumption of RIS are closely tied to hardware-level constraints such as phase resolutions or the number of tuneable elements per unit cell [18]. Although no theoretical limit exists on the number of tuneable elements, increasing their count within each unit cell significantly impacts the control complexity and overall power consumption.

Several works in [19], [20], [21], [22] have proposed models to estimate power consumption in RIS-assisted communication systems. The work in [19] suggest that power consumption depends on the number of identical unit cell N and the b-bit resolution of each unit cell, expressed as $P_{RIS} = NP_n(b)$. Similar model was used in work [21], where the system performance of active and passive RIS was evaluated under the same power budget, the RIS power consumption was modelled as $P_{RIS} = NP_{SW}$, where P_{SW} denotes the power consumption of a single unit cell. In particular, work in [22] presents a more detailed power consumption model with a comparative analysis of five RIS prototypes employing PIN diode, varactor diode, and RF switch. Their findings reveal that RF-switch-based RIS exhibit significantly lower power consumption at both drive circuit and unit cell level.

Although RF switches offer promising characteristics for energy-efficient RIS design, existing studies remain insufficient to fully quantify their practical advantages. A comprehensive evaluation must also account for control architecture, system functionality, implementation complexity and scalability. Some early work [23] has demonstrated the use of RF switches for passive reconfiguration of patch antennas, however, the designs are primarily oriented toward phased-array architectures rather than general reflective surfaces. This paper investigates an RF-switch-based RIS architecture that focuses on impedance tuning and reflection coefficient control. Specifically, a design that integrates a SPDT RF switch (QPC8019QSR, Qorvo) [24] with a reflective patch surface to enable impedance-based reconfigurability in a cost-effective and compact manner is presented. The integration introduces controllable impedance at selected via locations, enabling the surface to switch between reflective and absorptive mode with multiple level of magnitude control.

While extensive research has focused on phase control in reconfigurable surfaces, magnitude control offers complementary functionality and can be leveraged for both EM- and communication-based application. Such magnitude control enables the surface to function as an EM absorber [25], [26], with a direct application in reducing or dynamically controlling the radar cross-section (RCS) or stealth technology [27], [28]. In recent literature, amplitude-controllable surfaces are referred to as absorptive RIS (ARIS). ARIS implementations are primarily investigated for interference mitigation in spectrum-sharing scenarios and for enhancing physical layer security, with several studies suggesting that ARIS can outperform conventional passive RIS in suppressing multi-user interference [29], [30]. This aligns with the broader paradigm of RIS-enabled smart radio environments [5], in which the wireless channel is deliberately shaped to enhance communication performance.

The main contributions and novelties of this work are summarized as follows:

- Design methodology: A generalized approach for integrating RF switches into RIS is presented, based on impedance modelling and analysis of the load-controlled reflection coefficient, realizing an accurate prediction of unit cell performance prior to implementation.
- Experimental Verification: A fully functioning 8×8 RIS prototype with integrated control circuitry was fabricated and characterized. The measurements validate the proposed impedance selection methodology and confirm the efficacy of the control strategy.
- Dual Frequency operation: In addition to full-surface switching, ring-based configurations are explored and investigated, which provides the control on reflected magnitude at both 5.05 GHz and 5.50 GHz, demonstrating a versatile architecture for practical deployments.

The remainder of this paper is organized as follows. Section II describes the overall design methodology. Section III presents the full system implementation and the corresponding measurement setup. Experimental results are reported in Section IV and further analysed in Section V, including a comparative discussion of performance against existing works. Finally, conclusions are drawn in Section VI.

II. DESIGN METHODOLOGY

To integrate the RF switch into the unit cell, the design process focuses on generating the required load impedances at the selected via position, which determines the reflection coefficient of the unit cell under different operating states of the switch. The design process can be divided into two

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main stages. First, the influence of the loaded impedance on the unit cell response is analysed based on a predefined via location. Second, the desired impedance is realized through the integration of the RF switch.

For clarity, the term (R_C) used in this section denotes the conductor reflection coefficient, which represents simulated or measured reflection responds of the control circuitry. Whereas (R_{PW}) refers to the reflection coefficient of the unit cell under normal incidence of a plane wave.

A. OPERATING PRINCIPLE OF THE REFLECTIVE SURFACE

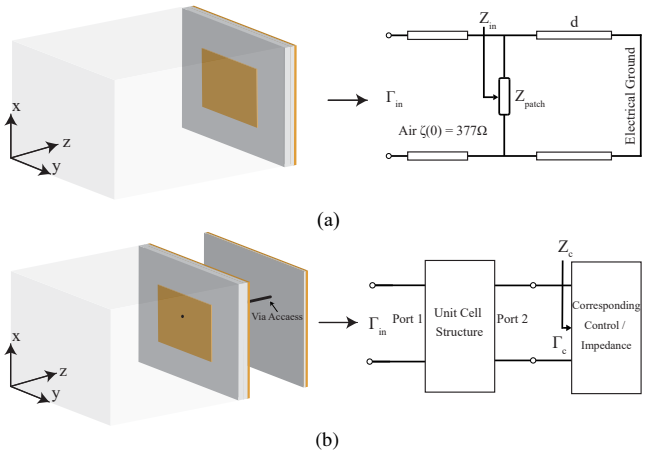


FIGURE 1. (a) Reflection coefficient of a patch unit cell under normal incidence in the z+ direction, with unit cell boundary condition. (b) reflection coefficient of the same unit cell with the integrated control board

A patch-array-based reflective surface can be modelled using a transmission-line circuit representation [31], as illustrated in Fig. 1(a). The complex reflection coefficient (Γ_{in}) of the surface is primarily governed by its input impedance (Z_{in}), which is equivalent to the parallel connection of the surface impedance (Z_s), governed by the periodic structure, and the impedance of the grounded dielectric substrate (Z_d). This relationship can be expressed as follows [32], [33]:

$$\Gamma_{in} = \frac{Z_{in} - \zeta_0}{Z_{in} + \zeta_0} \tag{1}$$

$$Z_{in} = \frac{Z_s Z_d}{Z_s + Z_d} \tag{2}$$

where ζ_0 is the impedance of the free space. The reflection coefficient can therefore be tuned by engineering either the surface impedance, the substrate impedance, or a combination of both. In conventional designs, surface geometry and substrate properties are optimized to achieve the desired reflection characteristics.

In contrast, the second approach used in this work introduces an additional load impedance integrated beneath the ground plane, which is coupled to the surface through a physical via, as shown in Fig. 1(b). This configuration provides greater design flexibility, enabling the integration of semiconductor devices, transmission lines, and other electronic components. By modifying the load impedances, the reflection coefficient of the surface can be dynamically controlled without altering the physical structure of the patch. The resulting structure can be represented with the concept of two-port network, expressed as follows [34]:

$$\Gamma_{in} = S_{11} + \frac{S_{12}S_{21}\Gamma_c}{1 - S_{22}\Gamma_c} \tag{3}$$

Based on the relation in (3), and under ideal conditions where S_{11} and S_{22} approach zero and S_{21} and S_{12} approach unity, the reflection coefficient of the unit cell Γ_{in} can be approximated as Γ_c. However, in practical implementations, non-ideal factors such as loss, parasitic coupling, and component tolerances introduce deviations from this ideal response, resulting in more complex reflection behaviour.

B. UNIT CELL DESIGN AND CONTROL MECHANISM

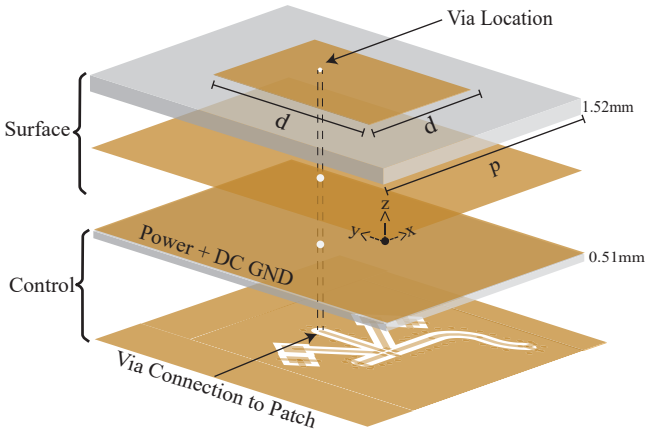


FIGURE 2. Unit cell structure and the corresponding control circuitry

The proposed unit cell consists of a square metallic patch with length of d = 14mm and a periodicity of p = 20 mm (approximately 0.33λ at the operating frequency). The structure is fabricated on a Rogers R4350B substrate with a thickness of 1.52 mm, dielectric constant ϵ of 3.66, and loss tangent δ of 0.004. Full wave simulation is performed in ANSYS HFSS using floquet port under normal incidence [35]. The result indicates a resonant frequency at 5.05 GHz with a reflection magnitude of 0.86 dB, as shown in Fig.3.

The patch unit cell is connected to the control layer through a vertical via, positioned at (0, 0.02λ, 0) relative to the centre of the patch, based on the coordinate system defined in Fig. 2. The selection of via locations in this work is guided by the findings in [36], which investigated the impact of via placement on the reflection coefficient of a patch unit cell. In [36], zero and infinite load impedances were modelled by connecting or disconnecting the via between the patch and the ground plane, respectively. The results demonstrated that strategic placement of the via, or the corresponding load impedance, within specific location

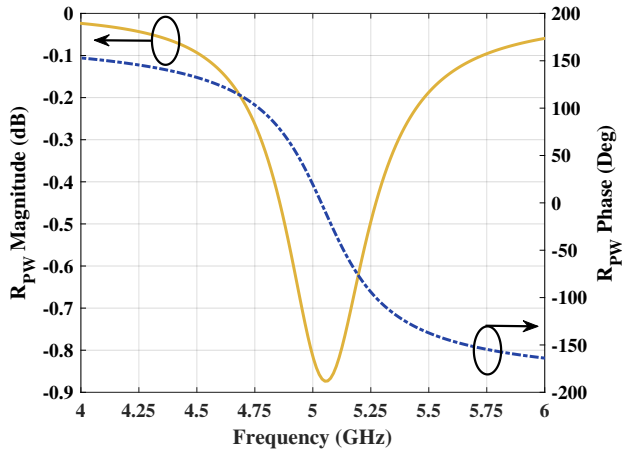


FIGURE 3. Simulated R_{PW} magnitude and phase response of the original patch unit cell

of the unit cell enables effective control on the reflection coefficient across a range of frequencies.

Fig. 4 illustrates the two operating modes of the RF switch. The overall impedance network consists of an RF switch integrated with the coplanar waveguide with ground (CPWG) transmission lines, with both ends terminated to ground. State switching is accomplished by selecting either the L2 or L3 branch of the CPWG line, while the inactive branch remains in a high-isolation state.

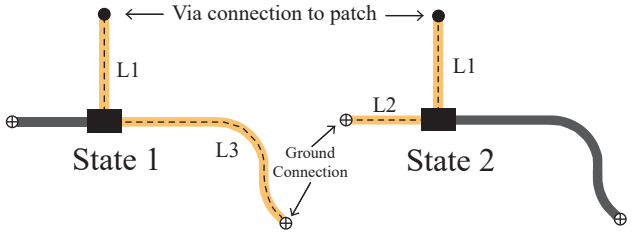


FIGURE 4. Two operating mode of the RF switch. The orange-highlighted path represents the active path selected by the applied control voltage

The total impedance at the starting point of L1 governs the reflection coefficient of the patch. This impedance results from a cascaded combination of the CPWG line L1, the SPDT switch, and the selected CPWG line L2 or L3, depending on the active path. The structure follows standard impedance transformation principles based on transmission line theory [34], expressed as:

$$Z_{in} = Z_i \frac{Z_{i+1}^{'} + jZ_i tan(\beta l_i)}{Z_i + jZ_{i+1}^{'} tan(\beta l_i)} \tag{4}$$

where Z_i denotes the impedance of i-th transmission line section, with corresponding phase constant β and length l_i. The term $Z_{i+1}^{'}$ is the equivalent input impedance of the subsequent section. Since both end of the L2 and L3 transmission line are terminated to the ground, the input impedance at the via can be tuned by adjusting the widths and lengths of the transmission lines. This approach facilitates rapid prototyping and design iteration. The final transmission line dimensions are summarized in Table 1, corresponding to two discrete impedance states.

TABLE 1. List of Parameters for CPWG transmission line

Parameter	Length (mm)	Width (mm)	Clearance (mm)
L1	3	0.3	0.12
L2	3.2		
L3	6.97		

C. IMPACT OF LOAD IMPEDANCE ON REFLECTION COEFFICIENT R_{PW}

A total of 90 discrete impedance values was computed using (4), based on sweeping the length l_i corresponding to electrical phases ranging from 0° to 180° in 2° intervals at a frequency of 5.05 GHz. These calculations are based on the initial assumption that the via encounters the impedance of a single CPWG transmission line of variable length terminated to ground. The computed impedances were modelled as a series RLC circuit and implemented as an RLC boundary between the via and the copper plane at the control layer in ANSYS HFSS, with a fixed resistance of 1 Ω. This process produced 45 distinct values of inductive impedance and 45 distinct values of capacitive impedance, each represented by a corresponding series RLC boundary. The impact of these impedances variations on the R_{PW} of the unit cell are summarized in Fig. 5.

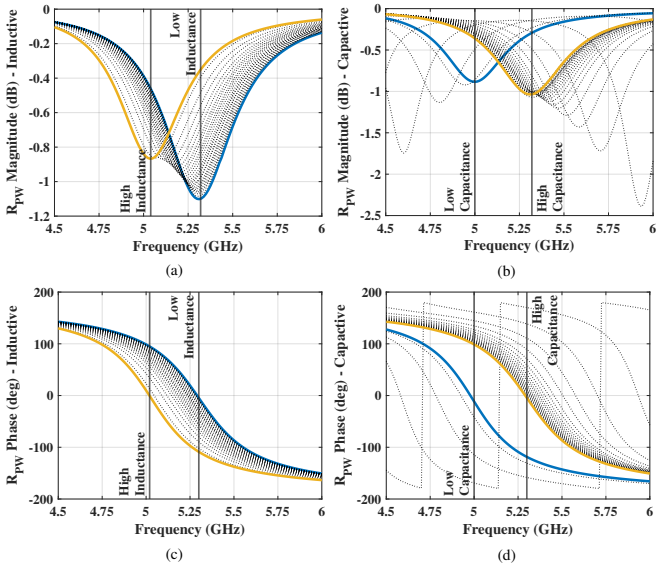
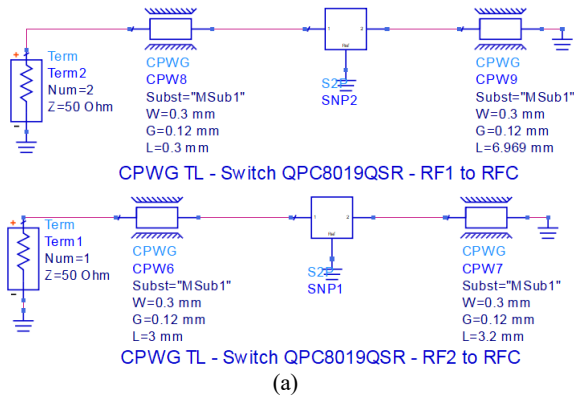


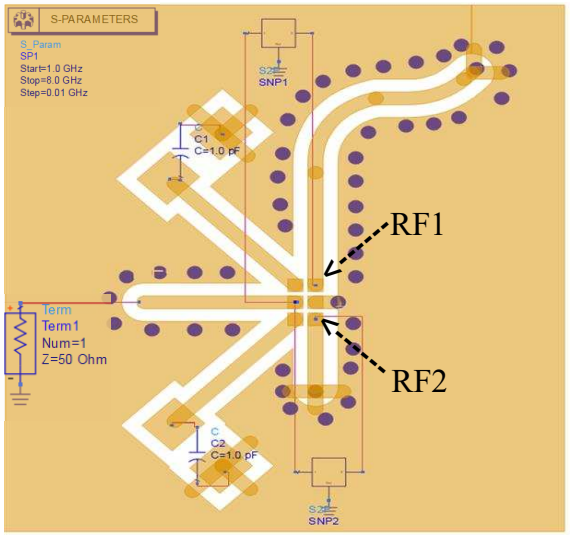
FIGURE 5. Simulated R_{PW} magnitude (a)-(b), and phase (c)-(d) based on the sweep of 45 inductive loads and 45 capacitive loads under TE polarization. Two highlighted curve are indication of minimum and maximum value of calculated inductance or capacitance

Based on the simulation, the magnitude and phase of the reflection coefficient can be effectively controlled by adjusting the load impedance at the via. A sweep of the RLC model with inductance values ranging from 0.302 pH to 0.91 nH produces an approximate 300 MHz shift in the unit cell's

resonant frequency. Similarly, sweeping the RLC model with capacitance values from 0.12 fF to 0.39 pF yields a non-linear frequency shift over 4.5 GHz - 6 GHz, enabling a wide range of tuneable phase responses. This analysis forms the foundation for the initial impedance point selection used in the proposed design.



(a)



(b)

FIGURE 6. ADS simulation: (a) schematic-level impedance selection, and (b) EM simulation incorporating the S-parameters of the RF switch, with the impedance evaluated at terminal 1

To replicate the desired impedance using the integrated RF switch, Advanced Design System (ADS) was employed in conjunction with the switch's S-parameter model, shown in Fig. 6. A co-simulation approach combining schematic and EM model was used to select the required impedance values by adjusting the physical dimensions of the CPWG lines.

Based on the available impedance range and the required surface functionality, two effective impedance points were identified at the patch resonant frequency of 5.05 GHz, as indicated by red points in Fig. 7. These two impedance points correspond to the values seen by the patch through the physical via when the SPDT RF switch is configured in state 1 or state 2.

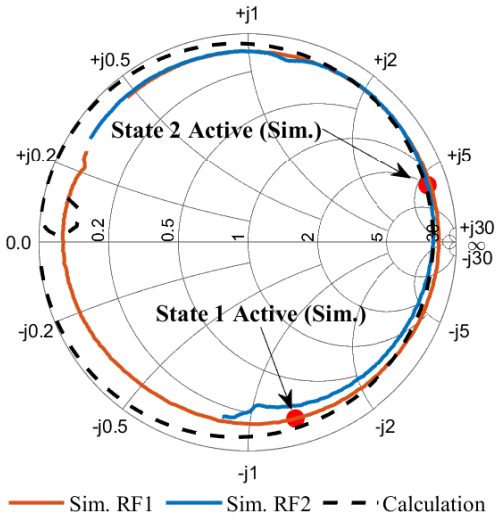


FIGURE 7. Smith chart of simulated R_C obtained from ADS EM simulation. The red points indicate the impedance at 5.05 GHz when state 1 or state 2 is active. RF1 and RF2 correspond to the respective RF ports in Fig. 6

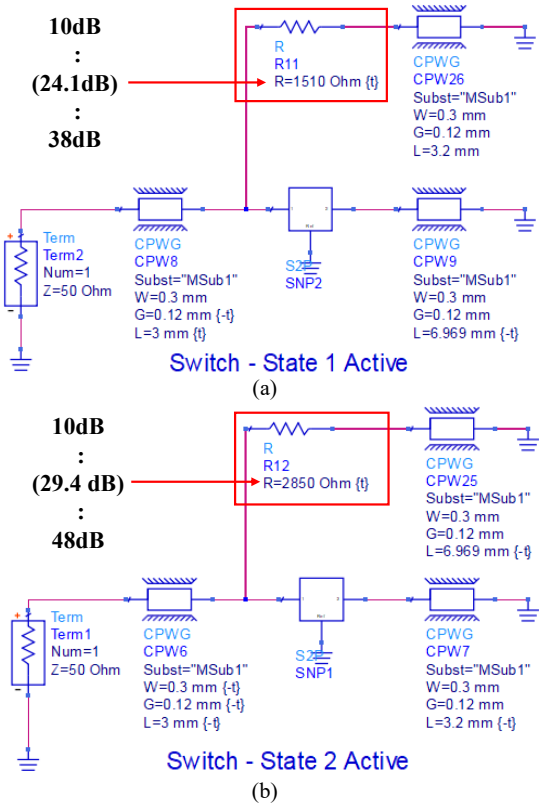


FIGURE 8. Schematic of the impedance model with a single resistor representing the inactive path isolation. (a) State 1 and (b) State 2 correspond to the operating modes of the switch shown in Fig. 4

D. IMPACT OF FINITE ISOLATION ON IMPEDANCE

In each operating state, the inactive RF port remains in high isolation. At 5.05 GHz, the isolation of the inactive RF port is specified as 24.1 dB and 29.4 dB for state 1 and state 2, respectively [24]. The isolation is modelled using a series resistor, based on a simplification of the well-known series-

FET (Field-Effect Transistor) based architecture of many practical RF switches. The resistor value was tuned to match the isolation values at 5.05 GHz. For sensitivity analysis, four additional isolation values were also defined and modelled for each state, spaced at 7 dB intervals for State 1 (covering 10 dB to 38 dB) and 9.5 dB intervals for State 2 (covering 10 dB to 48 dB).

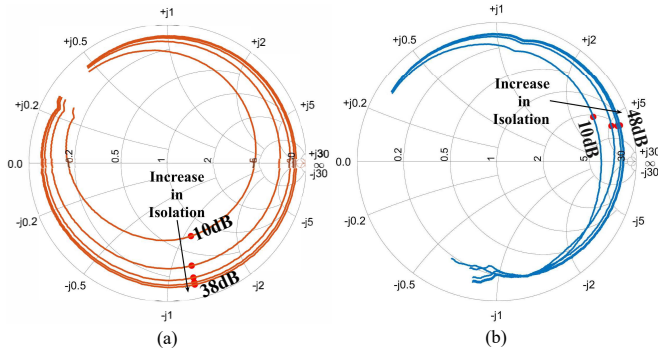


FIGURE 9. Simulated R_C based on ADS schematic in Fig. 8. The arrow indicates the shift in active-path impedance at 5.05 GHz due to change in the switch's off state isolation, (a) State 1 active and (b) State 2 active

Fig. 9 illustrates the change in effective impedance resulting from variations in the isolation of the inactive path. As the isolation decreases, additional loss is introduced into the overall system, causing a noticeable shift in the impedance at 5.05 GHz. The largest change occurs between the 10 dB isolation case and the next higher isolation level for both states. Beyond an isolation of approximately 25 dB, the incremental impact becomes minimal.

The obtained impedances were applied to the unit cell and simulated in ANSYS, and the resulting difference in the R_{PW} magnitude and phase due to isolation variation are shown in Fig. 10, referenced to the specified isolation level. The most significant deviation occurs at an isolation of 10 dB, yielding maximum R_{PW} magnitude differences of -2 dB and -1 dB, and phase variations of 5° and 17° for State 1 and State 2, respectively. Under this simplified isolation model, the influence of finite RF switch isolation on the unit cell response becomes negligible once the isolation exceeds approximately 20 dB, with magnitude variations within ±0.5 dB and phase deviations within ±5°.

E. PRACTICAL IMPEDANCE MEASUREMENT

Multiple control boards were fabricated with the selected RF switch to validate the design approach descried above. For consistency and mechanical stability, all prototypes were implemented on a Rogers R4350B substrate with a thickness of 1.52 mm. The lengths each CPWG line were systematically varied across the different boards to enable a practical evaluation of the achievable impedance values.

The conductor reflection coefficients R_C were measured at the via connection point of L1 using a calibrated vector network analyser (VNA). The measured R_C results revealed

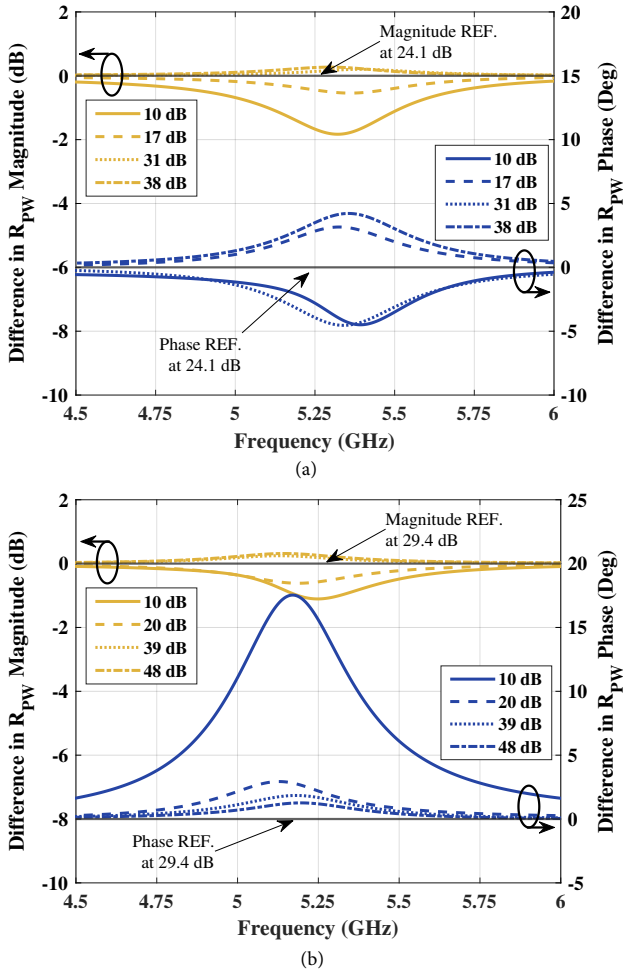


FIGURE 10. Differences in R_{PW} magnitude and phase resulting from isolation variation on the inactive path: (a) State 1 active, using 24.1 dB as the reference. (b) State 2 active, using 29.4 dB as the reference

extra phase shifts and losses across all configurations, independent of the specific CPWG line parameters.

To reconcile discrepancies between simulation and measurement, the CPWG line lengths were re-optimized based on the measured response, resulting in the final dimensions reported in this work. Fig. 11 presents the measured impedance compared with the simulated results ADS, the additional loss and phase contributions were accounted. These deviations are attributed primarily to a few millimetres of excess line length and clearance variations arising from manufacturing tolerances.

The capacitive response associated with state 2 induces an approximate 0.5 GHz upward frequency shift accompanied by a moderate reduction in reflection magnitude. In contrast, state 1 maintains a reflective response, closely matching the baseline performance of the patch. The resulting effect of unit cell under normal plane-wave incidence due to the impedance from both states is presented in Section IV Experimental Result.

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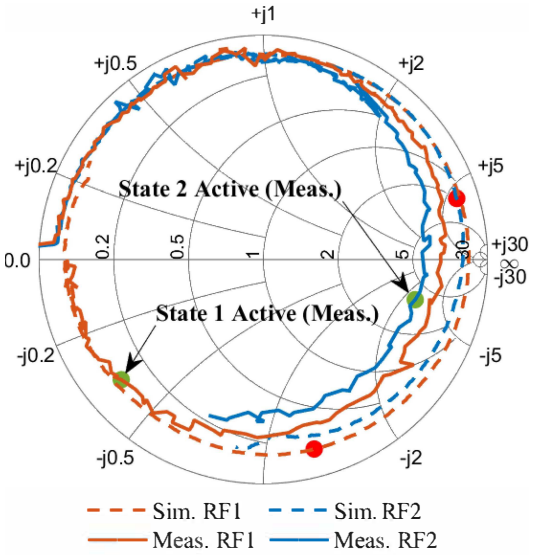

FIGURE 11. Smith chart of simulated and measured R_C with finalised parameters presented in this work, adjusted to account for discrepancies between measurement and simulation. RF1 and RF2 correspond to the respective RF ports of the switch in Fig. 6

III. SYSTEM IMPLEMENTATION AND MEASUREMENT SET-UP

To minimize control complexity and reduce the number of general-purpose-input-output (GPIO) pins, the full system prototype incorporates additional control units for individual unit cell control.

A. HARDWARE INTEGRATION AND CONTROL IMPLEMENTATION

Fig. 12 illustrates the configuration of the proposed unit cell in 4 × 4 array and the corresponding control circuitry. The control circuit incorporates two 8-bit shift registers (SN74LV595BMPWREP, Texas Instruments) connected in series, the outputs of the registers are routed through two 8-bit voltage level translators (SN74LXCH8T245PWR, Texas Instruments), which generate the required 1.8 V control voltage for each RF switch. All shift registers are driven by a single ESP32 microcontroller, enabling centralized and synchronized control of the entire array. A control circuit for a 4 × 4 array was measured to have a static power consumption of 3.7 μW when all switches were configured in state 1 (V_{ct} = 0), while the ESP32 consumes 125.4 mW in its idle state when powered directly at 3.3 V.

The complete RIS surface is constructed by assembling four of sub-arrays, forming an overall 64 unit cell prototype in 8 × 8 unit cell arrangement, with total surface dimension of 160 mm × 160 mm or approximately 2.7λ × 2.7λ in electrical length. The modular architecture simplifies both hardware integration and control scalability. Fig. 13 shows the fully assembled prototype. The extended edges of the board provide additional mechanical stability to support the structure during measurement and handling.

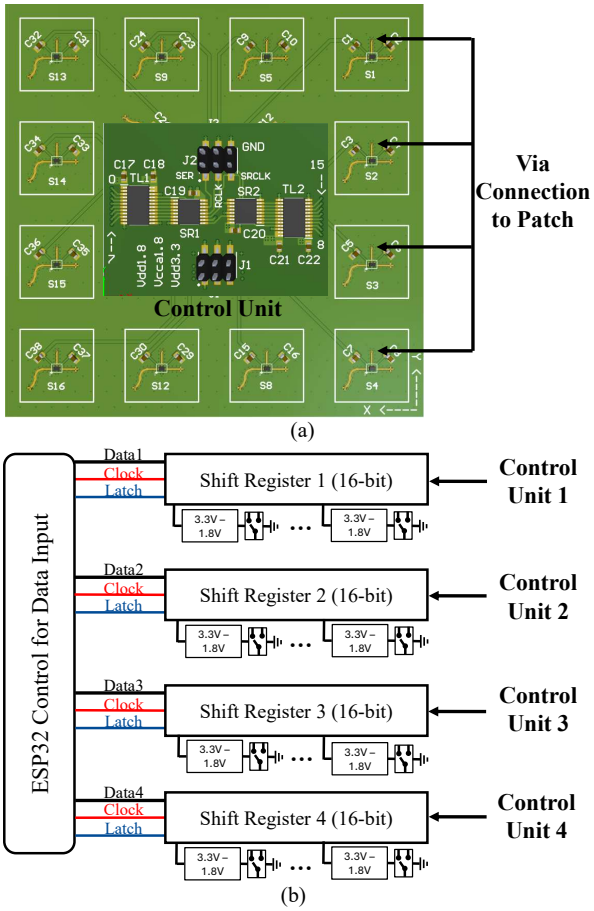

FIGURE 12. Control implementation: (a) rear view of the 4 × 4 array with the control circuitry and (b) corresponding full surface control logic

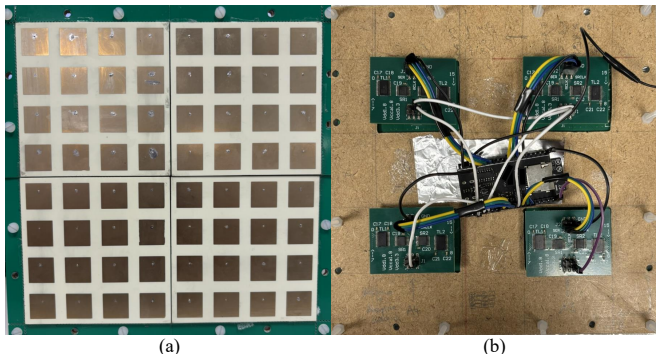

FIGURE 13. Fully assembled system: (a) front view and (b) rear view

B. MEASUREMENT SETUP

Measurements were carried out in an NRL arch anechoic chamber using the setup shown in Fig. 14. Both the transmitting and receiving horn antennas were connected to a Agilent Technologies E8362B, with the E-field oriented along the y-axis (TE polarization). The receiving horn was positioned to capture the reflected wave from the prototype surface under normal incidence.

The system calibration was conducted with the presence of all the required equipment, a 160 mm × 160 mm metal

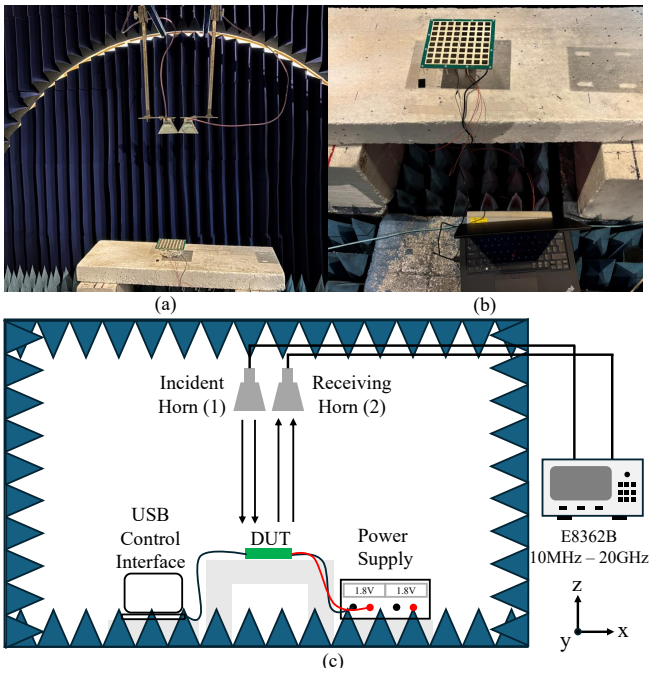

FIGURE 14. Measurement setup: (a)-(b) device under test inside the NRL arch anechoic chamber, and (c) detailed schematic of the setup

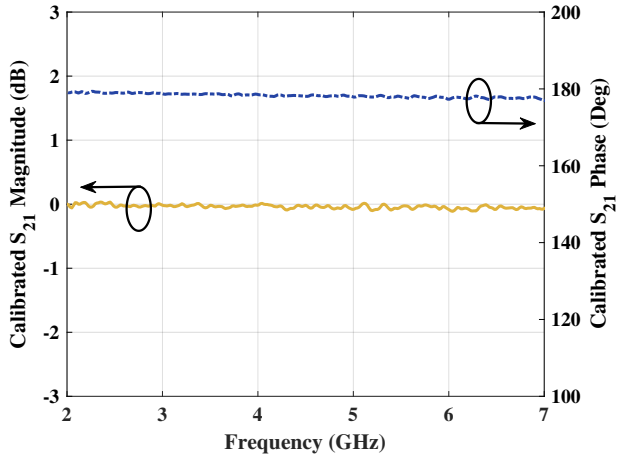

FIGURE 15. Reflection coefficient of calibrated system with surface sized metal plate, S_{21} is reference to number of horn antennas in Fig. 14

plate was used to calibrate the reflection responds prior to the measurement, result illustrated in Fig. 15, which ensure the effect of extending edge from the surface is also accounted where possible.

IV. EXPERIMENTAL RESULTS

All measured reflection magnitude and phase in this section are referenced to the surface reflection coefficient under normal-incidence TE-polarized plane wave excitation, using the measurement setup described in Fig. 14. The corresponding simulation results are obtained using the two measured impedance point from Fig. 11. The results are organized into two parts. Part A focuses on validating the reflection coefficient of the surface when all RF switches are configured to either state 1 or state 2, determined by the applied control voltage V_{ct}.

Part B builds upon this baseline by using the measured reflection magnitude and phase under the two impedance states to further investigate and evaluate a range of pattern-based surface configurations. This analysis provides insight into the impact of spatial switching patterns on the reflection characteristics of the surface.

A. PERFORMANCE EVALUATION: FULL SURFACE CONFIGURATION

The measured reflection magnitude and phase in Fig. 16 exhibit a frequency shift of approximately 500 MHz between the two states, accompanied by a corresponding change in reflection magnitude and an approximate 180° phase difference at 5.05 GHz. These results show excellent agreement with the simulated response, validating the effectiveness of the impedance-controlled design in achieving reconfigurable reflective surface functionality. In particular, the surface exhibits absorptive behaviour at 5.50 GHz when switched from the state 1 to state 2.

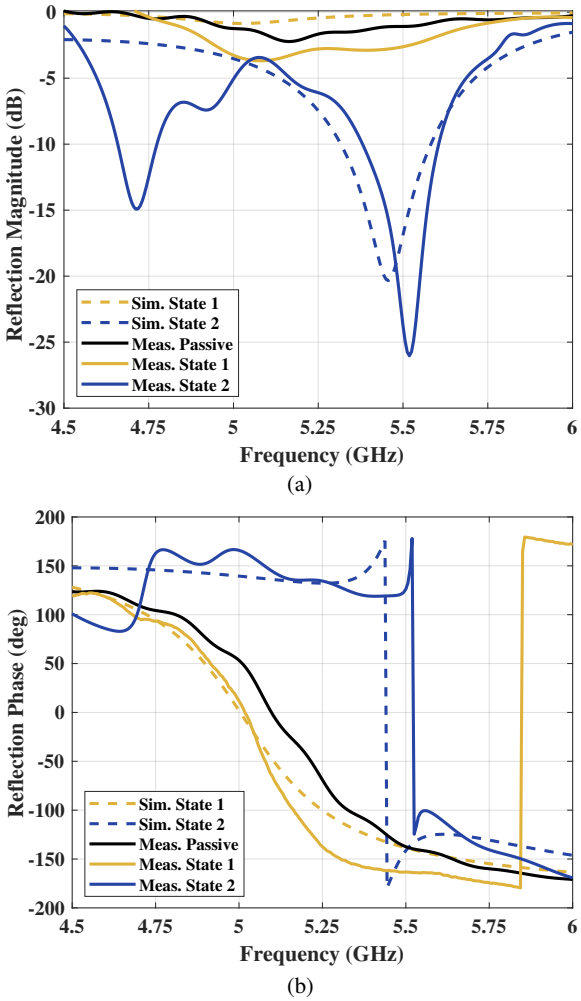

FIGURE 16. Reflection (a) magnitude and (b) phase responses with all switches operating between state 1 and state 2

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Additional measurements were conducted with all power and control disabled, during which the surface operated in a purely passive mode. The measured response in this configuration closely matched to all switches configured in the state 1, with a reduced loss. This difference is attributed to the parasitic loss introduced by the active switching components and the associated measurement setup.

B. PERFORMANCE EVALUATION: PATTERN BASED SURFACE CONFIGURATION

In the pattern-based measurements, a high control voltage V_{ct} is denoted as '1' (represented in blue), which configures the unit cell into state 2, whereas a low V_{ct} corresponds to state 1 and is shown as blank in the figures presented in this section. During these measurements, an absorptive response is defined as a reduction of at least 10 dB relative to the measured reflective response when all switches are operating in state 1.

The evaluated patterns are characterized by the spatial distribution of the '1' coding across the surface. The most effective configurations were found to be a set of modified edge-based patterns, derived from progressive activation of the outermost unit cell ring. These configurations are referred to as the '*incremental border*', '*single ring*', and '*nested ring*'. For clarity, the ring size used in this section refers to the perimeter of a complete square ring composed of four equal sides, measured from the centre point of each unit cell. All dimensions are expressed in terms of electrical size.

1) Incremental Border Pattern

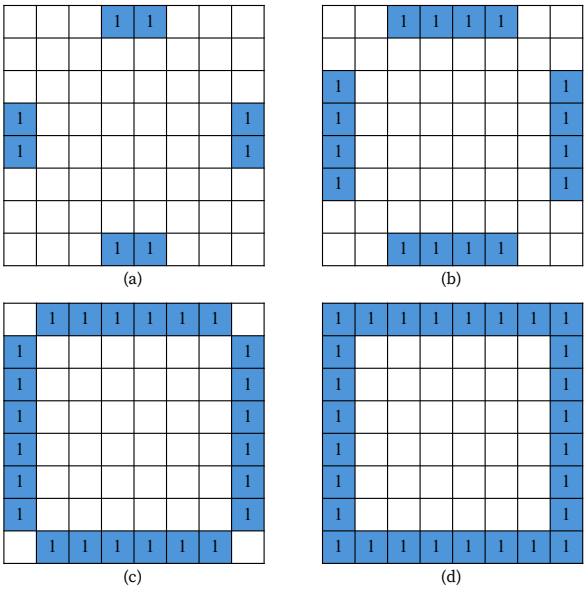

FIGURE 17. Incremental border configuration, where the loop becomes fully closed as the pattern progresses from (a) to (d)

Under this configuration, the applied control sequence progressively increases the number of active '1' unit cells along the edge of the surface, as shown in Fig. 14. The total number of activated switches begins at 8 and increases until all 28 switches at the edge are toggled to '1', forming the complete ring pattern with size of 9.24λ, shown in Fig. 17(d).

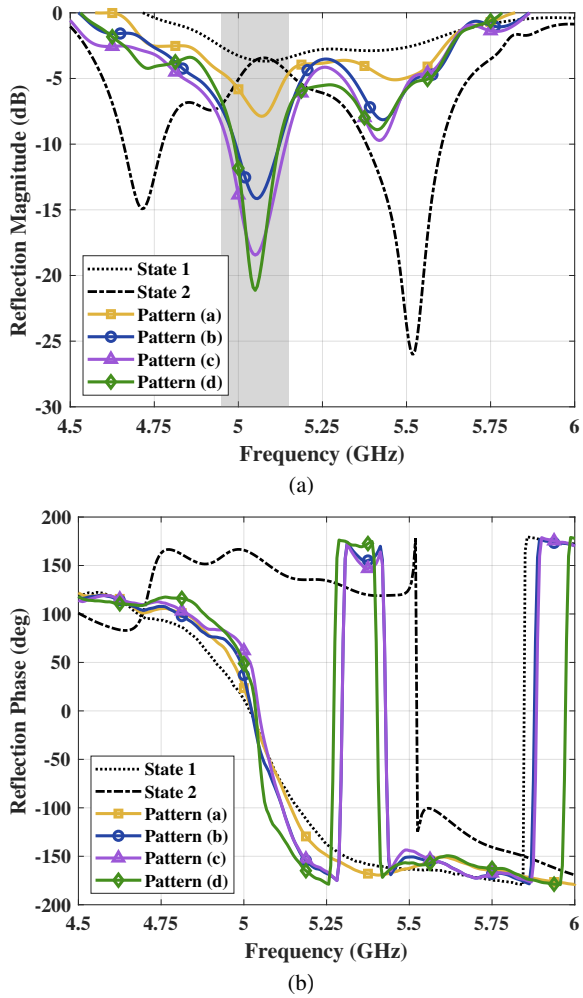

FIGURE 18. Measured reflection (a) magnitude and (b) phase responses based on pattern configuration shown in Fig. 17

The measured results shown in Fig. 18 demonstrate that varying the number of active unit cells along the outer edge has a clear impact on the reflection magnitude at the patch's resonant frequency at 5.05 GHz. This behaviour is distinct from the magnitude variation near 5.50 GHz, which is primarily governed by full-surface switching operation.

As the number of '1' elements increase from Fig. 17(a) to Fig. 17(d), a continuous decrease in reflection magnitude at 5.05 GHz is observed, starting at -7.8 dB for the pattern in Fig. 17(a), and decreasing to -13.3 dB and -18.4 dB for the patterns in Fig. 17(b) and Fig. 17(c), respectively. The minimum value of -21 dB is achieved when all outer-edge switches are activated, shown in Fig. 17(d).

2) Single Ring Pattern

Four single-ring configurations were defined and tested. The size of the ring are changed in the following orders, 9.24λ, 6.6λ, 3.96λ and 1.32λ, which effectively decrease the number of "1" coded element from 28 in the outermost ring to 4 in the innermost configuration, as illustrated in Fig. 19(a) to Fig. 19(d).

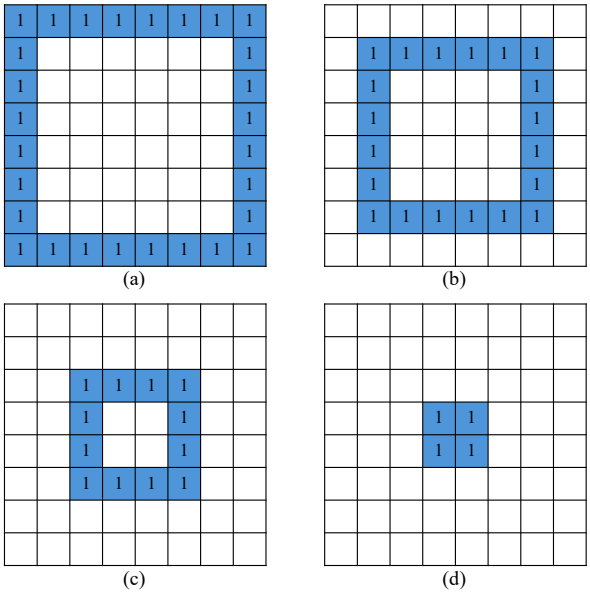

FIGURE 19. Single ring configuration with variation on size of the ring: (a) 9.24λ, (b) 6.6λ, (c) 3.96λ and (d) 1.32λ

The measured results in Fig. 20 indicate that the magnitude response at 5.05 GHz exhibits no consistent variation trend as the size of the ring decrease. A changes of approximately -5 dB in reflection magnitude is observed between the configurations shown in Fig. 19(b) and Fig. 19(c). The smallest ring pattern in Fig. 19(d), containing only four active unit cells, produces negligible variation in reflection magnitude, less than 1 dB compared with the fully reflective (all state 1) condition.

3) Nested Ring Pattern

In the nested configurations, two rings were nested in three different arrangements. The outer ring was kept fixed, while additional inner ring with size of 6.6λ, 3.96λ and 1.32λ are coded into the surface, illustrated in Fig. 21.

The results presented in Fig. 22 demonstrate that introducing an additional inner ring preserves the absorptive behaviour at 5.05 GHz, which is primarily governed by the outer ring. However, activating additional '1' coded unit cells toward the surface centre introduces two additional level of magnitude control at 5.50 GHz, with the degree of change directly related to the size of the inner ring. A distinct behaviour is observed in the configuration shown in Fig. 21(a). The change in reflection magnitude at 5.05 GHz is limited to approximately –2 dB, which is relatively small

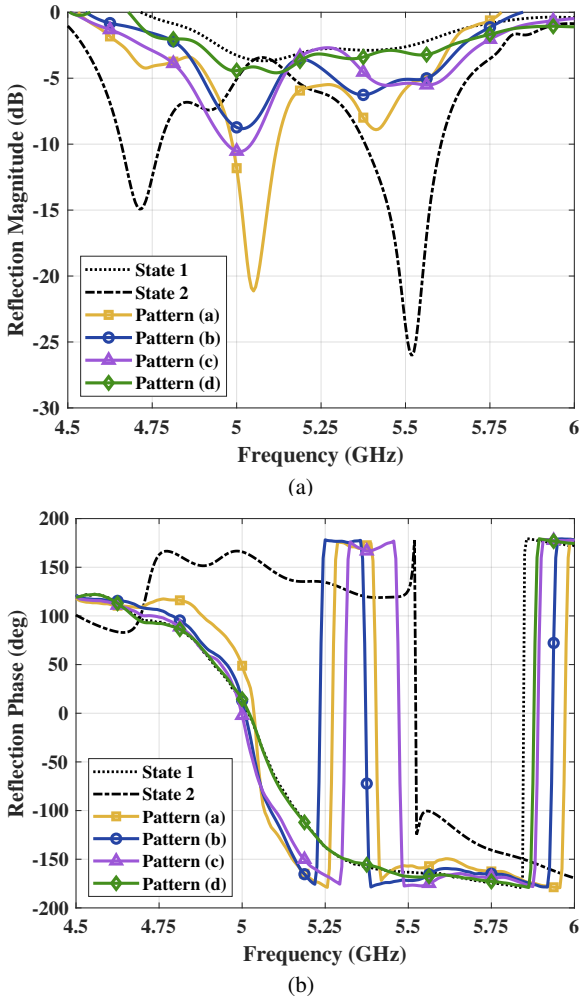

FIGURE 20. Measured reflection (a) magnitude and (b) phase responses based on single-ring patterns shown in Fig. 19

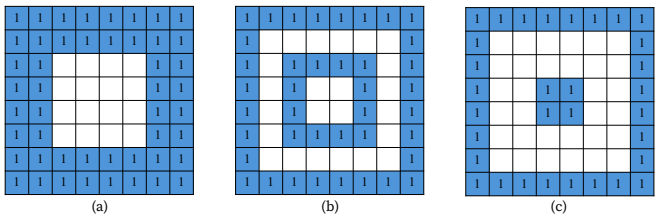

FIGURE 21. Nested ring configuration with variation on size of the inner ring: (a) 6.6λ, (b) 3.96λ and (c) 1.32λ

compared to the results obtained for the configurations in Fig. 21(b) and Fig. 21(c). However, the absorptive response now shifts toward 5.50 GHz, with the reflection magnitude and phase closely match those observed when all surface elements are coded as '1' (State 2).

V. DISCUSSION

The discussion is organized into three subsections: Part A provides an overview on the measured results, Part B evaluates the system's performance and Part C explores potential applications enabled by the proposed surface.

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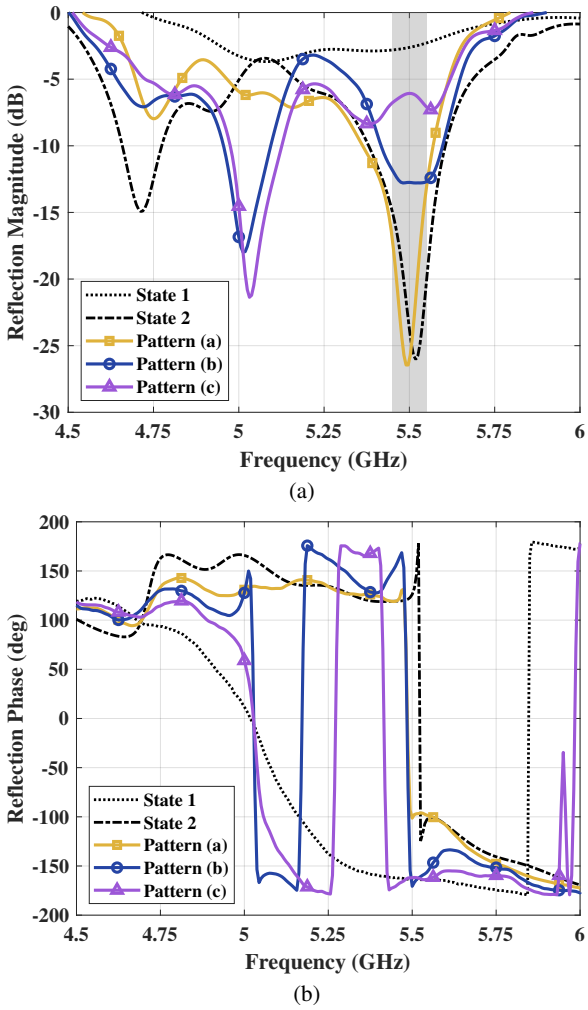

FIGURE 22. **Measured reflection (a) magnitude and (b) phase responses based on the nested-ring patterns shown in Fig. 21**

A. OVERVIEW ON EXPERIMENTAL RESULTS

The sets of patterns shown in Fig. 17 and the corresponding result in Fig. 18 demonstrate that the proposed RIS is capable of precise magnitude control at 5.05 GHz through selective activation of edge unit cells, thereby providing an additional degree of control beyond full surface switching operation.

The ring-based patterns were further investigated by implementing a series of single ring configurations, in which the ring size was progressively reduced toward the centre of the surface. The resulting configurations, shown in Fig. 19 with their corresponding measurements in Fig. 20, indicating that that edge-region configuration plays a dominant role in controlling the surface's reflection magnitude at 5.05 GHz.

Building upon the single ring analysis, nested ring configurations were further investigated to evaluate the influence of multiple ring activation regions on the reflection behaviour of the surface, result detailed in Fig 22. When the focus shifts to reflection magnitude control at 5.50 GHz, the nested ring configurations exhibit similar controllable behaviour to that of the incremental border patterns, confirming that the reconfiguration of multiple rings can effectively tune the reflection response across frequencies.

The various pattern-based configurations investigated in this work demonstrate that the proposed surface is capable of precise reflection magnitude control at both 5.05 GHz and 5.50 GHz. At 5.05 GHz, these patterns provides magnitude quantization over a range of -3 dB to -21 dB, with an averaged step size of approximately 5 dB.

Importantly, the pattern in Fig. 21(a) with corresponding result in 22 indicate that comparable performance to full-surface operation can be achieved by activating only a subset of unit cells (75 % in this case). This reduction in active elements directly translates to lower control complexity and reduced power consumption, particularly when deployed at scale. It further enhances the low-power characteristics of the RF-switch-based architecture and improves thermal concealment through reduced heat dissipation.

Furthermore, as observed in Fig. 18, the surface response in purely passive mode closely matches that of the reflective mode (State 1). This indicates that the switches can be selectively powered off without significantly affecting the EM performance of the surface, offering an additional means to reduce system level power consumption. Building on this observation, the results of various ring-based pattern configuration further demonstrate the potential for implementing a 'thinned' RIS, in which only a subset of unit cells requires active control. The remaining unit cells across the surface may employ simplified control, remain in a fixed state or even stay fully passive without any control mechanism, thereby reducing the hardware complexity and power consumption while maintaining desired surface functionality.

B. EVALUATION ON POWER CONSUMPTION AND BIAS COMPLEXITY

1) Power Consumption and Thermal Implications

For a switch operating from a 1.8 V supply, the measured supply current is 37 μA. Accordingly, a single switch configured in state 1 (V_{ct} = 0) consumes approximately 66 μW. When the switch is toggled to state 2 (V_{ct} = 1.8 V) an additional current of 0.2 μA is drawn, resulting in an extra 0.36 μW of power consumption. Based on this measurement, an 8 $\times$ 8 surface exhibits a total tunable elements power consumption of approximately 4.22 mW and 4.24 mW when all switches operate in State 1 and State 2, respectively. When the associated control circuitry is included, the total static power consumption of the complete system is approximately 135 mW.

A performance comparison between varactor- and PIN-diode-based implementations, including power consumption, is summarized in Table 2. PIN-diode-based designs typically exhibit the highest element level power consumption, as each diode often requires forward bias currents in the milliampere (mA) range. In contrast, varactor diodes consume negligible power under reverse bias. However, precise and stable tuning of varactors requires well-regulated bias voltages, which are

commonly generated using pulse-width modulation (PWM) drivers with level regulators [14] or digital-to-analogue converters (DAC) with operational amplifiers [22]. These auxiliary circuits introduce significant power consumption at the system level.

Beyond energy efficiency, the low static power consumption of the RF switch has direct implication on the thermal stability. With negligible self-heating, the device temperature remains close to the ambient temperature, independent of the switching state. This predictable thermal behaviour improves system robustness and avoids the need for bulky thermal management hardware such as heat sink or active cooling.

For a hypothetical 100×100 element RIS with one tunable device per element, the proposed RF-switch-based design would generate less than 1 W of aggregate heat. This low thermal load effectively removes thermal constraints, avoids non-uniform temperature distributions, and makes the approach well suited for large scale RIS deployments.

In contrast, a typical PIN-diode-based design ($\approx$10 mW per element) would generate an aggregate thermal load of approximately 100 W. Managing such thermal load requires addtional engineering and may lead to non-uniform temperature distributions across the surface, potentially degrading performance consistency in large-scale arrays.

The varactor-based design of the same scale introduce a substantial hardware overhead and system-level static power consumption that negates the efficiency benefits of the element itself.

2) Biasing Complexity and Switching Speed

Quantitative switching speed data are often not explicitly reported in the RIS literature, making direct numerical comparison across different tunable elements difficult. Consequently, the switching speed comparison presented in Table 2 relies on a qualitative assessment. This assessment considers the fundamental physical mechanisms and practical limitations associated with biasing and control circuitry, and is intended to provide a relative comparison with respect to the proposed work. It is noted that the classifications do not apply universally to all designs, as implementation details can significantly influence achievable performance.

The RF switches employed in this work supports switching speed of up to 80 ns [24]. The associated shift registers are specified with a typical clock frequency of 105 MHz [37]. Driven by the ESP32's SPI interface, which supports clock frequency of up to 80 MHz, the total time taken to updating all elements within a 4×4 sub-array in approximately 226 ns, accounting for 16-bit data transfer, latch pulse timing, and propagation delays introduced by the voltage-level translators. Higher update rates could be achieved by replacing the controller that supports a faster SPI operation.

PIN diodes exhibit fast switching behaviour at the device level, in range of nanoseconds. In practice, however, the achievable switching speed is constrained by the time required to inject or remove the charge carriers from the intrinsic region, a process that demands a large instantaneous currents and leads to increased power consumption and driver complexity [38], [39]. In RIS applications, where straightforward digital ON-OFF control is commonly adopted for simplicity, these practical considerations inherently limit the achievable switching speed.

Varactor diodes are generally considered as a fast tunable elements due to their voltage controlled capacitance. However, in practical RIS implementations, the effective switching speed between discrete capacitance states is governed by the settling time of the biasing circuitry, such as DAC, which is typically on the order of microseconds and increases with precision of the DAC [40]. As a result, varactor-based systems are often characterized by slower system level reconfiguration speeds and increased hardware complexity, as individual unit cell control typically requires a dedicated DAC per element.

C. POTENTIAL USE CASE AND APPLICATIONS

1) Radar Cross Section (RCS) Control

The significance of the RCS (σ) is defined by the fundamental radar range equation, which establishes the quantitative link between a target's scattering properties and the radar detection distance [44], expressed as:

$$R_{max} = \sqrt[4]{\frac{P_t G^2 \lambda^2 \sigma}{(4\pi)^3 P_{min}}} \tag{5}$$

where R_{max} denotes the maximum detection range, and remaining parameters, P_t, G, λ, and S_{min} are radar system dependent and represent the transmitted power, antenna gain, wavelength and minimum sensitivity respectively. For a planar surface with physical area (A) under normal incidence, the monostatic RCS can be further expressed as as a function of reflection magnitude [45]:

$$\sigma = \frac{4\pi A^2}{\lambda^2} |\Gamma|^2 \tag{6}$$

The demonstrated reflected magnitude control at 5.05 GHz and 5.50 GHz suggests the potential for tunable RCS reduction. Assuming the radar parameters in (5) and remaining parameters in (6) remains constant, the relationship can be simplified as $R_{max} \propto \sigma^{0.25}$. To clearly illustrate the impact of RCS variation, the relative change in detection range can be written as:

$$\frac{R_{new}}{R_{old}} = \left(\frac{\sigma_{new}}{\sigma_{old}} \right)^{0.25} \tag{7}$$

Based on (7), halving the detection range ($R_{new} = 0.5 R_{old}$) requires reducing the RCS by a factor of 16, corresponding to a 12 dB reduction relative to a perfectly reflective target (0 dB return loss). For the controllable return loss range between 3 dB and 21 dB achieved in this work, the corresponding maximum detectable range is reduced to

TABLE 2. Comparison with PIN-diode- and Varactor-diode-based reconfigurable surfaces

Work	Freq. (GHz)	Tuneable Elements	UC Power Consumption*1 (mW)	Total Power Consumption*2 (W)	Biasing Complexity	Switching Speed	Available Phase Difference	Quantized Phase Step	Magnitude (dB) Quantitation Range | Step
[14]	5.80	2 Varactor Diodes	0.0016	0.934	High	Slow	0°-180°	180°	-
[17]	5.90	3 PIN Diodes	18	2.8	Low - Medium	Moderate	0°-270°	90°	-
[23]	5.30	1 SP8T Switch	62	N/A	Medium	Moderate - Fast	0°-360°	51.42°	-
[41]	12.5	2 PIN Diodes	13.3	2.55	Low	Moderate	0°-180°	180°	-
[42]	4.9	2 Varactors Diodes	N/A	N/A	N/A	Slow	0°-315°	45°	2-8† | 6
[43]	4.15	4 Varactor + 2 PIN Diodes	N/A	2.662	Very High	Slow	0°-426°	Continuous	3-17.3 | Continuous
This Work	5.05 /5.50	1 SPDT Switch	0.063	0.135	Low	Fast	0°-180°	180°	3-21‡ | 5

N/A: Not available from the referenced context

* Reported maximum static power consumption: *1 per unit cell (UC), *2 the prototype

† Converted from the reported normalized amplitude levels of 0.4 and 0.8 in the referenced work

‡ The available reflection magnitudes achieved through surface pattern configuration at frequency of 5.05 GHz

approximately 84% and 30% of the baseline value, respectively. as illustrated in Fig. 23. Such reduction implies that radar receiver must operate closer to the scatter object to achieve detection. These results demonstrate the potential applicability of the proposed surface for RCS management and radar-surface interaction scenarios.

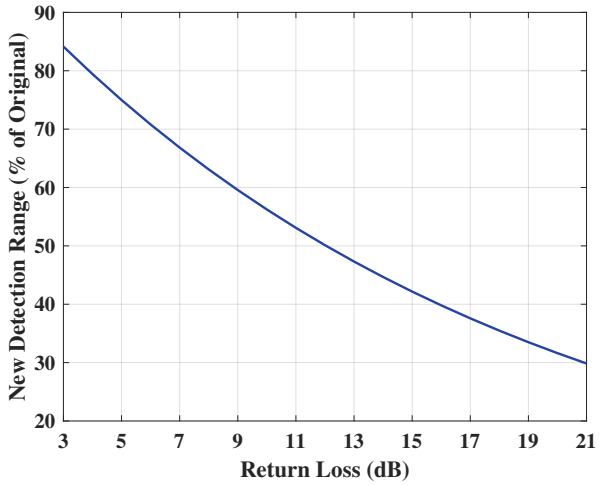

FIGURE 23. Theoretical reduction in the detection range based on (7), the detection range is normalised to a baseline target with 0 dB return loss

2) Backscatter Communication

The proposed surface is also well suited for backscatter communication applications. The fundamental operating principle of backscatter systems [46] is closely related to that of reflective RIS, in which information is encoded onto incident EM waves through controlled changes in the reflection coefficient. At 5.05 GHz, the two distinct phase states allow for Binary Phase Shift Keying (BPSK) modulation during full surface operation. Furthermore, the demonstrated magnitude control suggests the feasibility of amplitude-based modulation schemes, such as multi-level Amplitude Shift Keying (ASK). By utilizing the distinct reflection magnitude levels identified through the pattern analysis, the surface could support four level amplitude shift keying (ASK), enabling the transmission of 2 bits per symbol.

This versatility, combined with the inherently low power consumption and fast switching capability, makes the proposed surface a promising candidate for energy constrained backscatter communication systems.

VI. CONCLUSION

To the best of the authors' knowledge, this work presents the first demonstration of an RIS capable of selective magnitude control at two distinct frequencies, utilizing an SPDT RF switch as the tuneable element. The proposed impedance selection methodology has been validated through both full-wave simulations and complete system-level implementation. The fabricated prototype demonstrate the initial 1-bit (0°-180°) reflection phase control at 5.05 GHz and reflective-absorptive mode switching at 5.50 GHz under full surface operation. In addition, multi-level magnitude control at both frequencies is achieved through ring-based geometric patterns configuration. The RF-switch-based RIS presented in this work offers a well-balanced trade-off among power

consumption, biasing complexity and switching speed when compared with varactor- and PIN-diode-based RIS designs. Collectively, these results highlight the strong potential of the proposed surface for low-power programmable surfaces, with promising applications in RCS control and backscatter communication.

ACKNOWLEDGMENT

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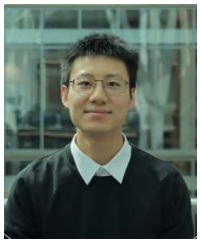

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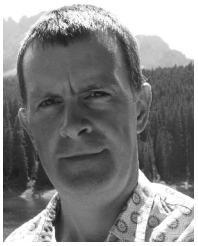

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