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Power Allocation Strategy for Hybrid Energy Storage Systems in DC Microgrids With Differential Power Processing Technique

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Abstract

Renewable energy resources (RESs) are gaining popularity as a means to reduce carbon emissions and meet the growing global power demand. Hybrid energy storage systems (HESSs), which integrate both battery energy storage systems (BESSs) and supercapacitors (SCs), are essential for maintaining a balance between RESs power generation and load consumption. BESSs typically address low-frequency power fluctuations, while SCs compensate for high-frequency variations. To effectively manage this, the converters of both BESSs and SCs must be capable of delivering the required full power, necessitating high power-ratings, as well as leading to high installation cost and power loss. To address this issue, this paper proposes a power allocation strategy for HESSs based on differential power processing (DPP) technique without compromising power allocation performance while significantly reducing the power-ratings of converters. Firstly, the inverted bidirectional buck converters are introduced to function as a front-end converter and subsequent DPP converters. Secondly, a modified droop control is implemented based on a triple-loop control algorithm to ensure the fast tracking of the reference current of battery/SC. Thirdly, the stability of the proposed DPP-based framework is analyzed. Finally, the performance of the proposed control framework is validated through hardware-in-loop (HIL) testing. The stability shows that the parameters of equivalent electric circuit models of both the battery and SC have no impact the system dynamics, thereby simplifying the controller design. The test results show that the proposed DPP-based framework achieves the power-sharing among HESSs and DC bus voltage regulation with power-ratings of the converters reducing to less than 15 %, thereby reducing the installation costs and power loss of converters.

Keywords: Differential power processing, Hybrid energy storage systems, DC microgrids, Power allocation, Modified droop control.

Nomenclature

Abbreviations

BESSs Battery energy storage systems
DPP Differential power processing
EECMs Equivalent electric circuit models
ESSs Energy storage systems
FPP Full power processing
HESSs Hybrid energy storage systems
HIL Hardware-in-loop

KCL Kirchhoff's Current Law
KVL Kirchhoff's Voltage Law
LPFs Low-pass filters
MPPT Maximum power point tracking
RESs Renewable energy sources
SCs Supercapacitors
SEPIC Single ended primary inductor converters
SoC State-of-Charge

Parameters and Variables

C Capacitor for converters
C_1 Capacitor of R_1C_1 network
C_{dc} Capacitor of DC bus
C_{sc} Capacitor of SC
D_b Duty ratio of DPP converter for battery
D_{fe} Duty ratio of front-end converter
D_{sc} Duty ratio of DPP converter for SC
I_b Output current of battery
I_b^{ref} Reference of output current of battery
I_0 Current of equivalent load
$I_{fe,\alpha}$ Output current of the front-end converter
$I_{fe,\beta}$ Input current of the front-end converter
I_{load} Current drawn by load
I_{res} Current generated by RESs
I_{sc} Output current of SC
I_{sc}^{ref} Reference of output current of SC
k Proportional gain for SoC recovery of SC.
k_{i1} Integral gain for voltage loop tracking
k_{i2} Integral gain for current loop tracking
k_i Integral gain for battery/SC current tracking
k_{p1} Proportional gain for voltage loop tracking
k_{p2} Proportional gain for current loop tracking
k_p Proportional gain for battery/SC current tracking
L Inductor for converters
P_b Output power of battery
P_{db} Output power of DPP converter for battery
P_{dsc} Output power of DPP converter for SC
P_{fe} Output power of front-end converter
P_{sc} Output power of SC
R_0 Internal resistance of battery
R_1 Resistor of R_1C_1 network
R_b Equivalent output resistance of battery
R_{sh} Parallel resistance of SC
R_s Serial resistance of SC
V^* Nominal voltage of DC bus
V_b Output voltage of battery
V_{OCV} Open circuit voltage of battery

V_b^*	Nominal voltage of battery
V_{db}	Output voltage of the DPP converters for the battery
V_{db}^{ref}	Reference voltage of DPP converter for battery
V_{dc}	DC bus voltage
V_{dsc}	Output voltage of the DPP converters for SC
V_{dsc}^{ref}	Reference voltage of DPP converter for SC
V_{fe}	Output voltage of the front-end converter
V_{fe}^*	Nominal voltage of the front-end converter
V_{sc0}	Voltage of C_{sc} at initial time
V_{sc}	Output voltage of SC
V_{sc}^*	Nominal voltage of C_{sc}
V_{sc}^{ss}	Steady-state value of V_{sc}
w_c	Cut-off frequency
Z_b	Droop coefficient of battery
Z_{sc}	Droop coefficient of SC

1. Introduction

The global efforts towards reducing carbon and pollutant emissions stemming from fossil fuel combustion has spurred the rapid advancement of renewable energy sources (RESs) power generation technologies [1]. Hybrid energy storage systems (HESSs), which combine battery energy storage systems (BESSs) and supercapacitors (SCs), are commonly implemented in DC microgrids to address power imbalances between RESs and load demands [2]. Due to their distinct output characteristics, BESSs are effective in compensating for low-frequency power fluctuations, while SCs handle high-frequency power discrepancies [3].

In the conventional HESS-DC bus configuration, as shown in Figure 1, both BESS and SC are linked to the DC bus via their respective converters. These converters facilitate power flow adjustment between HESSs and the DC bus, thereby compensating for the power mismatch between the loads and RESs. This power mismatch is represented by the current of the equivalent load, denoted as $I_0 = I_{load} - I_{res}$, where I_{load} and I_{res} are currents drawn by the loads and generated by RESs, respectively. A variety of control strategies for power distribution of HESSs in the conventional HESS-DC bus configuration have been suggested, typically falling into three categories: intelligent control strategies, filter-based strategies, and droop control strategies. Intelligent control strategies include model predictive control [4], fuzzy logic control [5], and artificial neural networks based control [6]. Filter-based strategies, as proposed in [7] and [8], employ low-pass filters (LPFs) to separate power mismatch into the average and transient components, the battery current controller manages the steady component, while the transient part is handled by SC. Both the intelligent and filter-based control strategies rely on a centralized framework, which necessitates a communication network to transmit reference currents to each energy storage unit. Moreover, these control strategies lack flexibility, requiring a redesign of the system when additional storage units are incorporated into HESSs.

In contrast to the intelligent and filter-based methods, the droop control approaches function in a decentralized manner, providing an effective solution for power distribution in HESSs. For example, the integral droop technique has been suggested for energy storage clusters with fast response rates [9], and its integration with traditional voltage-power (V-P) droop facilitates power distribution in a decentralized way. Xu et al developed a decentralized control

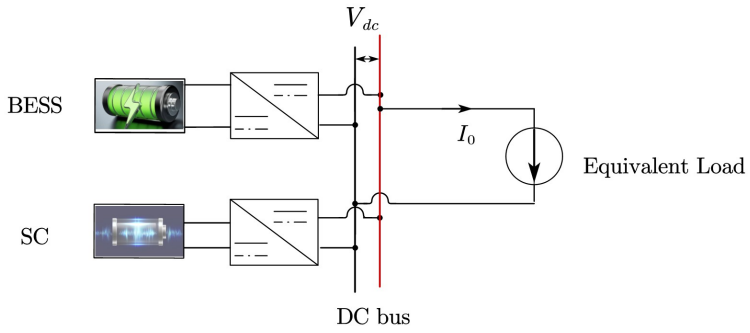

Figure 1: Conventional HESS-DC bus configuration

method using virtual resistance and virtual capacitance droop controllers for the battery and SC, respectively [10, 11, 12]. Moreover, a virtual impedance loop consisting of virtual resistors and capacitors in the middle of SC converter and the DC bus is proposed, which effectively decouples power transfer between SC and other storage units [13]. Gu et al proposed a frequency-coordinating virtual impedance for autonomous power management of DC microgrids [14]. A decentralized improved I-V droop control strategy for battery-SC HESS is proposed, where negligible DC bus voltage deviation can be achieved without extra voltage compensator [15]. Additionally, Su et al proposed a power buffer based framework, enabling the seamless addition of different energy storage units while ensuring efficient and straightforward power distribution [16].

In the conventional HESS-DC bus configuration, the converters for both BESS and SC must handle the entire power demand imposed on each, commonly known as full power processing (FPP) techniques. As the converters are required to manage the full load, this results in significant power losses and high installation costs [17]. In contrast, the concept of DPP techniques, first introduced in [18] for PV systems, processes only the power differences between the PV and the adjacent PVs/DC bus, avoiding the need for handling full power, which helps reduce power losses and system costs.

DPP techniques for PV systems are typically divided into two categories: series DPP and parallel DPP techniques [19, 20]. In series DPP configurations, PV elements are arranged in series, and the DPP converters are responsible for regulating the power differences between neighboring PV units. Lin et al introduced an enhanced DPP design featuring a virtual port connected in series with the submodule string [21]. Jiang et al proposed a DPP converter that incorporates several buck-boost choppers, along with a multidimensional perturb and observe algorithm. This approach enables truly distributed maximum power point tracking (MPPT) by adjusting the voltage of each submodule to its optimal power point, utilizing only a single current sensor [22]. A segmented DPP structure has also been introduced as a modular solution that employs bidirectional DPP flyback converters, aimed at enhancing PV power generation while reducing converter losses [23]. Architectures using series PV strings with DPP converters have been proposed, incorporating distributed MPPT methods to optimize overall system performance [24, 25]. Three typical DPP-based architecture, including series-resonant-voltage-multiplier, flyback-based PV-to isolated point, and flyback-based PV-to-Bus are compared, the key performance indexes includes the processed power, power losses, and overall system efficiency [26].

In parallel DPP techniques, PV elements are connected in parallel, and the voltage differences between the PV elements and the DC bus are regulated. A review of the literature

shows a limited number of studies focusing on these techniques. Lee et al explored the use of parallel DPP converters in a PV-powered wearable system, where inverted buck converters were employed as the DPP converters, these are essentially flipped versions of conventional buck converters, and are also referred to as flipped buck converters [27, 28]. Zhou et al employed flyback converters as DPP converters, with their inputs directly linked to the DC bus [29]. A modular PV-to-PV DPP method was proposed, enabling the addition or removal of PV panels in both series strings and parallel connections [30]. A ultra fast MPPT algorithm is proposed with flyback converters in parallel DPP architectures, and capacitance of DC link is significantly reduced [31].

In summary, the converters for both BESS and SC must handle the entire power demand in conventional HESS-DC bus configurations, resulting in high power-ratings for the converters. This leads to increased installation costs and higher power losses. Drawing inspiration from parallel DPP methods used in PV systems, a new DPP-based framework is introduced for power allocation of HESSs. This framework combines the power allocation strategy of HESSs and DPP techniques, allowing for a reduction in converter power-ratings while simultaneously optimizing power allocation within the system. In our previous work [32], the DPP technique was applied to multiple BESSs, effectively achieving steady-state power-sharing among them. In contrast, this paper focuses on transient power-sharing between SC and BESS, which requires fast battery/SC current tracking to prevent compromised power allocation. To address this challenge, a triple-loop control algorithm is proposed to ensure rapid battery/SC current tracking. Additionally, the influence of the inherent parameters of both SC and BESS on controller performance is analyzed.

The key contributions of this paper are outlined as follows:

1) A DPP-based framework is introduced for power allocation in HESSs, utilizing inverted bidirectional converters as both the front-end converter and subsequent DPP converters. This approach leads to a substantial reduction in the power-ratings of the converters, thereby reducing installation cost and power losses of converters.

2) A triple-loop control algorithm is proposed for the implementation of the modified droop control in the proposed DPP-based framework, where the reference current of battery/SC is tracked by dynamically adjusting the output voltage of DPP converters, ensuring fast battery/SC current tracking and accurate power allocation of HESSs.

3) The stability analysis reveals that the parameters of the equivalent electric circuit models (EECMs) of the battery and SC have no impact on the overall system dynamics. Therefore, it is not necessary to account for the inherent parameters of the battery and SC in the control design. This significantly simplifies the controller design process and facilitates the generalization of the proposed control framework to different types of batteries and SCs.

The structure of this paper is outlined as follows: Section 2 introduces EECMs for both the battery and the SC, as well as the droop control. In Section 3, the proposed DPP-based framework is described in detail, followed by a stability analysis in Section 4. Section 5 presents the results from the hardware-in-loop (HIL) testing of the proposed framework. Finally, Section 6 wraps up the paper with concluding remarks.

2. Preliminaries

2.1. Equivalent Electric Circuit Models of Battery and SC

EECMs of the battery and SC are built to investigate the impact of model parameters on system dynamics and to facilitate the proper design of the controller. Different EECMs for

batteries were proposed in [33]. The first-order EECM is the most prevalent among them, as illustrated in Figure 2 (a). In this model, V_{OCV} and R_0 represent the open circuit voltage and internal resistance of the battery, respectively, while the R_1C_1 network is employed to model the long-term relaxation behavior of the battery. V_b and I_b, respectively, represent battery's output voltage and current. According to the first-order EECM, V_b is expressed by

$$V_b = V_{\mathrm{OCV}} - I_b R_0 - I_b R_1 \left(1 - e^{\frac{-t}{R_1 C_1}}\right) \tag{1}$$

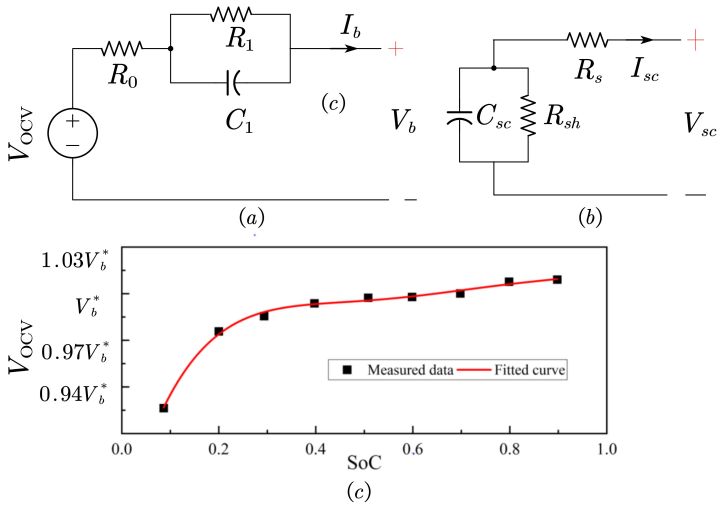

Figure 2: EECMs of battery and SC (a) first-order EECM of battery (b) EECM of SC (c) V_{OCV} versus SoC of $LiFeO_4$ battery

As shown in Eq (1), V_b varies with V_{OCV} and I_b. There is a near-linear correlation between SoC and V_{OCV}, although this relationship may vary slightly depending on the type of battery. The relationship between SoC and V_{OCV} for a typical $LiFeO_4$ battery cell is illustrated in Figure 2 (c) [34]. As the battery SoC increases, V_{OCV} also increases; consequently, V_b is higher at a specific I_b when the battery SoC is high. Additionally, it is easy to deduce that V_b is higher during the charging process compared to the discharging process at a specific SoC. In this study, the nominal of battery output voltage V_b^* equals to $V_{\mathrm{OCV}}(\mathrm{SoC} = 0.5)$ (battery is at idle mode and $\mathrm{SoC} = 0.5$).

The relationship between V_{OCV} and SoC can be modeled by the m-order polynomial function based on the experimental data, it is expressed by

$$V_{\mathrm{OCV}} = \alpha_m \mathrm{SoC}^m + \alpha_{m-1}\mathrm{SoC}^{m-1} + \cdots + \alpha_1 \mathrm{SoC} + \alpha_0 \tag{2}$$

where $a_m, ..., a_0$ is the constant value derived from curve fitting. The battery output characteristics can be obtained by combing Eq (1) and Eq (2).

EECM of SC is illustrated in Figure 2 (b), which consists of an ideal capacitor C_{sc}, a series resistance R_s representing the internal voltage drop, and a parallel resistance R_{sh} for modeling the leakage current [35]. Typically, R_{sh} is quite large while R_s is small. The voltage of the ideal capacitor C_{sc} is updated by

$$V_{sc} = V_{sc0} - \frac{1}{C_{sc}} \int I_{sc} dt \tag{3}$$

where V_{sc} is voltage of C_{sc}, V_{sc0} is voltage of C_{sc} at initial time, and I_{sc} is output current of SC.

2.2. The Droop Control for Power Allocation Between Battery and SC

In the conventional HESS-DC bus configuration illustrated in Figure 1, the droop control is introduced for power allocation by replacing the constant droop coefficients, the equations of battery and SC output current are expressed by [36]

$$I_b = \frac{V^* - V_{dc}}{Z_b s} \tag{4a}$$

$$I_{sc} = \frac{V^* - V_{dc}}{Z_{sc}} \tag{4b}$$

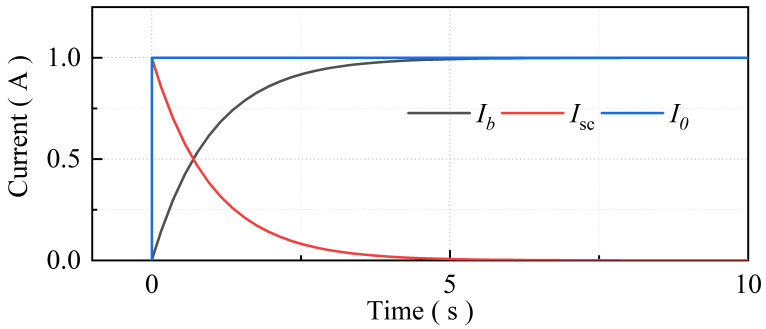

Figure 3: Output current dynamics of the battery and SC

where $Z_b s$ and Z_{sc} are droop coefficients, respectively. V^* and V_{dc} are nominal and measured DC bus voltage, respectively. To facilitate slow response of battery, an integrator is introduced in its control law expressed by Eq (4a), consequently, the battery output current gradually increases from 0. While control law of SC is expressed by Eq (4b), SC responds immediately when power mismatch occurs and causes the DC bus voltage deviation from its reference value. Hence, SC can compensate high-frequency power fluctuation. Following the control law defined in Eq (4), the power response pattern of battery and SC is illustrated in Figure 3 when there is a step change of I_0.

3. The Proposed DPP-based Framework

3.1. The DPP Techniques for HESSs

In the traditional HESS-DC bus setup shown in Figure 1, power exchange between HESSs and the DC microgrids is controlled by the converters, which handle the entire power output from both BESS and SC. This results in high demands on the converters' power-ratings. Since both the installation cost and power loss of the converters are directly related to the power flowing through them, the conventional HESS-DC bus configuration leads to significant power losses and increased installation expenses.

Motivated by the parallel DPP techniques used in PV systems, this study proposes a novel DPP-based framework to resolve the issues discussed earlier. As shown in Figure 4, DPP converters are placed between HESS and the DC bus, allowing for the regulation of power

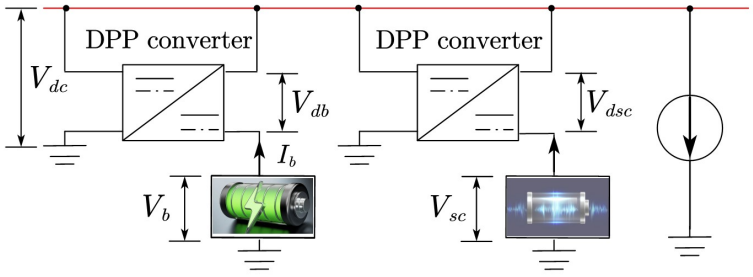

Figure 4: The HESS-DC bus configuration in the proposed DPP-based framework

flow between the two by adjusting the output voltages of the DPP converters for the battery (V_{db}) and for SC (V_{dsc}).

3.2. Inverted Bidirectional Buck Converters for DPP Implementation

Various types of converters are used as DPP converters in PV systems, such as flyback converters and single ended primary inductor converters (SEPIC) [19, 29]. Additionally, inverted buck converters are employed, offering a simpler design with fewer components compared to flyback converters and SEPIC [29, 27].

Considering the aforementioned advantages of inverted buck converters, they are introduced to function as a front-end converter and DPP converters in this study, the detailed system topology is illustrated in Figure 5. The front-end converter is incorporated to reduce the DC bus voltage to an appropriate middle level for powering the DPP converters. Therefore, the one side of front-end converter is connected to the DC bus, while the other side supplies power to **all DPP converters**. C_{dc} represents the capacitance of the DC bus, and V_{fe} denotes the output voltage of front-end converter. The choice of inverted buck converters rather than normal buck converters is due to the fact that normal buck converters would ground the positive output of the battery/SC, leading to uncontrollable power flow from the battery/SC [29].

In contrast to PV panels, which only provide unidirectional power to the DC bus, the bidirectional power flow is necessary in HESSs. The front-end converter utilizes switches S_{f1}/S_{f2}, while the DPP converter for the battery uses switches S_{b1}/S_{b2}, and the DPP converter for the SC is controlled by switches S_{s1}/S_{s2}. The components L and C represent the inductor and capacitor in all converters, respectively. The duty cycles D_{fe}, D_b, and D_{sc} correspond to the front-end converter, the DPP converter for the battery, and the DPP converter for the SC, respectively.

Figure 6 illustrates the power flow between the battery and DC bus when the front-end and DPP converter work at different operating modes. They are detailed as below:

S_{f1} and S_{b1} are on: battery $\leftrightarrow L \leftrightarrow S_{b1} \leftrightarrow L \leftrightarrow S_{f1} \leftrightarrow$ ground.

S_{f1} and S_{b2} are on /S_{f2} and S_{b2} are on: battery $\leftrightarrow L \leftrightarrow S_{b2} \leftrightarrow$ DC bus $\leftrightarrow$ load.

S_{f2} and S_{b1} are on: battery $\leftrightarrow L \leftrightarrow S_{b1} \leftrightarrow L \leftrightarrow S_{f2} \leftrightarrow$ DC bus $\leftrightarrow$ load.

The power flow between SC and DC bus can be analyzed in a similar way, the bidirectional power flow between battery/SC and DC bus are allowed with the proposed framework. Battery/SC works in the discharging mode when there is a power deficit on the DC bus, part of the battery power is injected to the DC bus through DPP converter directly, and the left power is either injected to the DC bus through the front-end converter or flow back to battery/SC from the ground.

Based on the configuration of the proposed DPP-based framework shown in Figure 5 as well as EECMs of battery and SC, I_b and I_{sc} can be derived by

$$I_b = \frac{V_{db} + V_{\text{OCV}} - V_{dc}}{R_b} \tag{5a}$$

$$I_{sc} = \frac{V_{dsc} + V_{sc} - V_{dc}}{R_s} \tag{5b}$$

where $R_b = R_0 + R_1(1 - e^{\frac{-t}{R_1 C_1}})$. It can be observed from Eq (5) that the dynamics of I_b and I_{sc} can be adjusted by changing V_{db} and V_{dsc}, respectively. Furthermore, R_b and R_s seem to have impact on the response of I_b and I_{sc} at the first glance, but the following stability analysis shows the opposite results, thereby simplifying the controller design.

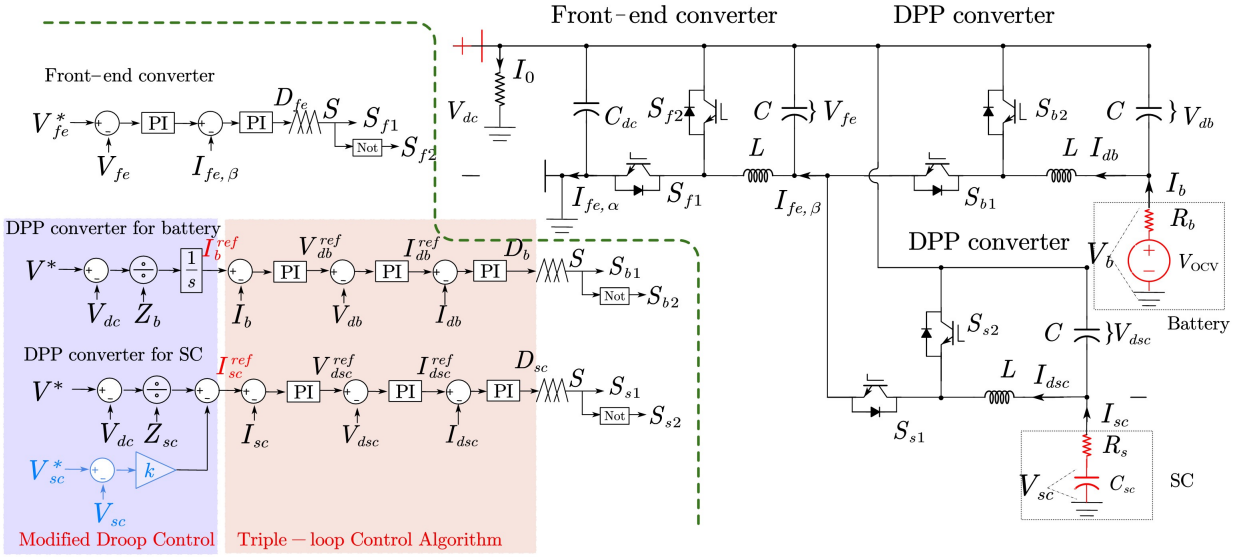

Figure 5: The detailed system topology and control algorithm in the proposed DPP-based framework

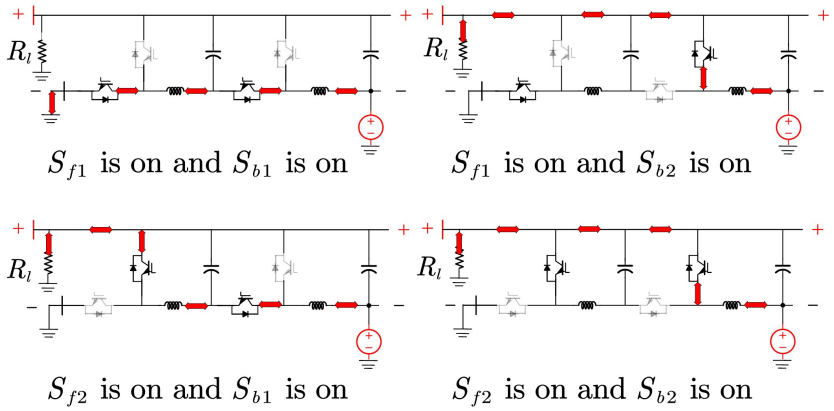

Figure 6: Power flow analysis of inverted bidirectional buck converters

3.3. Power Allocation Strategy for HESSs in the Proposed Framework

As illustrated in Figure 5, the power allocation strategy consists of two parts, the modified droop control and triple-loop control algorithm. The modified droop control generates current reference for battery/SC based on desired power allocation profile and SoC recovery of SC, while the triple-loop control algorithm is proposed for dynamic current reference tracking.

3.3.1. Modified Droop Control

To track the power allocation pattern between battery and SC and achieve SoC recovery of SC simultaneously, the modified droop control is proposed, the reference of output current of battery (I_b^{ref}) and SC (I_{sc}^{ref}) are calculated by

$$I_b^{ref} = \frac{V^* - V_{dc}}{Z_b s} \tag{6a}$$

$$I_{sc}^{ref} = \frac{V^* - V_{dc}}{Z_{sc}} - k\left(V_{sc}^* - V_{sc}\right) \tag{6b}$$

where V_{sc}^* is the nominal voltage of C_{sc}, and k is the proportional gain for SoC recovery of SC. In the proposed SoC recovery controller, only the proportional gain k is introduced while the integral gain is removed, the zero error SoC recovery still be achieved, as presented in Subsection 3.4. C_{sc} is modeled as an ideal capacitor, there is a linear relationship between its output voltage V_{sc} and SoC, hence, the SoC recovery can be achieved by regulating V_{sc} to the pre-set value.

3.3.2. Triple-loop Control Algorithm

Considering the need for battery and SC to quickly compensate for power mismatch, I_b^{ref} and I_{sc}^{ref} should be tracked quickly; otherwise the performance of power allocation is compromised. Therefore, a triple-loop control algorithm is proposed for the fast battery/SC current reference tracking, where I_{sc}^{ref} and I_b^{ref} are tracked by adjusting the output voltage of DPP converters, V_{dsc} and V_{db}, respectively. The reference voltage of DPP converter for battery (V_{db}^{ref}) and for SC (V_{dsc}^{ref}) are expressed by

$$V_{db}^{ref} = \left(I_b^{ref} - I_b\right)\left(k_p + k_i/s\right) \tag{7a}$$

$$V_{dsc}^{ref} = \left(I_{sc}^{ref} - I_{sc}\right)\left(k_p + k_i/s\right) \tag{7b}$$

where k_p and k_i are the proportional gain and integral gain for the reference tracking, respectively. After obtaining V_{db}^{ref} and V_{dsc}^{ref}, the widely used dual voltage-current loop can be implemented for voltage reference tracking in the DPP converters, thereby building the triple-loop control algorithm.

$$I_{db}^{ref} = \left(V_{db}^{ref} - V_{db}\right)\left(k_{p1} + k_{i1}/s\right) \tag{8a}$$

$$D_b = \left(I_{db}^{ref} - I_{db}\right)\left(k_{p2} + k_{i2}/s\right) \tag{8b}$$

$$I_{dsc}^{ref} = \left(V_{dsc}^{ref} - V_{dsc}\right)\left(k_{p1} + k_{i1}/s\right) \tag{9a}$$

$$D_{sc} = \left(I_{dsc}^{ref} - I_{dsc}\right)\left(k_{p2} + k_{i2}/s\right) \tag{9b}$$

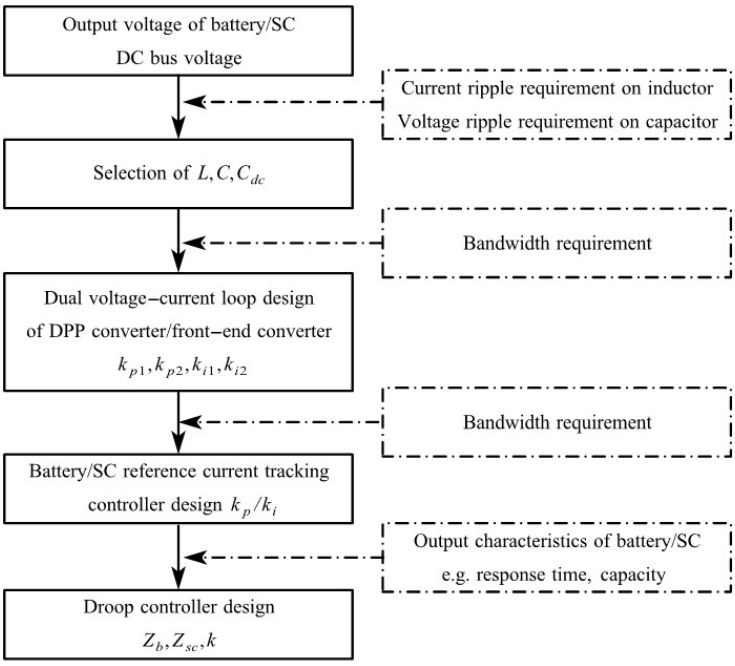

Figure 7: The flowchart of implementation of the proposed control framework

where k_{p1} and k_{i1} the proportional gain and integral gain for voltage loop tracking, while k_{p2} and k_{i2} the proportional gain and integral gain for current loop tracking. The bode plot analysis in next subsection along with the desired power allocation pattern in Section 5, demonstrates the effectiveness of the proposed triple-loop control algorithm for fast current reference tracking.

As aforementioned, the front-end converter is used to step down the DC bus voltage to an intermediate voltage level, otherwise the duty ratio of DPP converter would be too low considering the huge voltage ratio between V_{dc} and V_{db}/V_{dsc}. Hence, the output voltage of the front-end converter V_{fe} is regulated to an intermediate value V_{fe}^*. Similar with the DPP converters, the dual voltage-current loop is implemented for reference voltage tracking in the front-end converter as illustrated in Figure 5.

In summary, the proposed control framework includes modified droop control and the triple-loop control algorithm from outer loop to inner loop, while the triple-loop control algorithm can be further divided into battery/SC reference current tracking loop and conventional double voltage-current loop from outer loop to inner loop. As illustrated in Figure 7, the control framework should be implemented from the inner loop to the outer loop in the following manner: Firstly, the output voltage of the battery/SC and the DC bus voltage should be defined. Secondly, the parameters of the converter circuits (L, C, C_{dc}) should be selected based on the current ripple requirement of the inductor and the voltage ripple requirement of the capacitors. Thirdly, the PI controller parameters for the triple-loop control should be designed by considering the bandwidth standard—where the outer loop bandwidth is typically 1/10 to 1/5 of the inner loop. Finally, the parameters of the modified droop controller should be tuned according to the output characteristics of the battery/SC, such as response time and capacity. This systematic approach facilitates stable controller design.

3.4. The Performance of the Proposed Framework

3.4.1. Power-ratings of Converters

The power-ratings requirement of different converters are discussed in this subsection. Neglecting the response process of the capacitors in the converters, $I_b = I_{db}$ and $I_{sc} = I_{dsc}$ are assumed. Battery and SC are two units working as the sources and the equivalent load draw power from microgrid, thereby, Eq (10a) can be easily derived based on the power balance of the system. Taking the whole system in Figure 5 as a node, I_{sc} and I_b are injected current while $I_{fe,\alpha}$ and I_0 are the current flows out the node, Eq (10b) can be obtained based on Kirchhoff's Current Law (KCL). Similarly, Eq (10c) is obtained based on Kirchhoff's Voltage Law (KVL) by neglecting the voltage drop on R_s.

$$V_b I_b + V_{sc} I_{sc} = V_{dc} I_0 \tag{10a}$$

$$I_{fe,\alpha} = I_b + I_{sc} - I_0 \tag{10b}$$

$$V_b + V_{db} = V_{sc} + V_{dsc} = V_{dc} \tag{10c}$$

The power of DPP converters, battery and SC, and the front-end converter can be calculated by Eq (11) with aforementioned assumption

$$P_{db} = V_{db} I_b / P_{dsc} = V_{dsc} I_{sc} \tag{11a}$$

$$P_b = V_b I_b / P_{sc} = V_{sc} I_{sc} \tag{11b}$$

$$P_{fe} = V_{dc} I_{fe,\alpha} = V_{fe} I_{fe,\beta} \tag{11c}$$

In this study, V_{db} and V_{dsc} are designed much smaller than V_b and V_{sc} (less than 10 %), P_{db} and P_{dsc} will be much smaller than P_b and P_{sc}, thereby highly reducing the power-ratings of converters especially when compared to the conventional HESS-DC bus setup. Moreover, the power passing through the front-end converter, which is equal to the sum of the two DPP converters, also leads to a significantly lower power-rating for the front-end converter. A detailed discussion of the power-ratings for the different converters can be found in Section 5.

As aforementioned, V_{db} and V_{dsc} are designed much smaller than V_b and V_{sc} (less than 10 %), it is easy to derive Eq (12) based on Eq (10)

$$I_0 < I_b + I_{sc} < 1.1 I_0 \tag{12a}$$

$$I_{fe,\alpha} < 0.1 I_0 \tag{12b}$$

$I_{fe,\alpha}$ is a small value compared with I_0, it decreases as V_{db} or V_{dsc} decreasing. This also reveals the reason that power-ratings of DPP and front-end converters are small.

3.4.2. Performance of Triple-loop Control Algorithm

In this part, the dynamic behavior of tracking I_b^{ref} is analyzed as an example to demonstrate the performance of the proposed triple-loop control algorithm. The tracking of I_{sc}^{ref} can be analyzed in a similar way.

Based on the electric circuit of DPP converter for battery illustrated in Figure 5, Eq (13) is derived for different switch states.

$$(V_{dc} - V_{db}) - (V_{dc} - V_{fe}) = L \frac{dI_{db}}{dt} \;\; S_{b1} \text{ is on} \tag{13a}$$

$$-V_{db} = L\frac{dI_{db}}{dt} \; S_{b2} \text{ is on} \tag{13b}$$

Based on the state-space average model of power converters, the following equation is obtained:

$$V_{fe}D_b - V_{db} = L\frac{dI_{db}}{dt} \tag{14a}$$

$$C\frac{dV_{db}}{dt} = I_{db} - I_b \tag{14b}$$

Combing Eq (5a), Eq (8) and Eq (14), the transfer function of I_b in terms of I_b^{ref} is expressed by Eq (15). Where $a(s) = V_{fe}(k_{p2} + k_{i2}/s)$, $b(s) = k_p k_{p1} + k_p k_{i1}/s + k_{p1}k_i/s + k_i k_{i1}/s^2$. Based on Eq (15), the bode plot of I_b with different k_p and k_i is illustrated in Figure 8. It can be observed that the bandwidth of transfer function with $k_p = k_i = 10$ is 72.1 rad/s, This value increases to $1.52e^4$ rad/s with $k_p = k_i = 30$. Large control parameters lead to a high bandwidth of transfer function. Furthermore, $k_p = k_i = 30$ ensures a fast tracking speed for I_b^{ref} and I_{sc}^{ref} without compromise the performance of power allocation controller.

$$I_b = \frac{a(s)\,b(s)}{(1 + a(s)/(Ls))\,(LCs^2R_b + R_b + Ls) + a(s)\,(b(s) + k_{p1}R_b + k_{i1}R_b/s - R_b/(Ls))} I_b^{ref} \tag{15}$$

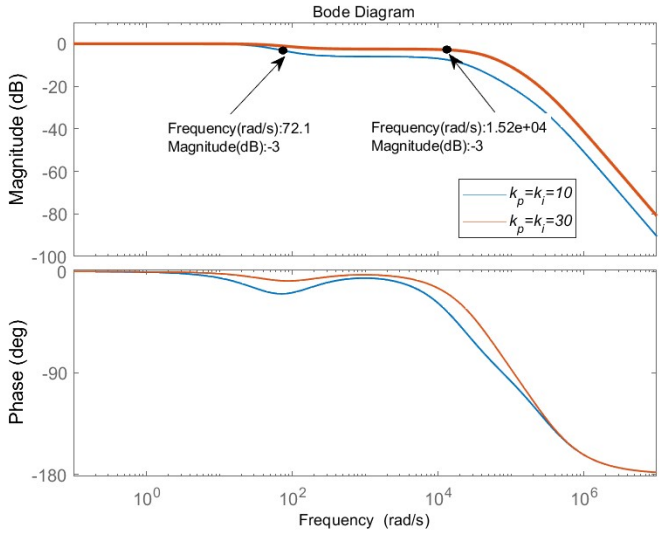

Figure 8: Bode plot of I_b with different k_p and k_i

3.4.3. Power Allocation Between Battery and SC

In the proposed DPP-based framework, I_{sc}^{ref} and I_b^{ref} can be tracked by adjusting the output voltage of DPP converters, assuming the response speed of inner loop is much faster than outer loop, i.e., $I_{sc} = I_{sc}^{ref}$ and $I_b = I_b^{ref}$, it yields

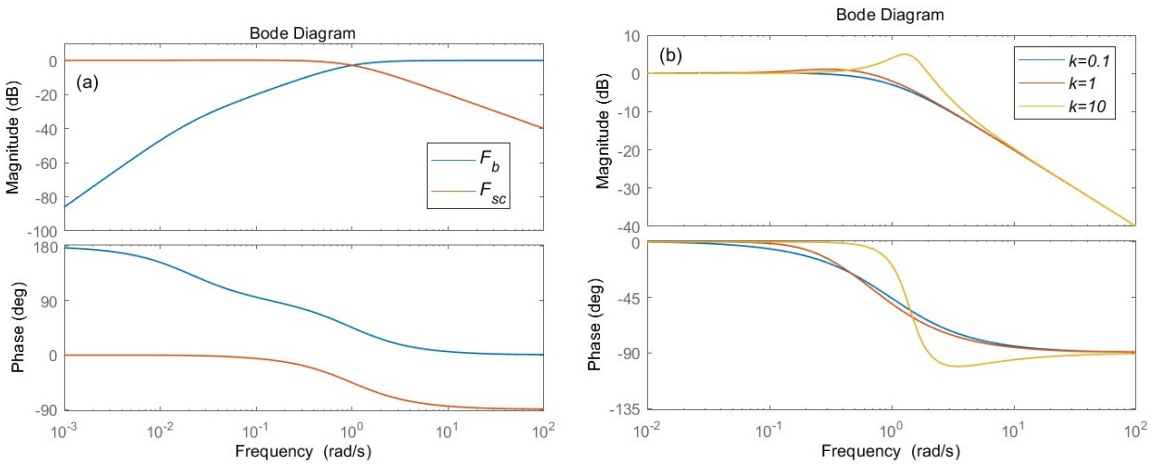

Figure 9: Bode plot (a) Bode plot for F_b and F_{sc} (b) Bode plot for F_b with different k

$$I_{sc} = \frac{V^* - V_{dc}}{Z_{sc}} - k\left(V_{sc}^* - V_{sc}\right) \tag{16a}$$

$$I_b = \frac{V^* - V_{dc}}{Z_b}\frac{1}{s} \tag{16b}$$

$$I_b + I_{sc} = I_0 \tag{16c}$$

It is easily to derive Eq (17) from Eq (16)

$$I_{sc} = F_{sc}\left(s\right) I_0 = \frac{s^2}{s^2 + Z_{sc}/Z_b s + Z_{sc}k/\left(Z_b C_{sc}\right)} I_0 \tag{17a}$$

$$I_b = F_b\left(s\right) I_0 = \frac{Z_{sc}/Z_b s + Z_{sc}k/\left(Z_b C_{sc}\right)}{s^2 + Z_{sc}/Z_b s + Z_{sc}k/\left(Z_b C_{sc}\right)} I_0 \tag{17b}$$

F_{sc} and F_b work as high-pass filter and LPF, respectively. I_0 is splitted into the high-frequency and low-frequency parts, respectively, and the former is compensated by SC while the latter is dealt by the battery. The bode plot of F_{sc} and F_b is illustrated in Figure 9 (a), it can be observed that F_{sc} and F_b intersect at cut-off frequency $w_c = Z_{sc}/Z_b$. Further, k is introduced for SoC recovery of SC, as elaborated in Eq (17), the dynamics of I_{sc} and I_b would be impacted by k/C_{sc} with a specific w_c. The bode plots of F_b with different k are illustrated in Figure 9 (b), a large k leads to a quick SoC recovery speed, however, it also leads to the oscillation of battery and SC output power. Therefore, the selection of k should be a trade-off between SoC recovery speed and oscillation requirements.

3.4.4. SoC Recovery of SC

In the proposed SoC recovery controller, only the proportional gain k is introduced while the integral gain is removed. Zero SoC recovery error can still be achieved with the proposed controller as elaborated below. Combing Eq (3) and Eq (6b), it yields

$$V_{sc} = \frac{\left(V_{dc} - V^*\right)/Z_{sc}}{k + C_{sc}s} + \frac{kV_{sc}^*}{k + C_{sc}s} \tag{18}$$

The control law expressed by Eq (4) shows the combination of battery and SC controller works as a PI controller, and the DC bus voltage will be restored to V^*. Therefore, the first item in the left side of Eq (18) is 0 in the steady-state (when DC bus voltage is restored), and applying the final-value theorem, it yields

$$V_{sc}^{ss} = \lim_{s\to 0} s\frac{kV_{sc}^*/s}{k + C_{sc}s} = V_{sc}^* \tag{19}$$

where V_{sc}^{ss} is the steady-state value of V_{sc}. Therefore, V_{sc} can be regulated to V_{sc}^* just with the proportional gain k.

4. Stability Analysis

The stability analysis is performed to validate the proposed DPP-based framework. In this study, C_{dc} is selected to be significantly larger than the other capacitors and inductors. Assuming that the dynamics of the front-end and DPP converters are sufficiently fast, this ensures that the output power from HESS is immediately delivered to the DC bus. The rate of change of the DC bus voltage is given by

$$\dot{V_{dc}} = \frac{1}{C_{dc}}\left(I_b + I_{sc} - I_0\right) \tag{20}$$

Similarly, we assume $V_{db}^{ref} = V_{db}$, $V_{dsc}^{ref} = V_{dsc}$ based on the fact that the bandwidth of the dual voltage and current control loops is typically much higher than that of the outer loop, allowing for effective reference voltage tracking. Combining Eq. (3) with the DPP control algorithm as defined in Eqs. (5) to (7), along with Eq. (20), results in:

$$\dot{\boldsymbol{\varphi}} = A\boldsymbol{\varphi} \tag{21}$$

where $\boldsymbol{\varphi} = [V_{dc}, V_{db}, V_{dsc}, V_{sc}, \gamma]^{\mathrm{T}}$ and $\dot{\gamma} = V_{dc}$.

$$A = \begin{pmatrix} \frac{-1}{C_{dc}R_b} - \frac{1}{C_{dc}R_s} & \frac{-1}{C_{dc}R_b} & \frac{-1}{C_{dc}R_b} & \frac{-1}{C_{dc}R_b} & 0 \\ a_{21} & a_{22} & a_{23} & a_{24} & a_{25} \\ a_{31} & \frac{R_s\theta_2}{R_s+k_p} & \frac{R_s\theta_1}{R_s+k_p} & a_{34} & 0 \\ \frac{1}{C_{sc}R_s} & 0 & \frac{1}{C_{sc}R_s} & \frac{1}{C_{sc}R_s} & 0 \\ 1 & 0 & 0 & 0 & 0 \end{pmatrix}$$

$a_{21} = \frac{R_b}{R_b+k_p}\left(\frac{k_i}{R_b} - \frac{k_p}{Z_b} - \frac{k_p}{R_b^2C_{dc}} - \frac{k_p}{R_bR_sC_{dc}}\right)$, $a_{22} = \frac{R_b}{R_b+k_p}\left(-\frac{k_i}{R_b} + \frac{k_p}{R_b^2C_{dc}}\right)$,

$a_{23} = a_{24} = \frac{R_b}{R_b+k_p}\frac{k_p}{R_bR_sC_{dc}}$, $a_{25} = -\frac{R_b}{R_b+k_p}\frac{k_i}{Z_b}$,$a_{31} = \frac{R_s}{R_s+k_p}\left(-\frac{k_i}{Z_{sc}} - \theta_1 - \theta_2\right)$

$a_{34} = \frac{R_s}{R_s+k_p}\left(k_ik + \theta_1\right)$, $\theta_1 = \frac{1}{R_s}\left(\frac{k_p}{R_sC_{dc}} - \frac{k_p}{Z_{sc}C_{dc}} - k_i - \frac{k_pk}{C_{dc}} + \frac{k_p}{R_sC_{dc}}\right)$, $\theta_2 = \frac{1}{R_b}\left(\frac{k_p}{R_sC_{dc}} - \frac{k_p}{Z_{sc}C_{dc}}\right)$

Based on Eq (21), the trajectory of eigenvalues as control parameters Z_b and Z_{sc} vary is illustrated in Figure 10 (a). The blue stars indicate the starting positions of the eigenvalues, while the red stars mark their final positions. The arrows show the trajectory of the eigenvalue movement as the parameters change. All eigenvalues are situated in the left half of the complex plane, confirming that the system remains stable. The eigenvalues move right which shows that the increase of Z_b and Z_{sc} slow down system dynamics. The movement of eigenvalues as R_s and R_b increase is illustrated in Figure 10 (b). All eigenvalues are kept unchanged, thus, the changing R_s and R_b do not impact the system response. The different power allocation patterns can be adjusted by changing w_c without considering R_s and R_b, which simplifies the controller design.

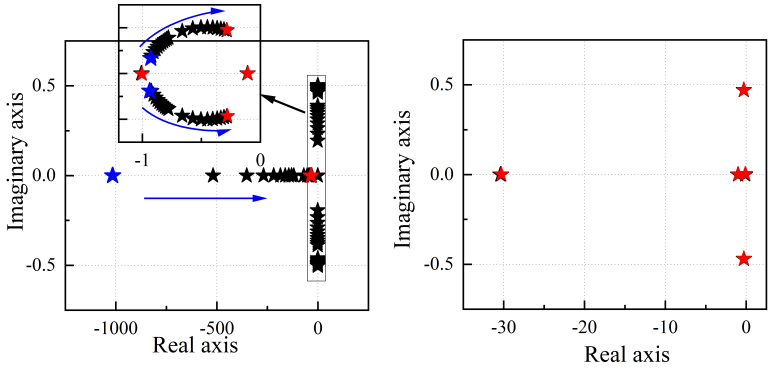

Figure 10: Eigenvalue movement (a) as Z_b and Z_{sc} increases (b) as R_s and R_b increases

5. Test Results and Discussions

The test results are divided into four subsections. The first three subsections are dedicated to evaluating the effectiveness of the proposed framework under hardware-in-the-loop (HIL) real-time testing. This testing is conducted using the Typhoon HIL-604 platform. As illustrated in Figure 11, the converters and HESSs are emulated by the Typhoon HIL-604, while control of the emulated system is implemented on a Texas Instruments TI LaunchPad (LAUNCHXL-F28069M), connected to the Typhoon HIL device via a LaunchPad interface.

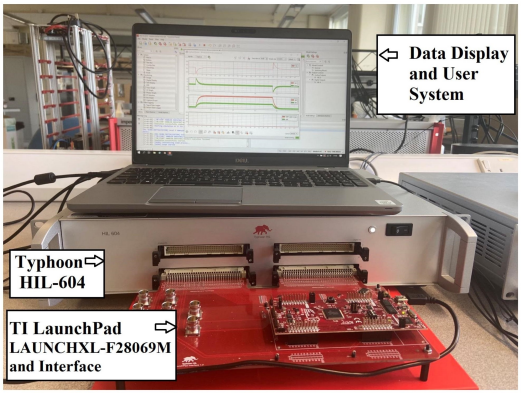

Figure 11: HIL tests

The fourth subsection compares the proposed framework with a conventional configuration. The first part of this subsection is also conducted under HIL real-time conditions. To isolate the impact of system configuration on current ripple—minimizing the influence of noise and controller delays—the results presented in Subsection 5.4.2 are obtained under an ideal environment using Matlab/Simulink. The system and controller parameters used in the tests are summarized in Table 1.

While the forth subsection is used to compared the proposed framework and conventional configuration. The first part of forth subsection is also conducted under HIL real-time environment. To focus on the impact of system configuration on the current ripple rather than noise and controller delay, the test results in subsection 5.4.2 are conducted in ideal environment, i.e., Matlab/Simulink. The sampling intervals in both HIL and Simulink tests are 10 us. The system and controller parameters used in the tests are summarized in Table 1.

Table 1: System and control parameters used in HIL tests

Parameters	Value	Parameters	Value	Parameters	Value
V^*	900V	V_{fe}^*	300V	V_{sc}^*	850V
V_b^*	845V	L	5e-3H	C	1e-3F
k	0.5	Z_{sc}	1	Z_b	1
k_p	10	k_i	10	R_s	0.01 Ω
R_0	0.42 Ω	R_1C_1	8.32 ΩF	C_{dc}	0.05 F

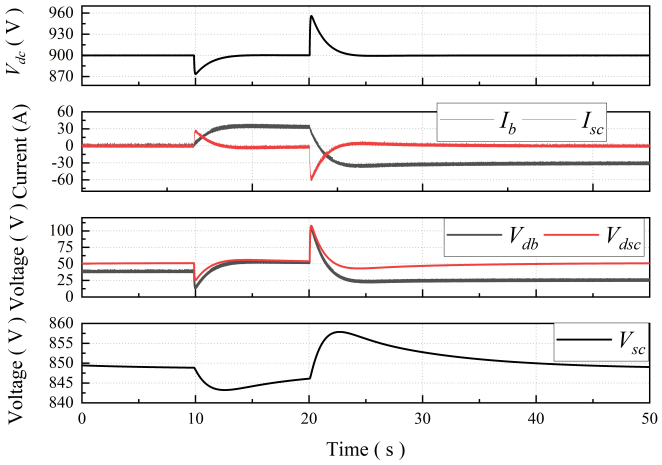

Figure 12: Test results under I_0 disturbances

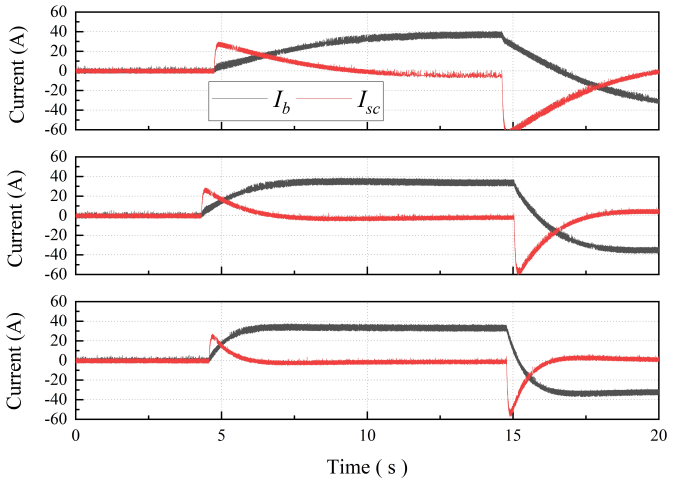

Figure 13: Power allocation between battery and SC with different w_c. From top to bottom $w_c = 0.4/w_c = 1/w_c = 2$

5.1. Overall System Performance

The overall system performance with the proposed DPP-based framework is illustrated in Figure 12, I_0 becomes positive (30A) at 10 s, battery and SC discharge to support the DC microgrid. SC response quickly and compensate the high-frequency power while the response of battery is slow. V_{db} and V_{dsc} are properly regulated at about 50 V to fill the voltage gap

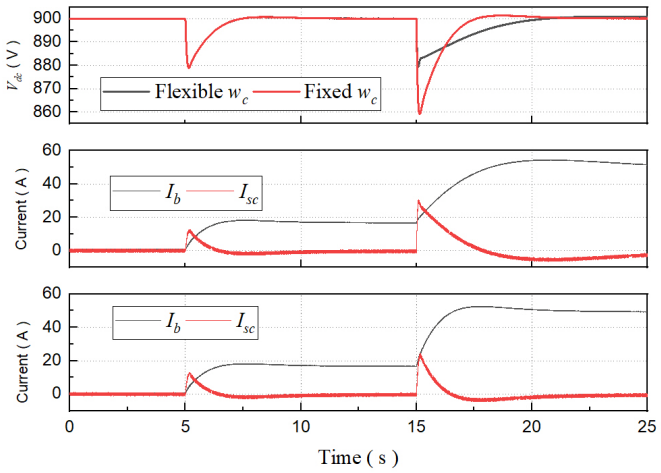

Figure 14: Test results with flexible and fixed w_c. From top to bottom V_{dc} under flexible and fixed w_c/Output current with flexible w_c/Output current with fixed w_c.

between V_{dc} and V_b/V_{sc}, consequently, the desired I_b and I_{sc} are tracked. DC bus voltage is regulated to its nominal value (900 V). At 20 s, I_0 turns negative (-30A), the only difference with the previous status is that battery and SC are charged. Further, V_{sc} is restored to its nominal value with the proposed controller.

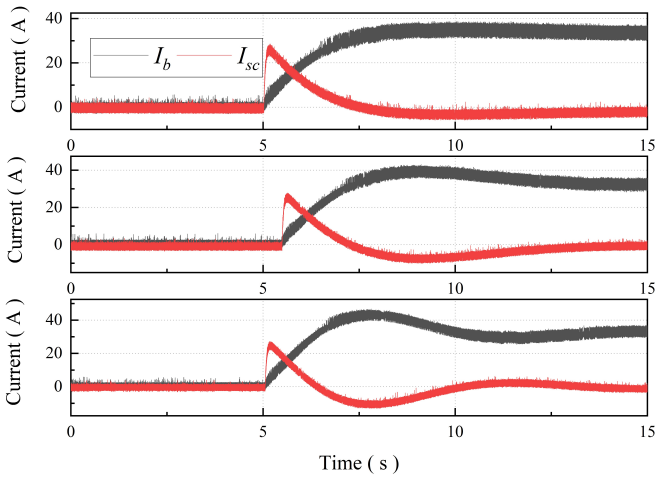

Figure 15: Power allocation between battery and SC with different k. From top to bottom $k = 0.5/k = 2/k = 5$

5.2. Dynamics of Power Allocation with Different w_c

In this test, the power allocation dynamics between the battery and SC with different w_c are validated. Z_b is held constant at 1, while Z_{sc} is varied to explore different power allocation dynamics. All other parameters remain unchanged as specified in Table 1. The power allocation dynamics for $w_c = 0.4$, $w_c = 1$, and $w_c = 2$ are depicted in Figure 13. A higher w_c results in a faster power allocation speed, manifested as a quicker increase in I_b and a faster decrease in I_{sc}. Consequently, the choice of w_c should be tailored to the output characteristics of both battery and SC.

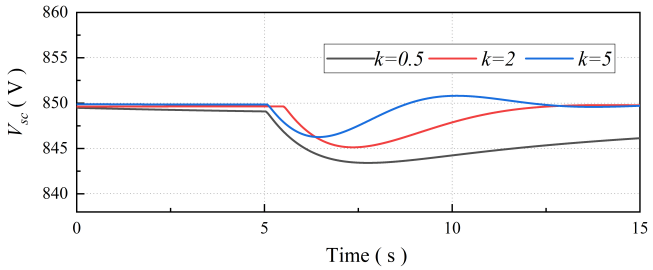

Figure 16: SoC recovery of SC with different k

Moreover, the test results with a flexible w_c that varies with the load condition are illustrated in Figure 14, where Z_b is kept constant at 1 while Z_{sc} changes with I_0. The load current I_0 increases to 15 A and 45 A at 5 s and 15 s, respectively. It can be observed that light load disturbance occurs at 5 s, the fluctuations of the DC bus voltage and the output currents of the battery and SC are nearly identical under both flexible and fixed w_c. However, at 15 s, the DC bus voltage drop and the rising rate of the battery output current are reduced in the flexible w_c case compared to the fixed w_c case. This improvement is attributed to the reduction of w_c with increasing I_0, which enhances the response speed of the SC. Consequently, the DC bus voltage drop and the burden on the battery are alleviated under heavy load conditions.

5.3. Power Allocation Dynamics with Different k

In this test, the power allocation dynamics with different k is researched. Figure 15 illustrate the response of I_b and I_{sc} with different k, and Figure 16 shows the response of V_{sc}. It can be observed that a greater k leads to a faster power allocation speed, but it also causes a large output power oscillations.

5.4. Comparison with the Conventional Configuration

5.4.1. Power-ratings of Converters

Table 2: Power of HESS and different converters

High SoC	BESS discharging	BESS charging
Front-end converter	1691W	717W
DPP converter for battery/SC	1691W	717W
Converter (conventional configuration)	27000W	27000W
Battery/SC	27000W	27000W
Low SoC	BESS discharging	BESS charging
Front-end converter	2390 W	1395 W
DPP converter for battery/SC	2390 W	1395 W
Converter (conventional configuration)	27000W	27000W
Battery/SC	27000W	27000W

As previously mentioned, the proposed DPP-based framework enables lower power-ratings for the converters when compared to the conventional configuration. The power levels of both the front-end and DPP converters are examined under four different battery operating conditions. To determine the power-ratings of the converters in the proposed framework, the

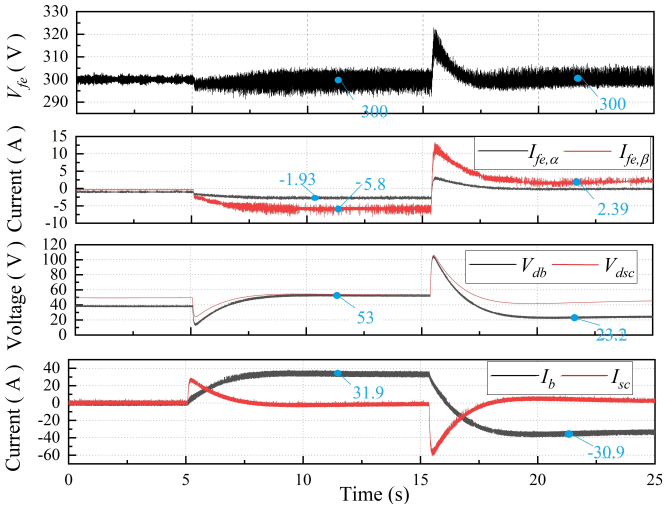

Figure 17: Performance of the converters under high SoC condition

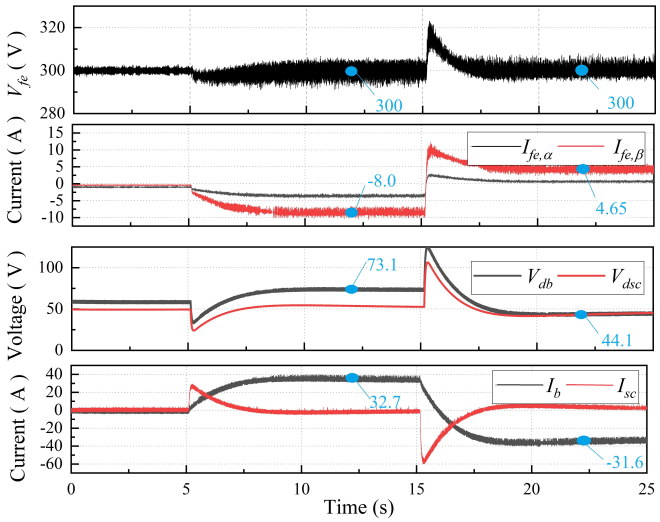

Figure 18: Performance of the converters under low SoC condition

waveforms of V_{db}, V_{dsc}, V_{fe}, $I_{fe,\alpha}$, $I_{fe,\beta}$, I_b, I_{sc} with high battery SoC (SoC=0.8) and low SoC (SoC=0.2) are illustrated in Figure 17 and Figure 18, respectively. In this test, I_0 turns to 30 A at about 5 s and turns to -30 A at about 15 s. As shown in Table 2, the power of front-end converter and DPP converters as well as battery and SC output power are calculated based on Eq (11). The numbers in blue in Figure 17 and Figure 18 are used for calculation. It is worth noting that the output power of SC and its DPP converter is 0 at steady-state because the power allocation is finished. Considering $I_{sc} = I_0$ at the beginning of power allocation and $I_b = I_0$ at the end of power allocation, it is reasonable to assume $P_{db} = P_{dsc}$ and $P_b = P_{sc}$.

The power requirements for the converters under the following four battery operating scenarios are summarized below:

High SoC and charging mode. In this case, the battery reaches its highest output voltage, and the voltage difference between the DC bus and the battery output is minimal. Therefore, the power required by the DPP and front-end converters is at its lowest.

Low SoC and discharging mode. In this scenario, the battery operates at its lowest

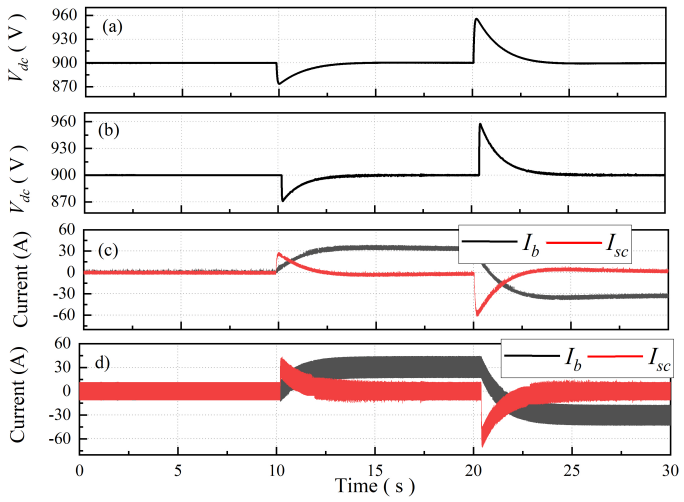

Figure 19: Performance of the proposed framework and the conventional configuration (a)/(c) Test results with the proposed framework (b)/(d) Test results with the conventional configuration

output voltage, resulting in the largest voltage difference between the DC bus and the battery output. This leads to the maximum power flow through the DPP and front-end converters.

High SoC and discharging mode / Low SoC and charging mode. The power demands for the DPP and front-end converters are between the two previous operating conditions.

For comparison, the power of the battery and SC converters in the conventional HESS-DC bus configuration is also presented in Table 2. In the worst-case scenario (low SoC and battery discharged), the power-ratings of the DPP converters for both battery and SC, as well as the front-end converter, are significantly reduced. Specifically, the power-rating is reduced to 2390/(30*900=27000)=8.85% of the power-rating of the battery converter used in the conventional HESS-DC bus configuration. The power of all converters in the proposed DPP-based framework is 2390×3=7170W, while the power for all converters in the conventional configuration is 27000×2=54000W. Thus, the total power-ratings of all converters is reduced to 7170/54000=13.28 % in the worst operating scenario. In the optimal operating scenario (high SoC and battery charged), the power-ratings for the DPP and front-end converters are reduced further to 2.66% of the power-rating of the battery converter in the conventional configuration. The overall power requirement for all converters is reduced to 3.98 % .

In conclusion, with the proposed DPP-based framework, the power-ratings of the converters are reduced to under 15 % in the worst-case operating scenario, and they are even lower in all other operating conditions. Since the power loss and installation cost of converters are directly proportional to their power-ratings, the adoption of the proposed framework results in a significant reduction in both installation costs and power losses.

5.4.2. Performance of DC Bus Voltage and Power-sharing

The performance of DC bus voltage regulation and power allocation between battery and SC with the proposed DPP-based framework and the conventional configuration is illustrated in Figure 19, where the normal buck converters are used in the conventional configuration. It can be observed from Figure 19 that similar response of DC bus voltage can be observed in two configurations, while the proposed DPP-based framework presents smaller current

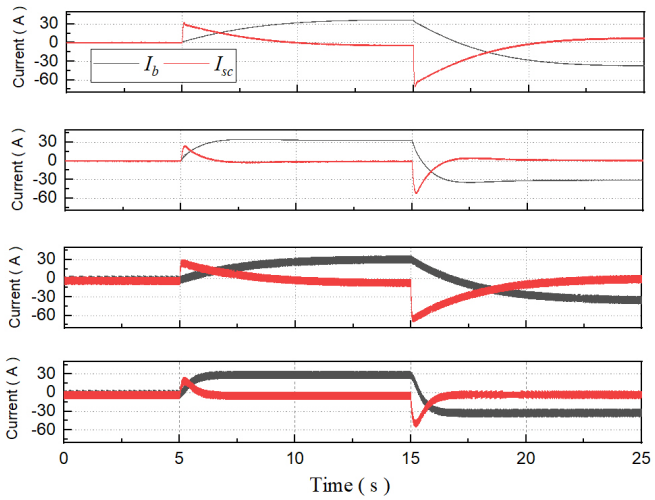

Figure 20: Output current performance of the proposed framework and the conventional configuration. From top to bottom The proposed framework with w_c=0.4/ The proposed framework with w_c=2/ The conventional configuration w_c=0.4/The conventional configuration w_c=2

ripple compared with the conventional configuration. The reasons are follows: the current ripple of battery and SC with the proposed DPP-based framework equal to $V_{db}(1-D_b)/L$ and $V_{dsc}(1-D_{sc})/L$, respectively, the current ripple of battery and SC with the conventional configuration equal $V_{dc}(1-D)/L$. V_{db}/V_{dsc} is much smaller than V_{dc}.

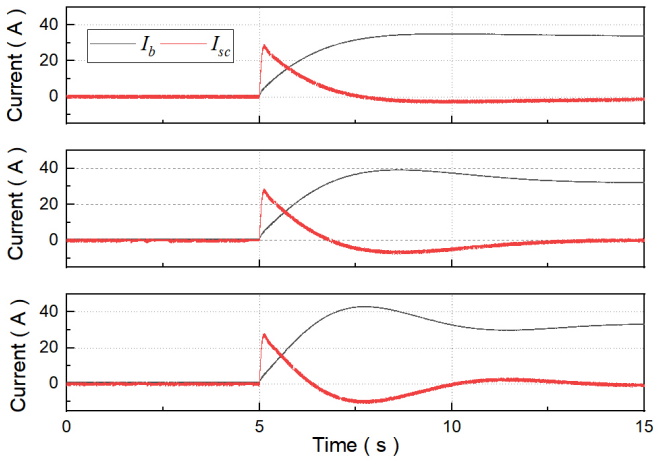

Figure 21: Performance of the proposed framework From top to bottom $k = 0.5/k = 2/k = 5$

The performance of the proposed framework and the conventional configuration under different values of w_c is illustrated in Figure 20. It can be observed that both the proposed framework and the conventional configuration achieve appropriate power sharing between the battery and SC. However, the proposed framework exhibits significantly lower current ripple compared to the conventional configuration. Specifically, the current ripple is approximately 1 A for the proposed framework and 15 A for the conventional configuration. The underlying reasons for this difference have been discussed as aforementioned.

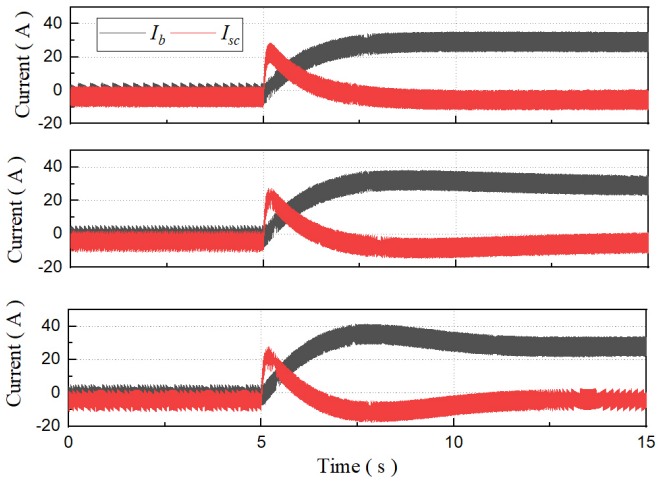

Figure 22: Performance of the conventional configuration From top to bottom $k = 0.5/k = 2/k = 5$

The power-sharing performance of the proposed framework and the conventional configuration under different values of k is illustrated in Figure 21 and Figure 22, respectively. Similar conclusions can be drawn from both figures: the proposed framework and the conventional configuration exhibit similar output current responses. However, the proposed framework demonstrates significantly lower current ripple compared to the conventional configuration, highlighting the superiority of the proposed approach.

6. Conclusions

This paper has presented a DPP-based framework for HESSs, maintaining power allocation performance while significantly lowering the power-ratings of the converters. This is accomplished by incorporating inverted bidirectional buck converters as both the front-end and DPP converters. The modified droop control strategy is applied based on the triple-loop control algorithm to ensure rapid tracking of the reference current for both the battery and SC. The stability analysis of the proposed DPP-based framework reveals that the parameters of the EECMs for the battery and SC do not affect the system's dynamics, thus simplifying the controller design. Real-time HIL tests validate the effectiveness of the proposed framework, demonstrating that power allocation performance is preserved with the power-ratings of the converters reducing to less than 15 %, making it a promising approach for designing HESS-DC microgrids with smaller converters. Additionally, the current ripples of the converters for battery and SC are significantly reduced compared to the conventional configuration.

For system integrators and microgrid designers, the proposed framework offers the following key advantages: Firstly, the reduced voltage stress lowers the voltage rating requirements for components such as capacitors and semiconductors in the converters. This, in turn, decreases the installation cost and physical size of the converters. Secondly, since converter power losses are proportional to the amount of power they process, system efficiency can be improved. The proposed framework processes less than 15% of power in conventional configuration under various operating conditions, thereby enhancing overall system efficiency. Furthermore, the proposed framework can be generalized to other types of DC-based homogeneous and hybrid ESSs. The DPP converters compensate for voltage differences between DC bus and ESSs. For

HESSs, droop coefficients can be designed based on distinct output characteristics, while in homogeneous systems, they can be based on the respective capacities of the storage units.

Despite its advantages, the proposed method has two main limitations. Firstly, an additional converter is required to step down the DC bus voltage to an intermediate level, increasing the system's structural complexity compared to conventional configurations. Secondly, a more sophisticated control strategy—namely, a triple-loop control algorithm—is needed for fast output current tracking of the battery and SC, which adds complexity to the controller design.

In future work, the stability of DC microgrids incorporating the proposed framework will be analyzed under constant power loads disturbances. Constant power loads introduce a negative impedance effect, which can reduce the stability of the system.

References

[1] D. E. Olivares, A. Mehrizi-Sani, A. H. Etemadi, e. a. Cañizares, Trends in microgrid control, IEEE Transactions on Smart Grid 5 (2014) 1905–1919. doi:10.1109/TSG.2013.2295514.

[2] S. Parhizi, H. Lotfi, A. Khodaei, S. Bahramirad, State of the art in research on microgrids: A review, IEEE Access 3 (2015) 890–925.

[3] J. Su, K. Li, L. Zhang, X. Pan, J. Yu, A decentralized power allocation strategy for dynamically forming multiple hybrid energy storage systems aided with power buffer, IEEE Transactions on Sustainable Energy 14 (2023) 1714–1724.

[4] B. Hredzak, V. Agelidis, G. Demetriades, Application of explicit model predictive control to a hybrid battery-ultracapacitor power source, Journal of Power Sources 277 (2015). doi:10.1016/j.jpowsour.2014.11.148.

[5] I. J. Cohen, D. A. Wetz, B. J. McRee, Q. Dong, J. M. Heinzel, Fuzzy logic control of a hybrid energy storage module for use as a high rate prime power supply, IEEE Transactions on Dielectrics and Electrical Insulation 24 (2017) 3887–3893. doi:10.1109/TDEI.2017.006647.

[6] J. Ramoul, E. Chemali, L. Dorn-Gomba, A. Emadi, A neural network energy management controller applied to a hybrid energy storage system using multi-source inverter, in: 2018 IEEE Energy Conversion Congress and Exposition (ECCE), 2018, pp. 2741–2747. doi:10.1109/ECCE.2018.8558326.

[7] E. Schaltz, A. Khaligh, P. O. Rasmussen, Influence of battery/ultracapacitor energy-storage sizing on battery lifetime in a fuel cell hybrid electric vehicle, IEEE Transactions on Vehicular Technology 58 (2009) 3882–3891. doi:10.1109/TVT.2009.2027909.

[8] H. Zhou, T. Bhattacharya, D. Tran, T. S. T. Siew, A. M. Khambadkone, Composite energy storage system involving battery and ultracapacitor with dynamic energy management in microgrid applications, IEEE Transactions on Power Electronics 26 (2011) 923–930. doi:10.1109/TPEL.2010.2095040.

[9] P. Lin, P. Wang, J. Xiao, J. Wang, C. Jin, Y. Tang, An integral droop for transient power allocation and output impedance shaping of hybrid energy storage system in dc microgrid, IEEE Transactions on Power Electronics 33 (2018) 6262–6277. doi:10.1109/TPEL.2017.2741262.

[10] Q. Xu, J. Xiao, P. Wang, X. Pan, C. Wen, A decentralized control strategy for autonomous transient power sharing and state-of-charge recovery in hybrid energy storage systems, IEEE Transactions on Sustainable Energy 8 (2017) 1443–1452. doi:10.1109/TSTE.2017.2688391.

[11] Q. Xu, X. Hu, P. Wang, J. Xiao, P. Tu, C. Wen, M. Y. Lee, A decentralized dynamic power sharing strategy for hybrid energy storage system in autonomous dc microgrid, IEEE Transactions on Industrial Electronics 64 (2017) 5930–5941. doi:10.1109/TIE.2016.2608880.

[12] Q. Xu, J. Xiao, X. Hu, P. Wang, M. Y. Lee, A decentralized power management strategy for hybrid energy storage system with autonomous bus voltage restoration and state-of-charge recovery, IEEE Transactions on Industrial Electronics 64 (2017) 7098–7108. doi:10.1109/TIE.2017.2686303.

[13] Y. Zhang, Y. W. Li, Energy management strategy for supercapacitor in droop-controlled dc microgrid using virtual impedance, IEEE Transactions on Power Electronics 32 (2017) 2704–2716. doi:10.1109/TPEL.2016.2571308.

[14] Y. Gu, W. Li, X. He, Frequency-coordinating virtual impedance for autonomous power management of dc microgrid, IEEE Transactions on Power Electronics 30 (2015) 2328–2337. doi:10.1109/TPEL.2014.2325856.

[15] Z. Wang, P. Wang, W. Jiang, P. Wang, A decentralized automatic load power allocation strategy for hybrid energy storage system, IEEE Transactions on Energy Conversion 36 (2021) 2227–2238. doi:10.1109/TEC.2020.3038476.

[16] J. Su, K. Li, L. Zhang, X. Pan, J. Yu, A decentralized power allocation strategy for dynamically forming multiple hybrid energy storage systems aided with power buffer, IEEE Transactions on Sustainable Energy 14 (2023) 1714–1724.

[17] M. E. Başoğlu, Comprehensive review on distributed maximum power point tracking: Submodule level and module level mppt strategies, Solar Energy 241 (2022) 85–108.

[18] P. S. Shenoy, K. A. Kim, B. B. Johnson, P. T. Krein, Differential power processing for increased energy production and reliability of photovoltaic systems, IEEE Transactions on Power Electronics 28 (2013) 2968–2979. doi:10.1109/TPEL.2012.2211082.

[19] H. Jeong, H. Lee, Y. C. Liu, K. A. Kim, Review of differential power processing converter techniques for photovoltaic applications, IEEE Transactions on Energy Conversion 34 (2019) 351–360. doi:10.1109/TEC.2018.2876176.

[20] T. Zhang, J. Jiang, A review on differential power processing for pv submodule dmppt, 2020 IEEE 3rd Student Conference on Electrical Machines and Systems (SCEMS) (2020) 1012–1017. doi:10.1109/SCEMS48876.2020.9352300.

[21] L. Lin, J. Zhang, S. Shao, Differential power processing architecture with virtual port connected in series and mppt in submodule level, IEEE Access 8 (2020) 137897–137909.

[22] J. Jiang, T. Zhang, D. Chen, Analysis, design, and implementation of a differential power processing dmppt with multiple buck–boost choppers for photovoltaic module, IEEE Transactions on Power Electronics 36 (2021) 10214–10223.

[23] H. Jeong, S. Park, J. H. Jung, T. Kim, A. R. Kim, K. A. Kim, Segmented differential power processing converter unit and control algorithm for photovoltaic systems, IEEE Transactions on Power Electronics 36 (2021) 7797–7809.

[24] J. Biswas, A. M. Kamath, A. K. Gopi, M. Barai, Design, architecture, and real-time distributed coordination dmppt algorithm for pv systems, IEEE Journal of Emerging and Selected Topics in Power Electronics 6 (2018) 1418–1433. doi:10.1109/JESTPE.2017.2756698.

[25] F. Wang, T. Zhu, F. Zhuo, H. Yi, An improved submodule differential power processing-based pv system with flexible multi-mppt control, IEEE Journal of Emerging and Selected Topics in Power Electronics 6 (2018) 94–102. doi:10.1109/JESTPE.2017.2719919.

[26] X. Wang, H. Wen, G. Chu, Y. Zhu, Y. Yang, Y. Wang, L. Jiang, Performance quantization and comparative assessment of voltage equalizers in mismatched photovoltaic differential power processing systems, IEEE Transactions on Power Electronics 39 (2024) 1656–1675. doi:10.1109/TPEL.2023.3328325.

[27] H. Lee, K. A. Kim, Differential power processing converter design for photovoltaic wearable applications, in: 2016 IEEE 8th International Power Electronics and Motion Control Conference (IPEMC-ECCE Asia), 2016, pp. 463–468. doi:10.1109/IPEMC.2016.7512330.

[28] H. Lee, K. A. Kim, Design considerations for parallel differential power processing converters in a photovoltaic-powered wearable application, Energies 11 (2018) 3329.

[29] H. Zhou, J. Zhao, Y. Han, Pv balancers: Concept, architectures, and realization, IEEE Transactions on Power Electronics 30 (2015) 3479–3487. doi:10.1109/TPEL.2014.2343615.

[30] C. Liu, Y. Zheng, B. Lehman, Pv panel to pv panel transfer method for modular differential power processing, IEEE Transactions on Power Electronics 37 (2022) 4764–4778. doi:10.1109/TPEL.2021.3123450.

[31] N. A. Meineri, I. Santana, I. G. Zurbriggen, Ultra-fast mppt for residential pv systems with low dc-link capacitance and differential power processing, IEEE Transactions on Power Electronics 40 (2025) 2736–2745. doi:10.1109/TPEL.2024.3416928.

[32] J. Su, K. Li, Differential power processing based control framework for multiple battery energy storage systems in dc microgrids, IEEE Transactions on Sustainable Energy 15 (2024) 1949–3037.

[33] L. Lu, X. Han, J. Li, J. Hua, M. Ouyang, A review on the key issues for lithium-ion battery management in electric vehicles, Journal of Power Sources 226 (2013) 272–288.

[34] C. Zhang, K. Li, J. Deng, Real-time estimation of battery internal temperature based on a simplified thermoelectric model, Journal of Power Sources 302 (2016) 146–154.

[35] F. Naseri, S. Karimi, E. Farjah, E. Schaltz, Supercapacitor management system: A comprehensive review of modeling, estimation, balancing, and protection techniques, Renewable and Sustainable Energy Reviews 155 (2022) 111913.

[36] Z. Wang, P. Wang, W. Jiang, P. Wang, A decentralized automatic load power allocation strategy for hybrid energy storage system, IEEE Transactions on Energy Conversion 36 (2021) 2227–2238.