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From Concept to Practice: an Automated LLM-aided UVM Machine for RTL Verification

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Abstract— **Verification presents a major bottleneck in Integrated Circuit (IC) development, consuming nearly 70% of the total development effort. While the Universal Verification Methodology (UVM) is widely used in industry to improve verification efficiency through structured and reusable testbenches, constructing these testbenches and generating sufficient stimuli remain challenging. These challenges arise from the considerable manual coding effort required, repetitive manual execution of multiple EDA tools, and the need for in-depth domain expertise to navigate complex designs. Here, we present UVM^2, an automated verification framework that leverages Large Language Models (LLMs) to generate UVM testbenches and iteratively refine them using coverage feedback, significantly reducing manual effort while maintaining rigorous verification standards. To evaluate UVM^2, we introduce a benchmark suite comprising Register Transfer Level (RTL) designs of up to 1.6K lines of code. The results show that UVM^2 reduces testbench setup time by up to 38.82× compared to experienced engineers, and achieve average code and function coverage of 87.44% and 89.58%, outperforming state-of-the-art solutions by 20.96% and 23.51%, respectively.**

I. Introduction

IC verification is the most resource and time-intensive phase in IC frontend design, consuming nearly 70% of the total development effort [1]. As illustrated in Fig. 1, IC verification usually begins with a verification blueprint, followed by functional verification, formal verification, and ultimately sign-off [2]. Among these stages, the functional verification alone accounts for approximately 70% of the total verification effort and encounters two significant challenges that hinder verification efficiency [3]–[7].

The first challenge is the complexity associated with testbench generation. UVM-based testbench is widely used in industrial due to its modular, layered architectures and reusable verification components [8]–[10]. For instance, stimulus generation is modularly encapsulated via sequencers, enabling reuse across designs [11]–[14]. However, this modularity significantly increases the complexity of testbench setup. Engineers must manually instantiate and configure numerous hierarchical components adhering to SystemVerilog class conventions and UVM library specifications [15]–[17], while ensuring accurate connections to the interfaces and protocol behaviours of the Design-Under-Test (DUT). As a result, verification testbench codebase typically grows to 4 or 5 times the size of the original RTL codes, imposing a substantial engineering burden.

The second challenge lies in testcase supplement, which involves generating effective test cases to achieve comprehensive function coverage [18]–[20]. This requires iterative refinement of test cases, including the careful generation of scenarios to capture boundary conditions, rare event sequences, and intricate state transitions. Coverage achieved, defined as the fulfilment of all user-defined function points, becomes increasingly more challenging as design complexity grows [21]–[23]. The manual identification and supplement of these scenarios into testbench are both costly and prone to human error.

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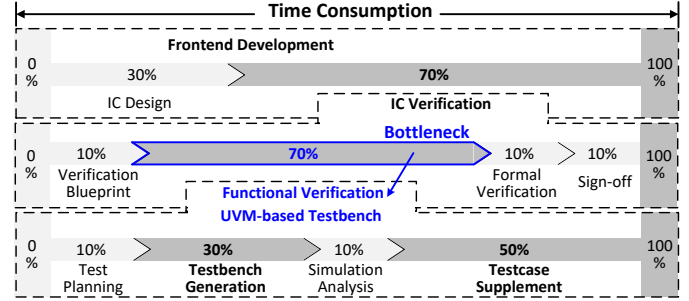
Fig. 1: Breakdown of the IC frontend design and verification workflow, demonstrating the effort required at each stage, where the functional verification dominates the time consumption of the entire workflow.

Recent advances in large language models (LLMs) have opened new opportunities for automated assistance in hardware design and verification [24]–[34]. Prior work has made promising strides: MEIC [35] demonstrated the feasibility of employing LLMs in verification. However, it neither adopts a UVM-based verification flow, thus remaining disconnected from industry-standard methodologies, nor scales beyond small designs (typically fewer than 150 lines of RTL), limiting its applicability to realistic industrial settings. UVLLM [36] improved upon this by integrating LLMs into a UVM-compatible workflow, demonstrating that LLMs can assist in generating UVM components. Nevertheless, the overall verification testbench still demands manual construction. Furthermore, both approaches rely on randomised stimulus generation without targeted coverage refinement or feedback-driven optimisation, leading to limited code and function coverage achievements and reduced verification efficiency.

In this paper, we present an LLM-aided UVM Machine (**UVM^2**), the first systematic framework to realise an automated, LLM-driven function verification. By integrating domain-knowledge-guided prompt engineering with syntactic rule constraints [37]–[40], UVM^2 automatically generates UVM-based verification testbench, and iteratively refines test stimuli based on coverage feedback. This approach not only lowers the barrier to adopting UVM-based verification by significantly reducing the need for human involvement, but also turns a promising concept into a practical and scalable solution, demonstrating improved verification outcomes (e.g., more than 20% improvement over the the state-of-the-art solutions) and increased efficiency (e.g., reducing setup time by more than 15×).

The main contributions of this paper are:
- **An automated framework for UVM testbench generation:** UVM^2 employs LLMs guided by domain-specific strategies to produce industrial-grade, UVM testbench, significantly alleviating manual development overhead.
- **Automated stimuli generation with an iterative refinement:** UVM^2 iteratively improves function coverage by analysing collected coverage data and supplementing test stimuli, thereby
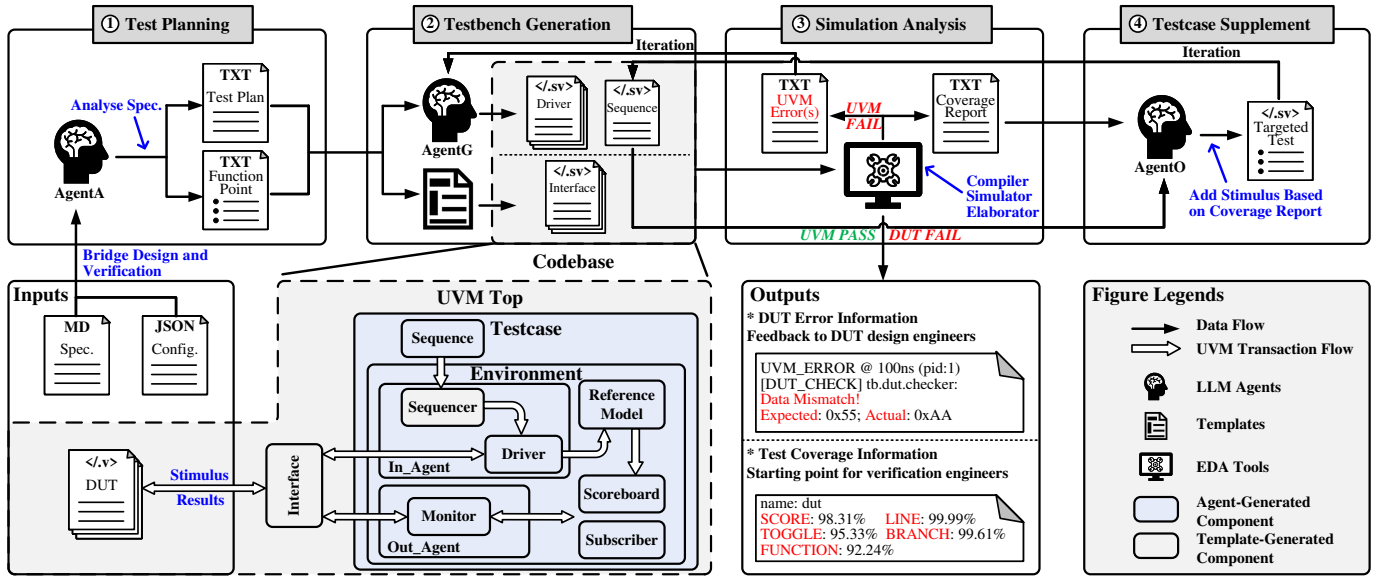
Fig. 2: Overview of the UVM^2 Framework, which integrates UVM with LLM agents to automate the IC verification workflow. The framework includes Analysis Agent (AgentA) for test planning, Generation Agent (AgentG) for automatic testbench creation and error-driven regeneration, and Optimisation Agent (AgentO) for iterative testcase supplement based on coverage analysis.

accelerating coverage achieved.

- **End-to-end integration into practical verification workflows:** UVM^2 supports the complete functional verification, demonstrating its scalability and adaptability across diverse and real RTL designs and protocols.
- **Open-source release of the UVM^2 framework and benchmark:** we release the complete UVM^2 framework and all component within it to support wider adoption. In addition, we publish our evaluation benchmark comprising 10 real RTL designs (ranging from 400 to 1,600 lines of code) for cross-comparison and future research at https://anonymous.4open.science/r/UVM_Machine-7806/.

The rest of this paper is organised as follows. Section II introduces the overall architecture of UVM^2. Section III then details the key techniques in each workflow and their rationales. Section IV assesses our work based on the five proposed research questions. Section V concludes the paper and outlines future research directions.

II. UVM^2: AN OVERVIEW

Aiming to accelerate the verification execution loop, UVM^2 utilises task-specific LLM agents with templates within a standardised UVM tool-chain as shown in Fig. 2. It comprises three specialised agents, one each for analysis, generation and optimisation, and a library of reusable templates as predefined scripts that ensure generation accuracy and reduce LLM usage. UVM^2 produces the verification results as an error information report and a coverage report and assumes following three inputs:

- **Design specifications:** which define the intended functionality and behaviour of the DUT, written in Markdown format.
- **Configuration files:** in which the user specifies the target DUT and the reset state using a JSON file.
- **DUT:** the design entity implemented in RTL code.

These inputs are already expected in existing industrial verification and align with the standard workflow followed by verification engineers, enabling UVM^2 to integrate seamlessly without the need for additional formats or tool dependencies. To maximise accuracy while keeping token usage predictable, each LLM agent is fine-tuned and guided by domain-specific prompts. The overall flow is developed through the following iterative processes:

- **Test Planning.** The Analysis Agent (AgentA) examines the input design specification to identify function points and constructs a coverage-driven testcase plan.
- **Testbench Generation.** Leveraging the identified test plan, the Generation Agent (AgentG) and the pre-validated templates jointly produce a UVM-based verification testbench.
- **Simulation Analysis.** Any errors in the generated UVM testbench are captured during simulation and used to refine the verification testbench, while coverage data are also collected for analysis and supplement.
- **Testcase Supplement.** If coverage remains insufficient, the Optimization Agents (AgentO) create additional targeted sequences to improve stimulus diversity, iteratively refining the testbench until coverage goals or user-defined iterations are reached.

Modularity and flexibility. To allow UVM^2 to evolve with future verification techniques, all artefacts are exchanged via well-defined formats, enabling designers to swap in a domain-specific LLM, replace an EDA tool, or insert additional processes without impacting the validity of the workflow.

III. THE FRAMEWORK PIPELINE

We first present test planning from input specifications (Section III-A) and UVM testbench generation (Section III-B), both serving as the foundation of the framework. We then describe simulation analysis with error handling (Section III-C) and coverage-driven supplementation (Section III-D) to refine the UVM testbench and improve verification quality. Finally, we introduce the benchmarking setup used to assess framework performance (Section III-E).

A. Test planning

In IC design, the design process focuses on implementing functional behaviour, while functional verification ensures all possible scenarios, including edge cases, are handled correctly. Effective verification relies on interpreting the design specification and identifying function points for testing, a task requiring domain expertise. In UVM^2, we automate this process with LLM-based agents, AgentA. However, general-purpose LLMs often struggle with complex specifications due to their lack of structured memory and tendency to hallucinate [41]–[43], leading to missed edge cases. To address this,
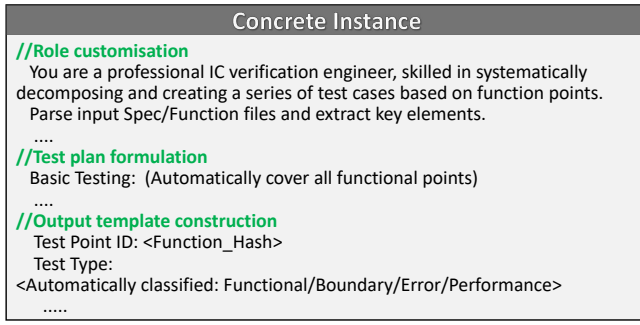
Concrete Instance

```
//Role customisation
   You are a professional IC verification engineer, skilled in systematically
   decomposing and creating a series of test cases based on function points.
   Parse input Spec/Function files and extract key elements.
   ....
//Test plan formulation
   Basic Testing: (Automatically cover all functional points)
   ....
//Output template construction
   Test Point ID: <Function_Hash>
   Test Type:
<Automatically classified: Functional/Boundary/Error/Performance>
   .....
```

Fig. 3: Prompt Instructions for AgentA.

UVM^2 breaks down the analysis into a structured reasoning pipeline that mimics expert verification engineers.

As shown in Fig. 3, our approach follows a three-step analysis flow, designed to isolate the high-level cognitive tasks involved in human-driven verification planning:

1) **Role customisation:** AgentA is first guided through prompts to act as an IC verification engineer, enabling it to identify the functional expectations stated in the specification, including signal dataflow, control dependencies, input/output interaction patterns, and state transitions. From these elements, the agent extracts specific functional points, leading to a deeper understanding of the design's intended behavior.

2) **Test plan formulation:** based on the function points, AgentA is required to define testing strategies for each functional point, including stimulus conditions, observability points, and coverage goals. For example, testing an arithmetic unit involves exercising the full range of operands and all signed/unsigned combinations under both overflow and underflow scenarios.

3) **Output template construction:** to ensure consistency, all related files, including the test plan and functional points (stored in .txt format), follow a predefined template. This template captures each functional point along with its associated test strategy and a draft test case, thereby enabling integration with UVM components and supporting manual inspection and refinement.

This three-step process not only ensures that critical functional points are consistently extracted from the specification, but also improves LLM reliability by enforcing deterministic reasoning paths. The generated test plan serves as the foundation for subsequent verification stages, ensuring alignment between spec-driven objectives and testbench implementation.

B. Verification Testbench Generation

A robust verification testbench must not only support a broad range of stimuli and monitoring strategies but also reflect the structure and interaction logic of the underlying design. In UVM-based flows, the generation of testbenches is extremely time-consuming, largely due to component dependencies. UVM components are tightly coupled structurally and behaviourally. For instance, the Driver and Monitor are inseparable from the Interface: the Driver needs signal-level connectivity to drive transactions, and the Monitor must observe the same signals to collect functional responses. Likewise, an Agent encapsulates and coordinates multiple sub-components (Sequencer, Driver, Monitor), and cannot be constructed without knowing their details. Naively generating each module in isolation risks producing structurally invalid or semantically inconsistent testbenches.
Dependency-Driven UVM Testbench Flow. To address this, UVM^2 employs a dependency-driven testbench generation flow as shown in Fig. 4 that sequences component creation based on interdependencies. The process begins with shared infrastructure (e.g., Interface), proceeds to leaf-level components (Driver, Monitor), then composites
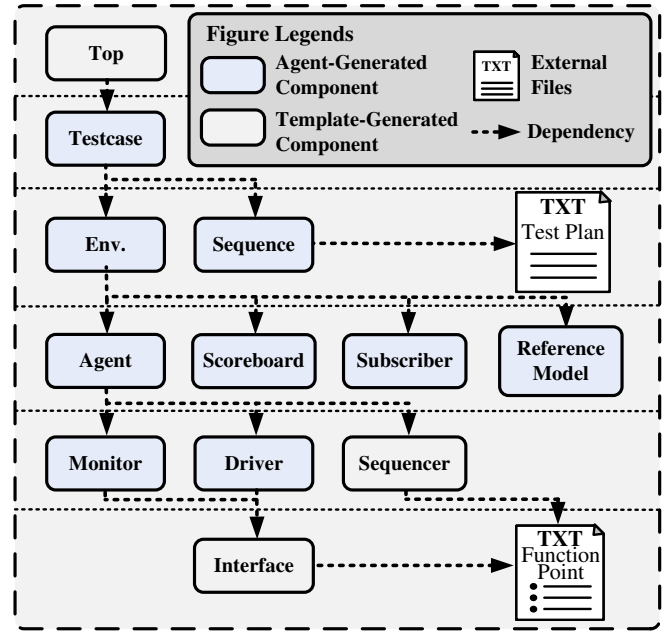

Fig. 4: Dependency-Driven UVM Testbench Generation Workflow with Hierarchical Organization and External Dependencies.
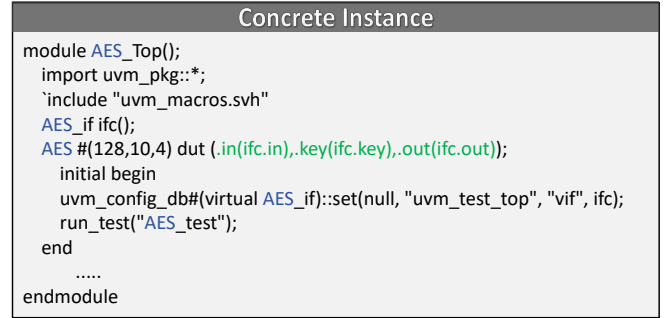
Concrete Instance

```
module AES_Top();
   import uvm_pkg::*;
   `include "uvm_macros.svh"
   AES_if ifc();
   AES #(128,10,4) dut (.in(ifc.in),.key(ifc.key),.out(ifc.out));
      initial begin
      uvm_config_db#(virtual AES_if)::set(null, "uvm_test_top", "vif", ifc);
      run_test("AES_test");
   end
      .....
endmodule
```

Fig. 5: The "Top" module Template in the Testbench. This template facilitates the integration of the testbench with the DUT. The DUT instance name (blue text) and DUT ports (green text) are customizable parameters that allow the template to be configured for various verification scenarios.

(Agents), and concludes with environment-level modules (Scoreboard, Top, Testcase). This ensures each component is generated with complete contextual awareness of its dependencies.

Once the flow is defined, component generation strategies must be selected. Analysis reveals that certain UVM modules exhibit deterministic and repetitive patterns, with variations primarily in signal names and data widths. These can be efficiently synthesised using template-based generation. In contrast, modules involving behavioural logic, such as transaction sequencing or protocol-specific checks, require semantic understanding and are better suited for LLM-based generation. Accordingly, UVM^2 employs a hybrid synthesis strategy (Fig. 4), combining templates for structurally regular components with LLMs for functionally complex ones to optimise efficiency, correctness, and robustness.
Template-Based Generation. Templates are employed for modules that show high regularity across designs. This choice is motivated by three main factors: stability, speed, and reduced hallucination risk. Interface modules follow near-identical formats, varying primarily in the number and naming of input/output ports. Top modules serve as wrappers that instantiate all lower-level components and connect them via DUT ports; their structure is fixed and easily scriptable. Sequencer modules exhibit a rigid control pattern that dispatches sequences to the Driver and rarely require complex logic. Fig. 5 is an example

```
                    Concrete Instance
//Role customisation
   You are an IC verification engineer and you need to use UVM
to build a tesebench.
--UVM {component name} Generation Specification for {module name} --

//Dependency definition
   The content of {new component name} shall be generated based on:
{existing component_names}

//Function expectation
   1.This file is part of the UVM tesebench components, used to {basic
requirements}
   2. At the beginning of the code, add {code requirements}
   3. Pay attention to the input signals must be declare as {functional
requirements}

//Mistake mitigation
   The following mistakes must be prevented: {frequent errors}
```

Fig. 6: Prompt Instructions for AgentG.

generated by the top module using a template. After extracting the module name and port signal from the spec, the template will automatically fill in and generate the complete component.

LLM-Based Generation. In contrast, components with complex behaviour, such as Driver, Monitor, and Scoreboard, require precise functional encoding tailored to specific testcase semantics and verification goals identified earlier. These modules necessitate adaptable code generation that aligns with both design behaviour and test intent. To support this, UVM^2 applies a structured prompting framework for each LLM generation task, as shown in Fig. 6. Each prompt is systematically constructed in four stages to guide the LLM in producing accurate, context-aware SystemVerilog code.

1) **Role customisation:** we guide AgentG to act as an IC verification expert through prompt engineering, enabling it to more accurately understand the design functionality, verification objectives, and the required UVM components. This prompt-driven fine-tuning effectively constrains the relevance and scope of the generated content.

2) **Dependency definition:** dependency information is provided to ensure consistency with related components. For example, a Monitor must reference signal definitions from the Interface and transaction structures from the Sequence Item.

3) **Function expectation:** the prompt outlines the component's functional responsibilities, such as capturing rising-edge events, introducing random timing variations, or detecting protocol violations. It also includes guidance on recommended coding patterns, such as TLM port usage.

4) **Mistake mitigation:** typical mistakes are outlined in the prompt to reduce the impact of hallucinations caused by AgentG, such as missing reset logic, inconsistent transaction identifiers, or incorrect signal directions.

Together, these four stages emulate the thought process of skilled verification engineers, ensuring the generated code is functionally valid and integrable into the overall testbench architecture.

By integrating dependency-driven planning, template-based generation for structural components, and guided LLM synthesis for behavioural modules, UVM^2 delivers a scalable and automation-friendly workflow for UVM testbench construction. This division of labour not only accelerates testbench generation but also improves modular correctness and robustness in industrial-scale projects.

C. Simulation Analysis

Once the UVM testbench is assembled, the DUT is simulated using Synopsys VCS to verify functionality and assess coverage. VCS compiles the DUT and testbench, executes generated testcases, and collects reports on function coverage, code coverage, and runtime

---

Algorithm 1: Repair Mechanism.

Input: Verification log V_{log}
Output: repaired Uvm_Component UC_{True}

1 **Function** Fixed_Err(V_{log}) :
2 $\quad$ /∗ Err : $Error\ message\ of\ component$ ∗/
3 $\quad$ /∗ $GeneAgentMap =$
$\qquad$ {
$\qquad$ "$driver''$: "G_driver_agent'',
$\qquad$ "$monitor''$: "$G\_monitor\_agent''$,
$\qquad$ ...
$\qquad$ } ∗/
4 $\quad$ **for** $phase \in phases$ **do**
5 $\qquad$ **if** $ErrInPhase(V_{log},\ phase)$ **then**
6 $\qquad\quad$ $PhaseErr =$ GetErr(V_{log}, $phase$);
7 $\qquad\quad$ **for** $UC,Err \in PhaseErr_i$ **do**
8 $\qquad\qquad$ $AgentID =$ GeneAgentMap[UC];
9 $\qquad\qquad$ $UC_{True} =$ CallAgent($AgentID$, Err);
10 $\qquad\quad$ **end**
11 $\qquad$ **end**
12 $\quad$ **end**
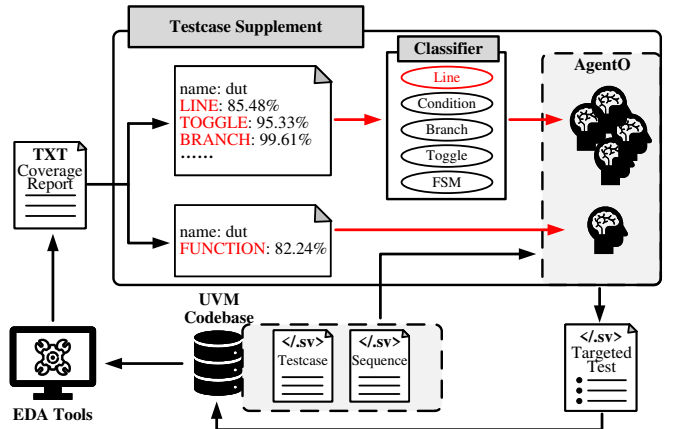13 $\quad$ **return** UC_{True}
14 **End Function**

Fig. 7: Testcase Supplement Workflow with Coverage Analysis.

logs, which are essential for evaluating testbench quality and identifying verification gaps. If design bugs are found, UVM^2 provides detailed diagnostics to assist in debugging.

Repair Mechanism. However, due to the generative nature of our framework, initial outputs from LLMs or templates may contain errors, such as syntax issues, interface mismatches, or improper sequencing, particularly when LLMs receive ambiguous context or insufficient dependency information. Inspired by prior work such as MEIC, which demonstrated the value of iterative LLM refinement through feedback, we introduce a repair mechanism into UVM^2. As outlined in Algorithm 1, if simulation fails, the framework attempts to repair faulty components using LLMs by taking UVM error logs as structured prompts. These are then fed back into the AgentG to drive a second (or third) round of regeneration, focusing on correcting specific structural or behavioural issues. This iteration cycle is repeated iteratively until one of two termination conditions is met: (i) the simulation completes successfully, or (ii) a predefined maximum iteration is exhausted.

D. Testcase Supplement

Ensuring the correctness of a testbench is only one part of the verification process—it does not by itself ensure completeness. In hardware verification, both code and functional coverage are essential indicators, and low or plateaued coverage often suggests that the applied stimuli are not effectively exercising key parts of the DUT. To

//Role customisation
You are an IC verification engineer and you need to use UVM to build a tesebench.
--{modulename}_add_{type_name}_seq Generation Specification --

//Coverage analysis
The new {type_name}_seq shall be generated based on: {existing files}
Consider the following characteristics of this type: {analysis_guidance}

//Stimulus supplement
To generate effective content, ensure the stimulus meets these requirements:
{stimulus_requirements}

//Mistake mitigation
Within randomize() with {} blocks:
* Prohibited: {common mistakes}

Fig. 8: Prompt Instructions for AgentO.

tackle this issue, we introduce a testcase optimisation mechanism that enhances stimulus generation through sequence refinement, focusing on the protocol-level behaviours defined within UVM.

As shown in Fig. 7, testcase supplement phase in UVM^2 analyzes coverage gaps, categorizing them by logic region, transaction stage, or stimulus dependency. Deficient types are passed to AgentO, which revises sequences to target these gaps, generating new testcases until satisfactory coverage is achieved. Precise prompting is crucial, as LLMs without guidance may repeat patterns or miss gaps, making goal-oriented context essential for effective coverage improvement.

To resolve this, we design a prompting instructions for each coverage type. As shown in Fig. 8, it includes four stages that collaboratively shape the LLM's response:

1) **Role customisation:** We assign AgentO the role of an IC verification expert, equipped with sufficient knowledge to generate and optimize the UVM testbench.
2) **Coverage analysis:** We also provide the DUT section, relevant protocols, and reference the specific coverage metrics or types that remain unsatisfied. For the test points that do not satisfy the coverage criteria, we offer explanations to facilitate the process.
3) **Stimulus supplement:** This part includes specific constraints, such as generating sequences with varying payload sizes or triggering edge-case interrupts. These information are used to assist the LLM in supplementing missing stimuli.
4) **Mistake mitigation:** To reduce LLM hallucination during stimulus supplementation, we explicitly forbid certain potentially problematic stimulus sequences in the prompt, including those with syntactic errors or functionally invalid behaviors.

Optimisation mechanism. The refinement loop is designed to be fault-tolerant. If the updated testbench fails simulation, UVM^2 reverts to the last valid version. The loop continues until either the target coverage is achieved or the number of optimization iterations exceeds a user-defined maximum. This closed-loop, coverage-driven refinement strategy mirrors expert workflows while dramatically reducing manual effort, resulting in faster, more reliable verification cycles.

E. Benchmark

While simpler benchmarks such as RTLLM [44] and Verilog-Eval [38], which target designs with fewer than 200 lines of code, are useful for testing basic LLM capabilities in RTL design and verification, they do not accurately reflect the complexities of industrial scenarios. As such, they are not suitable for assessing the full scope and scalability of UVM^2 in real-world applications.

To evaluate the effectiveness of UVM^2, we curated a diverse set of hardware design modules that collectively represent a wide spectrum of real-world verification challenges, as illustrated in Table I. These benchmarks span cryptographic cores (AES, SHA256, SM4), arithmetic units (ALU), memory controllers (DDR3, SDRAM), data

compression (Huffman Encoder - HUF), and peripheral communication interfaces (SPI, UART). Each module presents unique structural and behavioral characteristics, ranging from highly sequential logic (e.g., SHA256, HUF) to pipelined arithmetic computation (e.g., ALU) and complex control flow (e.g., DDR3, SDRAM).

We deliberately selected modules with varying design sizes and complexities, as reflected by their line counts, to assess the scalability and adaptability of our approach. For instance, the AES and HUF modules involve intricate data-path logic and state machines, posing significant coverage challenges. Memory controllers like DDR3 and SDRAM demand rigorous protocol compliance, while modules such as UART and SPI, though smaller, require nuanced handling of asynchronous communication and timing constraints.

IV. EVALUATION

This section presents our experimental setup, evaluation metrics, research questions, and results to answer the questions.

Experimental setup. In our experiment, we employed LLM agents via the Deepseek API, with Deepseek-v3 as the default model. We set the temperature of the agents, which controls the output randomness of the LLM, to 0.3. Then we used our benchmark for assessment and adopted VCS as the simulation tool for our testbench. Additional, we set the iteration times of the iteration mechanism in both Testcase Analysis and Testcase Supplement to 2, since little improvement can be observed based on pre-experiment results. Following the pass@5 evaluation standard commonly used in the LLM field, each component was generated five times per module to minimise experimental randomness.

A. Evaluation Metrics

To evaluate the performance of our work in correct and complete UVM-based testbench, we propose the following metrics:

Success Rate of Generation (SR_G): This metric evaluates the correctness of the generated UVM testbenches by comparing them against a reference testbench manually constructed by experienced engineers. A generated testbench is considered correct if it passes the full VCS simulation flow and produces results that match the expected outputs defined by the reference testbench. Otherwise, it is categorized as a generation failure. This metric reflects the functional validity of the generation framework.

$$SR_G = \frac{N_{\text{correct}}}{N_{\text{total}}} \times 100\% \qquad (1)$$

Coverage: This metric quantifies the test completeness of a generated testbench after it has successfully passed the simulation phase. It is composed of two standard components:

- Code Coverage (C_{code}): Automatically provided by simulation tools such as VCS, this measures the percentage of RTL code exercised by the testbench (e.g., line, branch, toggle coverage).
- Functional Coverage (C_{func}) : This represents how thoroughly the testbench exercises the RTL design with respect to the functional scenarios outlined in the design specification.

Completion Time: This denotes the time to complete the entire functional verification process depicted in Fig. 1. In our work, it corresponds to the time to execute the entire functional verification process under the premise that UVM^2 generates a correct Testbench.

B. Research Questions

We conducted experiments to evaluate UVM^2 with respect to five key research questions (RQs):

RQ1: How effective is UVM^2 in generating syntactically and semantically correct UVM testbenches? This research question evaluates the capability of UVM^2 to produce valid UVM testbenches that conform to standard structure and compile without errors.

TABLE I: Benchmark designs used for evaluation, including a variety of commonly implemented hardware modules such as cryptographic cores (AES, SHA256, SM4), arithmetic units (ALU), memory and communication controllers (DFI, SDRAM, SPI, UART), and a Huffman encoder.

| Design	Description	Module Counts	Line Counts
AES	Encrypts a 128-bit plaintext input using a configurable key (128, 192, or 256 bits) and outputs 128-bit ciphertext.	8	684
ALU	A 32-bit unit that performs FP arithmetic, logical operations (OR, AND, XOR), shifts, FP to INT conversion, and complement.	7	409
DFI	A lightweight DDR3 memory controller that efficiently manages the interface between a system and DDR3 memory devices.	2	430
HUF	A synchronous Huffman encoding system that compresses 4-bit input data symbols by calculating their frequencies, generating Huffman codes, and outputting a compressed serial bitstream.	**10**	**1,572**
SDRAM	A controller for synchronous dynamic random-access memory (SDRAM) with a Wishbone bus interface.	1	604
SHA256	A cryptographic unit that computes a 256-bit hash value from a 24-bit input message using the SHA-256 algorithm.	3	**1,412**
SM4	A synchronous implementation of the SM4 encryption/decryption algorithm, supporting both modes through a 128-bit key and data interface.	**9**	**1,142**
SPI	A lightweight SPI controller supporting Master mode with FIFO-based data transfer and interrupt-driven operation.	1	839
UART	Facilitates serial communication between a host and peripherals, supporting configurable baud rates and stop bits.	3	639
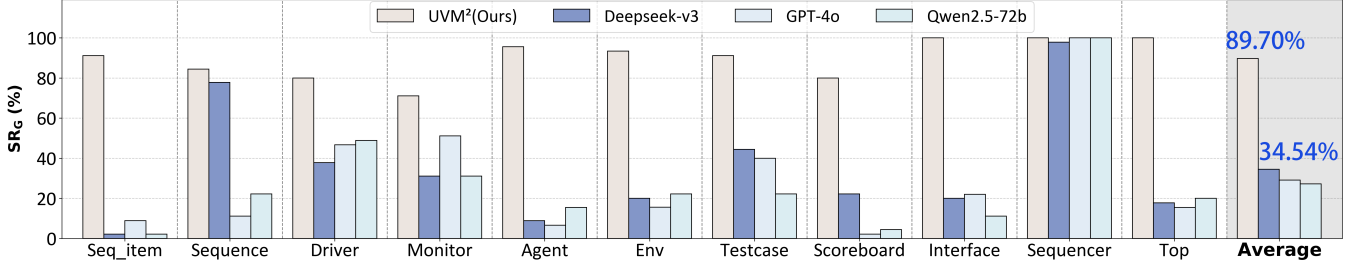
Fig. 9: SR_G of 11 UVM components with UVM^2 against SOTA LLMs

RQ2: How does the verification completeness achieved by UVM^2 compare to existing LLM-based verification approaches? This question investigates whether UVM^2 can generate testbenches that reach comparable or higher code and functional testcase coverage than other LLM-driven methods.

RQ3: How much of a performance gain in terms of efficiency can end-to-end verification using UVM^2 achieve compared to that of expert engineers? This question explores whether UVM^2 can reduce the total time needed to complete the functional verification process relative to manual effort.

RQ4: How does the repair mechanism influence the success rate of UVM testbench generation? This question examines whether incorporating automatic repair significantly improves the ability of UVM^2 to generate usable testbenches after initial failures.

RQ5: How does the optimisation mechanism in UVM^2 affect functional coverage improvement? This research question evaluates the effectiveness of the optimization strategy in increasing the achieved coverage metrics during simulation.

C. Results and Discussions

The results of our experiments are presented as follows, with each aligned to its respective research question.

Result 1: Fig. 9 illustrates the SR_G of UVM^2 for various UVM components, achieving an average success rate of 89.70%. Notably, the three components generated from the template technique achieve a 100% success rate, validating the reliability of this approach. Among components generated by AgentG, agent, env, testcase, and seq_item exceed 90% SR_G. However, driver and monitor, two components requiring in-depth domain knowledge of timing information like handshakes, show lower success rates (approximately 80%), reflecting the challenge of encoding complex designs without explicit guidance.

UVM^2 is also compared with three widely-used LLM baselines: GPT-4o (closed-source), Deepseek-v3, and Qwen2.5-72b (two open-source models widely adopted for their strong problem-solving capabilities). To ensure experimental rigor, each generated component was

used to replace the corresponding module in a manually crafted UVM testbench developed by experienced engineers, while the remaining components were kept unchanged. This approach ensures a valid evaluation since individual components cannot be tested in isolation due to inherent interdependencies, as illustrated in Fig. 4. For each generation task, the rest of the testbench was provided as reference context. Among these baselines, Deepseek-v3 achieves the highest overall success rate at 34.54%. In contrast, UVM^2 reaches a success rate that is 2.59× higher, surpassing all baselines across every component category. Notably, in the agent and seq_item categories, where UVM^2 particularly excels, baseline performance is minimal, as agent success rates are 8.88%, 6.66%, and 15.55%, and seq_item success rates are 2.22%, 8.89%, and 2.22% for Deepseek-v3, Qwen2.5-72b, and GPT-4o, respectively. This significant discrepancy underscores critical limitations in baseline capabilities.

Fig. 10 provides concrete examples of such errors and their corrected versions, illustrating how LLM outputs deviate from UVM design norms without structured guidance.

Insufficient protocol analysis/constraint generation. UVM requires precise sequence constraints (e.g., DFI protocol specifications). Legacy LLMs fail to parse protocols, generating invalid constraints (e.g., incorrect address ranges). This oversight can derail simulations entirely, as critical scenarios remain unaddressed, not merely reducing coverage but rendering verification incomplete and unreliable

Hallucinations in naming/logic. LLMs invent invalid UVM class names or misapply methods. Naming like HUF_Driver driver (as presented in Fig. 10) isn't inherently wrong. However, in this UVM component, other parts are named as drv. This naming inconsistency leads to mismatches during instantiation, triggering runtime errors. Such lapses in naming coherence violate UVM's structural norms, severely undermining the testbench's reliability.

Inadequate understanding of TLM mechanism. LLMs often omit critical TLM declarations, such as uvm_analysis_imp_decl. Without these foundational elements, subsequent method usage becomes flawed, including incorrect instantiation of uvm_analysis_imp. This

Fig. 10: Four categories of errors in LLM-generated UVM components and their corrections.
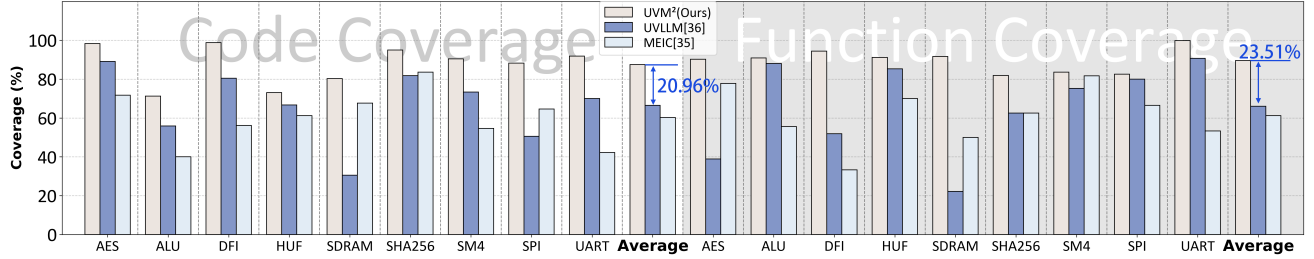

Fig. 11: Code Coverage and Function Coverage of UVM², UVLLM, MEIC

combination of missing declarations and misapplied methods disrupts the TLM-based communication that underpins UVM verification, ultimately rendering components non-functional.

Ambiguous component responsibilities. Each UVM module must adhere to its role. For instance, the top module's duty includes proper DUT instantiation. Failing this (as in the incorrect example) violates the principle of clear - cut responsibilities. Such role - neglect doesn't just cause minor issues but invalidates the entire verification setup, highlighting that overlapping or overlooked duties can collapse the UVM testbench's effectiveness.invalidates testbench correctness.

These results demonstrate that relying solely on legacy LLMs for UVM testbench generation is infeasible due to domain knowledge gaps. By contrast, UVM² significantly enhances feasibility through targeted techniques (e.g., templates, iterative repair), achieving robust performance across both simple and complex components.

Result 2: We measured the coverage of the testbench generated by UVM² across 9 modules and compared it with two instances (MEIC and UVLLM) of LLMs applied in functional verification. Notably, since function coverage relies on the setting of expected functional scenarios by humans, the function coverage in this experiment used the functional scenarios defined by experienced engineers when constructing the testbench as the expected scenarios.

Fig. 11 demonstrates the verification coverage of UVM² and the other two control groups in each module. Specifically, the average code coverage of UVM² reaches 87.44%, which is 20.96% and 27.24% higher than UVLLM and MEIC respectively. In terms of function coverage, UVM² achieves 89.58%, which is 23.51% and 28.40% higher than UVLLM and MEIC respectively. Among them,

DDR3 achieves the highest code coverage of 98.31% and function coverage of 94.44%. As the number of RTL code lines increases and the number of sub-modules grows, the coverage of UVM² decreases but still remains competitive. HUF, an RTL code with nearly 1,500 lines and containing ten submodules, has a code coverage of 73.07%, however, the function coverage is 91.21% since several code segments contribute to just one function point in this design. Moreover, the coverage of UVM² in the verification of each module is higher than that of the other two works. This result indicates that UVM² significantly improves the test completeness in LLM-based verification. Meanwhile, UVM² also practices the theory of applying LLM to UVM-based verification, demonstrating that LLM-based testing does not have to rely solely on random stimuli.

Result 3: We recorded the time required for UVM² to complete each process, as well as the total time, comparing it with the time taken by experienced verification engineers to build UVM testbenches.

As shown in Table II, UVM² significantly outperforms human verification engineers in achieving similar coverage conditions. For the HUF module, UVM² achieves a speedup of 14.68×, while for less complex modules like DFI, the performance gap widens, with a speedup of up to 38.82×. The two most time-consuming phases, testbench generation and testcase supplement, have average execution time of 41.34 minutes and 20.84 minutes, respectively. As illustrated in Fig. 1, these phases account for approximately 30% and 50% of the total workflow time. In comparison, human experts typically spend 8.10 hours and 13.51 hours on these tasks, yielding speedups of 11.75× and 38.90× for UVM² respectively. These results demonstrate UVM²'s potential to significantly reduce

TABLE II: Completion Time of UVM^2 against Human Verification Engineers. The time statistics for each stage incorporate multiple generation attempts as required. The "Simulation" time includes compile, elaboration, simulation and repair iterations for components.

Design	UVM^2					Human	Speedup
	Planning	Generation	Simulation	Supplement	Total	Total	
AES	3.55min	12.52min	6.47min	5.83min	28.37min	16.22h	34.30x
ALU	3.43min	15.22min	5.28min	8.51min	32.44min	16.13h	29.83x
DFI	2.12min	11.53min	5.90min	5.41min	24.96min	16.15h	38.82x
HUF	25.45min	72.22min	40.85min	25.42min	163.94min	40.12h	14.68x
SDRAM	32.18min	80.22min	45.24min	25.35min	182.99min	39.34h	12.90x
SHA256	22.48min	48.43min	30.52min	30.74min	132.17min	33.26h	15.10x
SM4	22.52min	50.31min	35.50min	30.32min	138.65min	30.25h	13.09x
SPI	24.46min	65.25min	42.32min	35.47min	167.50min	31.26h	11.20x
UART	4.29min	16.33min	12.52min	20.55min	53.69min	20.32h	22.71x
Average	15.61min	41.34min	24.96min	20.84min	102.75min	27.01h	**15.77x**

TABLE III: SR_G of UVM^2-generated UVM testbenches across three iterative verification rounds. "Gain" indicates the percentage improvement from the previous round.

Design	Round1	Round2	Gain	Round3	Gain
AES	93.33%	95.56%	2.23%	95.56%	0.00%
ALU	86.67%	91.11%	4.44%	93.33%	2.22%
DFI	82.22%	91.11%	8.89%	91.11%	0.00%
HUF	44.44%	77.78%	33.34%	77.78%	0.00%
SDRAM	42.22%	86.67%	44.45%	86.67%	0.00%
SHA256	66.67%	84.44%	17.77%	84.44%	0.00%
SM4	57.77%	82.22%	24.45%	82.22%	0.00%
SPI	64.44%	80.00%	15.56%	80.00%	0.00%
UART	84.44%	86.67%	2.23%	88.89%	2.22%
Average	69.13%	86.17%	17.04%	86.67%	0.50%

verification time and highlight its competitiveness in accelerating functional verification.

Result 4: We evaluated the generation success rate of UVM testbenches with different iterations for the repair mechanism in UVM^2.

Table III presents the generation success rate of UVM testbenches for each module across three rounds (including one initial generation round, followed by two repair iterations) under the condition of multiple tests. The results show that with our repair mechanism, the final generation success rate is 86.67%, reflecting an increase of 17.54% compared to the initial generation success rate of 69.13%. We observed that in AES and UART, the generation success rate could reach 93.33% in the round 1, while for RTL like HUF and SDRAM, multiple rounds were needed to generate a correct UVM testbench. This reveals the model's deficiency in understanding in-depth domain expertise regarding timing handshakes, interface protocols in IC design, and verification domains. Meanwhile, the improvement in the generation success rate between the third and second rounds is insignificant, merely 0.50%. Further increasing the number of repair iterations would not yield better results. This validates that setting the number of iterations in the repair mechanism to 2 is reasonable, avoiding unnecessary resource waste.

Result 5: We evaluated the effect of the optimization mechanism in UVM^2 on verification coverage by comparing the coverage with and without the testcase supplement phase. The results, presented in Fig. 12, highlight the improvements in both code and function coverage. Specifically, the optimization mechanism led to an increase of 7.6% and 9.7% in code and function coverage, separately.

Notably, the optimization is especially beneficial for certain modules. For instance, the SPI module witnesses a 17.7% increase in code coverage, while the ALU module experiences a 29.5% improvement in function coverage. However, some modules showed slight gains. In the SM4 module, for example, despite a 5.1% rise in code coverage, functional coverage hasn't improved noticeably. This outcome can be attributed to the fact that, in practical designs, certain function points require the joint triggering of multiple code blocks. In the case of the SM4 module, once function coverage reached 83.5%, an additional 5.4% in code coverage was insufficient to trigger new function points.
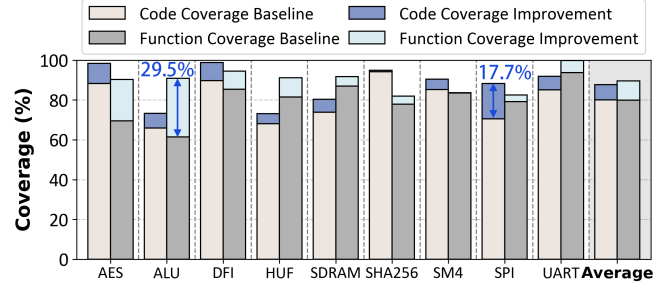

Fig. 12: Coverage improvement via testcase supplement

It is important to note that the average time required for the testcase supplement phase was 20.84 minutes, as shown in Table II. Despite the time-cost overhead, the improvements in coverage demonstrate the competitiveness and effectiveness of the optimisation mechanism.

V. CONCLUSION

In this work, we explored the use of LLMs for hardware design verification and identified key challenges that hinder their effectiveness. To address these issues, we introduced UVM^2 a structured framework that enhances LLM capabilities through hierarchical guidance and systematic prompting. UVM^2 enables the generation of UVM testbench with a generation success rate of 86.67%. With approximately 88% coverage, the average runtime is 102.75 minutes, achieving up to 38.82x speedup in development efficiency.

Recognizing the limitations of existing benchmarks, where most DUTs are under 150 lines, we developed a new benchmark(up to 2k lines) to better reflect real-world verification demands. UVM^2 seamlessly integrates with industrial tools such as Synopsys VCS to automate the entire verification workflow. It also incorporates a optimisation mechanism, allowing generated testbenches to reach an average 87.44% code coverage and 89.58% function coverage, outperforming state-of-the-art solutions by 20.96% and 23.51% respectively.

Our results demonstrate that UVM^2 significantly narrows the gap between LLM capabilities and the stringent requirements of industrial-grade hardware verification. However, challenges remain. Enhancing LLM understanding of hardware protocols and semantics, and embedding richer verification knowledge into the generation process, are essential directions for future work. By advancing these areas, we move closer to realizing autonomous, expert-level verification assistance powered by foundation models.

VI. ACKNOWLEDGEMENT

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