Engineering Science and Technology, an International Journal 67 (2025) 102068

Contents lists available at ScienceDirect

Engineering Science and Technology, an International Journal

journal homepage: www.elsevier.com/locate/jestch

Full length article

Effect of Dual Three-Phase configurations and interleaved carrier-based PWM techniques on the DC-Link current stress

Ander DeMarcos [a],*, Milijana Odavic [b], Endika Robles [a], Unai Ugalde [a], Jon Andreu [a]

[a] Department of Electronic Technology, University of the Basque Country (UPV/EHU), Plaza Ingeniero Torres Quevedo 1, Bilbao, 48013, Spain
[b] Department of Electronic and Electrical Engineering, University of Sheffield, Mappin St, Sir Frederick Mappin building, Sheffield, S1 3JD, United Kingdom

ARTICLE INFO

Keywords:
Multiphase
Interleaving
Dual Three-Phase (DTP) configuration
Double Zero-Sequence Injection (DZSI) PWM
DC-Link capacitor
DC-Link current spectrum

ABSTRACT

Dual Three-Phase (DTP) winding configurations are gaining importance in automotive powertrains, where the DC-Link capacitor plays a critical role in terms of power density and reliability, as it accounts for approximately 40% of the inverter's volume and about 30% of its failures. This work systematically analyses the influence of various DTP configurations (S0-DTP, A30-DTP, S60-DTP) and DTP-specific Double Zero-Sequence Injection (DZSI) PWM techniques on the DC-Link capacitor current spectrum to minimize its RMS value. Using the Double Fourier Integral formalism, this work derives analytical expressions for input current harmonics, identifies dominant ripple components, and assesses interleaving strategies to suppress these harmonics, thereby reducing RMS current stress on the capacitor. The findings are validated through experimental measurements, which confirm that proper selection of DZSI-PWM techniques and interleaving angles leads to up to 85% reduction in capacitor RMS current stress compared to standard non-interleaved modulation, thus enhancing power converter reliability without additional hardware modifications. These insights offer practical design guidelines for electric vehicle powertrains and high-performance multiphase inverters.

1. Introduction

The electric vehicle powertrain is undergoing significant advancements in power electronics and machine drive systems. The introduction of wide-bandgap semiconductors, rare earth-free motors, and innovative converter architectures is radically transforming the electric mobility landscape, emphasizing enhancements in specific power (kW/kg), power density (kW/ℓ), efficiency (%), and cost ($/kW) [1]. This trend has revived interest in multiphase machines since the early 20th century, prompting researchers to reconsider the choice of three-phase machinery. In this context, a whole new field has been explored, gradually extending the knowledge from three-phase drive technology to cover multiphase modelling, design, modulation, and control [2,3]. However, the most interesting aspect of this advancement is not just extending existing three-phase technologies, but also discovering new ways to exploit the extra advantages offered by multiphase machines. These advantages include power distribution among phases, reducing torque ripple, improving torque density via harmonic current injection (in concentrated winding machines), minimizing DC-Link current ripples [4] (resulting in smaller DC-Link capacitors), and enabling intrinsic fault-tolerant operation [5,6].

In order to benefit from such advantages, multiple three-phase topologies have emerged as well-established solutions [7,8]. These include the dual three-phase (DTP) configuration (Fig. 1-①), which has garnered attention for several reasons: (i) it strikes a favourable balance between performance and complexity; (ii) it enables a smooth transition from three-phase technologies by utilizing multiple generic and modular three-phase inverters, each feeding independent three-phase winding sets (Fig. 1-②) [9,10]; and (iii) it exhibits excellent fault tolerance, in handling open- and short-circuit events, as well as DC power supply faults (only when each inverter is supplied from independent power supplies).

DTP configurations can be classified into symmetrical (S) and asymmetrical (A) depending on the phase displacement (δ) between the two three-phase sets (Fig. 1-①: S0-DTP ($\delta = 0°$), A30-DTP ($\delta = 30°$), and S60-DTP ($\delta = 60°$) configurations). Significant efforts are being made to study the performance of these promising DTP architectures. Recent works have addressed various aspects of these configurations, focusing on the spatial harmonics of the magnetomotive force, the parameters of the equivalent circuits in the different planes, and the current quality at the output, through their winding configuration and coil-pitch (chorded vs unchorded windings) [11,12]. Furthermore, in [13] the total current

* Corresponding author.
E-mail addresses: ander.demarcosa@ehu.eus (A. DeMarcos), m.odavic@sheffield.ac.uk (M. Odavic), endika.robles@ehu.eus (E. Robles), unai.ugalde@ehu.eus (U. Ugalde), jon.andreu@ehu.eus (J. Andreu).

https://doi.org/10.1016/j.jestch.2025.102068
Received 26 December 2024; Received in revised form 6 March 2025; Accepted 11 April 2025
Available online 3 May 2025

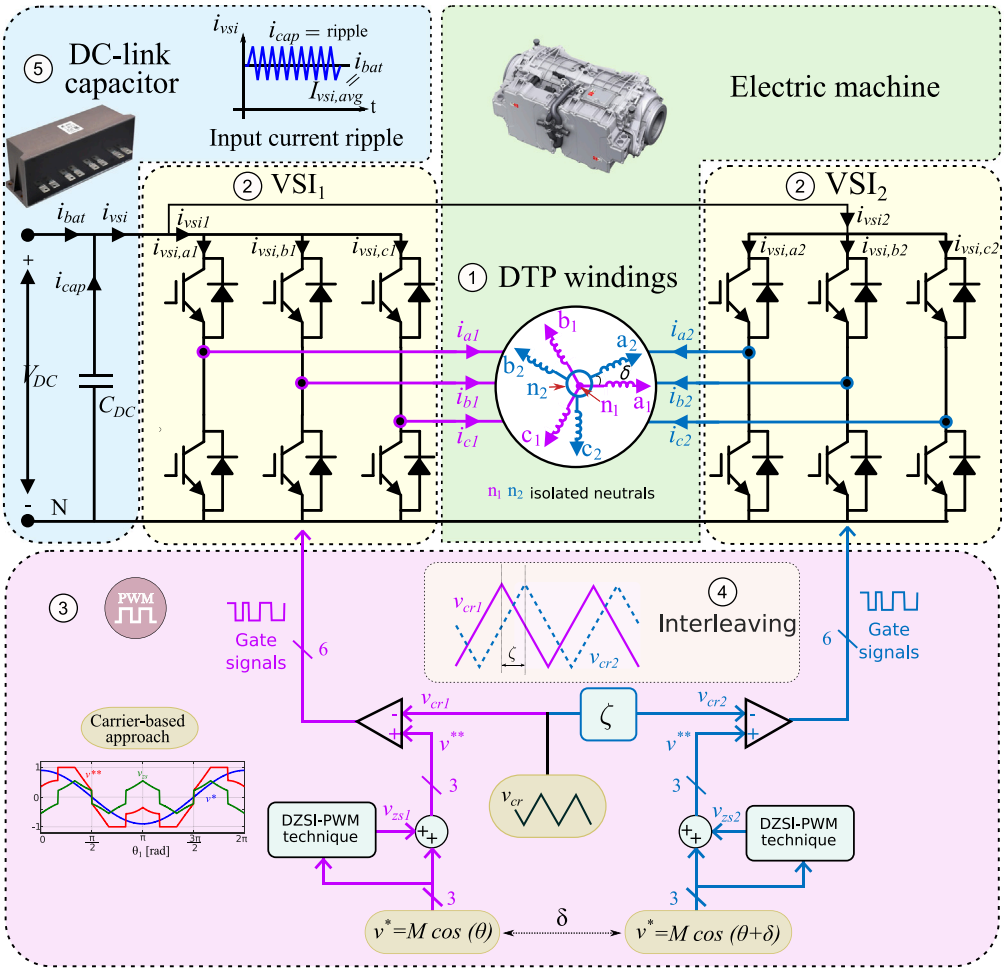


Fig. 1. Conceptual architecture of an DTP configuration considering all its constituent elements and the concepts analysed in this work.

harmonic distortion is compared between the S60-DTP and A30-DTP configurations using direct controllers.

Voltage-Source Inverters (VSIs) along with Pulse-Width Modulation (PWM) techniques are widely used for controlling the output power of those electric traction systems. For DTP configurations, Double Zero-Sequence Injection (DZSI) PWMs are usually preferred over other Carrier-Based (CB) PWMs, because they consist of duplicating the standard three-phase VSI and their well-studied three-phase CB-PWMs, typically used in three-phase drives [14]. Thus, an independent zero-sequence is injected into each three-phase set (Fig. 1-②, VSI$_1$ and VSI$_2$). Table 1 and Fig. 2 show how these CB-PWMs are implemented, where $v^* = M\cos(\theta)$ is the modulating signal, v_{zs} is the injected zero-sequence component, $v^{**} = v^* + v_{zs}$ is the modified modulating signal, θ is the modulating signal's angular position and the modulation index (M) is defined as $M = \hat{V}_1/(0.5 \cdot V_{DC})$ [15], where $\hat{V}_1$ is the peak phase-neutral voltage and V_{DC} is the DC-Link voltage. Fig. 1-③ also shows how two homopolar sequence components are injected equally but phase-shifted by δ to each three-phase set composing the DTP. When modulating the VSI$_2$, it is feasible to phase-shift the carrier an interleaving angle ζ, as depicted in Fig. 1-④.

Exploiting this additional degree of freedom has proven beneficial for multiple aspects of DTP-based systems. In particular, interleaving has been extensively studied in the context of torque ripple, vibrations, and output ripple, with promising results for both S0-DTP and A30-DTP configurations [16–19]. Furthermore, interleaving modulation schemes have been successfully applied to minimize common-mode voltage (CMV) of A30-DTP permanent magnet synchronous machines [20].

Beyond its impact on the inverter output, interleaving has also been widely employed to reduce the input current in parallelled three-phase VSIs [21–24]. This aspect is especially relevant given that DC-Link capacitors (Fig. 1-⑤, C_{DC}) can account for up to 40% of the total volume of the VSI [3,25–27] and are directly linked to 30% of VSI failures [28–30]. However, despite these potential benefits, publications analysing interleaved modulation for DTP machines remain limited, often focusing on a single winding configuration or specific DZSI-PWM techniques [31–35].

Therefore, this work differs from previous research by thoroughly investigating the S0-DTP, A30-DTP, and S60-DTP configurations together with the DZSI-PWM techniques. First, it analyses how the winding configurations inherently affect the DC-Link current ripple without interleaving. Then, the potential of introducing the interleaved variants of these modulation techniques is explored to further reduce the current stress on the DC-Link capacitor without requiring additional hardware, thereby enabling for smaller and more reliable DC-Link capacitors. Thus, this approach not only enhances converter reliability but also contributes to the optimal design of inverters in electric traction systems.

2. Theoretical basis of the DC-link capacitor current stress in DTP configurations

The DC-Link capacitor is responsible for reducing the low-frequency voltage ripple at the input of the converter, in both steady and transient states, as well as storing the necessary energy to allow an instantaneous power balance between the converter input (battery) and output (DTP load). It must provide a low-impedance path for switching currents in order to decouple and reduce the current ripple from the battery (stress

Table 1
Phase leg reference voltage e.g. v^{**} for inner integral limits of (1).
Source: Adapted from [14].

θ [rad] / CB-PWM	$-\pi$	$-5\cdot\frac{\pi}{6}$	$-2\cdot\frac{\pi}{3}$	$-\frac{\pi}{2}$	$-\frac{\pi}{3}$	$-\frac{\pi}{6}$	0	$\frac{\pi}{6}$	$\frac{\pi}{3}$	$\frac{\pi}{2}$	$2\cdot\frac{\pi}{3}$	$5\cdot\frac{\pi}{6}$	π
SPWM	$M\cdot\cos(\theta)$												
MINMAX-PWM	$\frac{\sqrt{3}}{2}M\cdot\cos(\theta-\frac{\pi}{6})$			$\frac{3}{2}M\cdot\cos(\theta)$			$\frac{\sqrt{3}}{2}M\cdot\cos(\theta+\frac{\pi}{6})$	$\frac{\sqrt{3}}{2}M\cdot\cos(\theta-\frac{\pi}{6})$		$\frac{3}{2}M\cdot\cos(\theta)$		$\frac{\sqrt{3}}{2}M\cdot\cos(\theta+\frac{\pi}{6})$	
D-PWMMAX	$1-\sqrt{3}\cdot M\cdot\cos(\theta+\frac{5\pi}{6})$				1					$1+\sqrt{3}\cdot M\cdot\cos(\theta+\frac{5\pi}{6})$			
D-PWMMIN	-1		$1+\sqrt{3}\cdot M\cdot\cos(\theta+\frac{5\pi}{6})$				$1-\sqrt{3}\cdot M\cdot\cos(\theta+\frac{5\pi}{6})$					-1	
D-PWM1	-1	$1-\sqrt{3}\cdot M\cdot\cos(\theta+\frac{5\pi}{6})$		$1+\sqrt{3}\cdot M\cdot\cos(\theta+\frac{\pi}{6})$		1		$1-\sqrt{3}\cdot M\cdot\cos(\theta+\frac{5\pi}{6})$		$1+\sqrt{3}\cdot M\cdot\cos(\theta+\frac{\pi}{6})$		-1	
D-PWM3	$1-a$	-1	$-1+b$	$1-a$	1	$-1+b$	$-1-a$	1	$1+b$	$-1-a$	-1	$1+b$	

$a=\sqrt{3}\cdot M\cdot\cos(\theta+\frac{5\pi}{6})$ $b=\sqrt{3}\cdot M\cdot\cos(\theta+\frac{\pi}{6})$

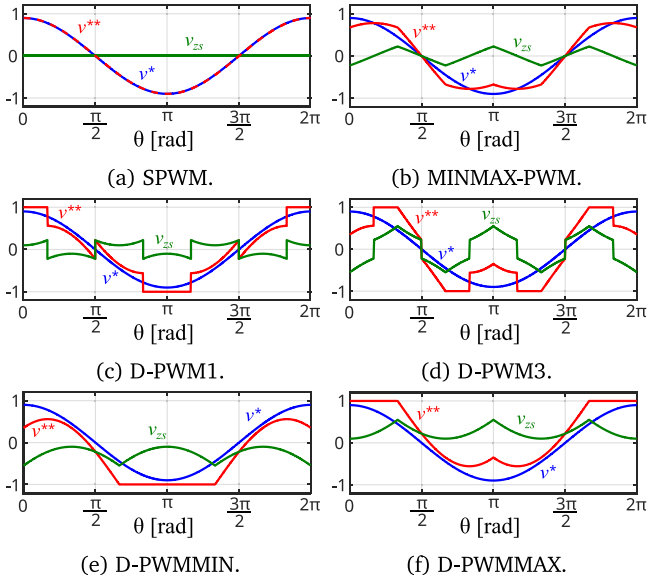


Fig. 2. Voltage reference modulating signals and zero-sequence components for the most relevant CB-PWMs with $M = 0.9$.

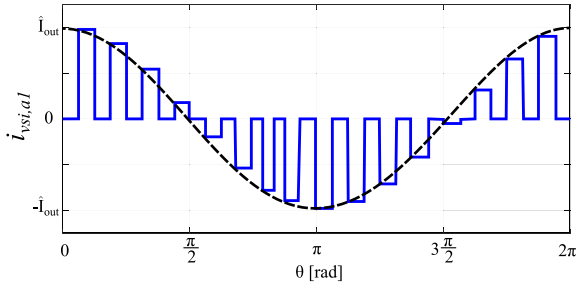


Fig. 3. Conceptual pulsed current waveform for one branch of the DTP configuration e.g. $i_{vsi,a1}$.

reduction and lifetime extension) and maintain a proper voltage at the VSI input, thus ensuring the control of the fundamental voltage amplitude at the converter output. The RMS value of the current through the DC-Link capacitor ($I_{cap,rms}$) is a key parameter in its selection, as it directly impacts its size, thermal stress and reliability [36,37]. Since 'the worst case scenario' for the DC-Link capacitor occurs when the whole input current ripple goes through the DC-Link capacitor [23,38], $I_{cap,rms}$ is obtained by adding up the RMS values of its harmonics. Thus, the critical role played by the DC-Link capacitor makes it necessary to study its current spectrum for DTP configurations in detail.

The input current of the leg 'a' of the VSI_1 (Fig. 1, $i_{vsi,a1}$) consists of pulses whose width is determined by the applied PWM technique, and height proportional to the output instantaneous phase current (i_{a1}). Fig. 3 shows the conceptual pulsed waveform of this current. Its harmonic spectrum can be calculated using the double Fourier integral method. This analysis assumes that the carrier frequency is much higher than the fundamental frequency ($f_{sw} \gg f_1$); and therefore, that the phase currents are sinusoidal, with amplitude $\hat{I}_{out}$, phase lag ϕ, and having no high-frequency ripple current [33]. It is also assumed that the carrier signal and modulation signal are in phase, neglecting the effect of any phase shift between them on the harmonics distribution:

$$C_{mn}^{i_{vsi,a1}} = \frac{1}{2\pi^2}\int_0^{2\pi}\left(\int_{-\left[1+v_{a1}^{**}(y)\right]\frac{\pi}{2}}^{\left[1+v_{a1}^{**}(y)\right]\frac{\pi}{2}} \hat{I}_{out}\cos(y-\phi)\cdot e^{j(mx+ny)}dx\right)dy \tag{1}$$

where C_{mn} represents each harmonic which arise at frequency values equalling $f_h = m f_{sw} + n f_1$, where m is the carrier index variable and n is the baseband index variable. In addition, $x = 2\pi f_{sw} t$ and $y = 2\pi f_1 t = \theta$ are two time variables which represent the carrier and modulating angles, respectively. Eq. (1) shows that the complex Fourier coefficient associated with the inverter input current is proportional to the amplitude of the load current $\hat{I}_{out}$. Therefore, from this point onward, all these Fourier coefficients are normalized with respect to $\hat{I}_{out} = 1$ A to facilitate comparison.

Table 1 shows the phase leg voltage reference v_{a1}^{**} in order to solve the inner integral limits of (1) depending on the selected PWM technique. Fig. 2 shows graphically the waveform of this leg voltage reference.

The Fourier coefficients for the consecutive branches *'b1'* and *'c1'* ($C_{mn}^{i_{vsi,b1}}$ and $C_{mn}^{i_{vsi,c1}}$) of the VSI_1 can be obtained from (1) by replacing ny with $n(y+\frac{2\pi}{3})$ and $n(y+\frac{4\pi}{3})$, respectively. Likewise, $C_{mn}^{i_{vsi,a1}}$ can be phase-shifted as

$$C_{mn}^{i_{vsi,1b}} = C_{mn}^{i_{vsi,a1}}\cdot e^{jn\frac{2\pi}{3}}, \tag{2}$$

$$C_{mn}^{i_{vsi,1c}} = C_{mn}^{i_{vsi,a1}}\cdot e^{jn\frac{4\pi}{3}}. \tag{3}$$

Now, because $i_{vsi1} = i_{vsi,a1} + i_{vsi,b1} + i_{vsi,c1}$,

$$\begin{aligned} C_{mn}^{i_{vsi1}} &= C_{mn}^{i_{vsi,a1}}\cdot\left[1 + e^{jn\frac{2\pi}{3}} + e^{jn\frac{4\pi}{3}}\right] \\ &= C_{mn}^{i_{vsi,a1}}\cdot\left[1 + 2\cos\left(n\frac{2\pi}{3}\right)\right]; \end{aligned} \tag{4}$$

which clearly show that $C_{mn}^{i_{vsi1}} = 0$ for all values of n except for 0 and multiples of 3. Therefore, although at the output currents of any three-phase VSI the triplen harmonics cancel each other out, the opposite occurs at the input.

Fig. 4 depicts the spectra of i_{vsi1}, obtained through numeric calculations of (4) using Matlab, for $\cos\phi = 1$[1], as a function of M, for the most relevant DZSI-PWMs. These input current spectra are inherent to any traditional three-phase VSI, but are also applicable to DTPs since they are composed of two such three-phase VSIs. Fig. 4 also illustrates

[1] The value of $cos\phi$ for standardized driving cycles in electric drives oriented to electric vehicle applications is close to unity [33].

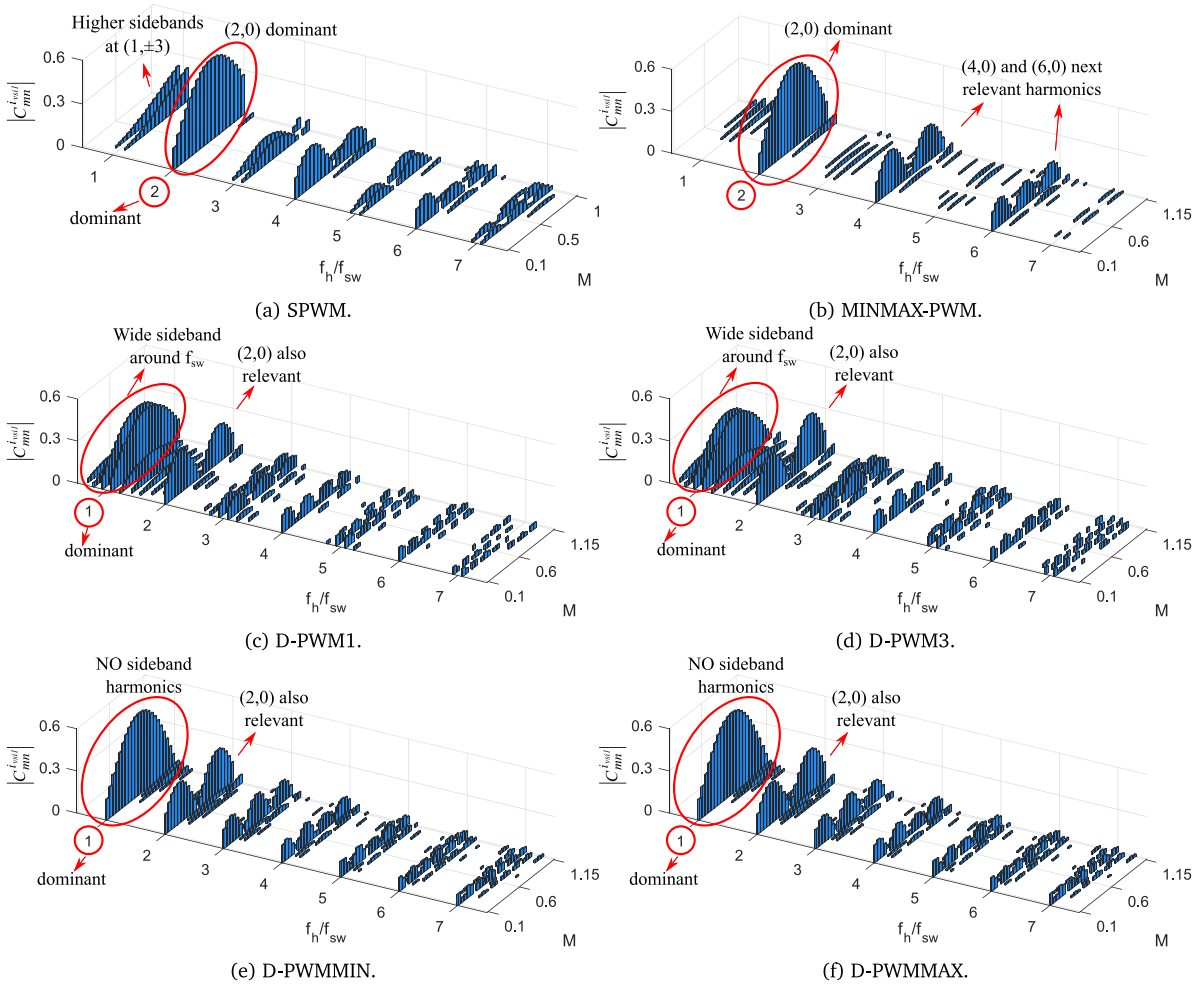


Fig. 4. Normalized input current harmonics of the VSI_1 ($i_{vsi1}/\hat{I}_{out}$) using double Fourier integral formalism $\left(|C^{i_{vsi1}}_{mn}|\right)$ as a function of the modulation index (M), for the analysed DZSI-PWM techniques, with $\cos\phi = 1$.

how continuous modulations (SPWM and MINMAX-PWM) exhibit a dominant harmonic, characterized by the highest amplitude, at $(m, n) = (2, 0)$, whereas discontinuous modulations tend to have more sidebands around $m = 1$. It is worth noting that the input current spectra of D-PWMMAX and D-PWMMIN are almost equal, and due to the absence of abrupt changes in the modified modulating signal (v^{**}), they exhibit fewer sidebands.

Usually, each three-phase subsystem has its own isolated neutral point (Fig. 1, n_1 and n_2). Thus, the Fourier coefficients for the input current harmonics of the second three-phase stator winding result

$$C^{i_{vsi2}}_{mn} = C^{i_{vsi,a1}}_{mn} \cdot \left[1 + 2\cos\left(n\frac{2\pi}{3}\right)\right] \cdot e^{jn\delta}, \tag{5}$$

where $e^{jn\delta}$ corresponds to the δ displacement of the second stator winding with respect to the first one, and consequently, to the phase shift between the modulating signals (v^*) of both VSIs. By adding (4) and (5) the Fourier coefficients of the input current for any DTP configuration

$$C^{i_{vsi}}_{mn} = C^{i_{vsi,a1}}_{mn} \cdot \left[1 + 2\cos\left(n\frac{2\pi}{3}\right)\right] \cdot \left[1 + e^{jn\delta}\right] \tag{6}$$

are obtained. The main difference between the input current harmonics of a three-phase system (4) and a dual three-phase VSI (6) lies in the $\left[1 + e^{jn\delta}\right]$ term. This means that the phase displacement δ between the two three-phase sets determines how the input current harmonics interact, as it modifies (or even cancels) some high-frequency harmonics. Table 2 determines how harmonics interact when summing i_{vsi1} and i_{vsi2} (Fig. 1-②). When the modulus is 2, the harmonics are in phase and reinforce each other. If the modulus is $\sqrt{2}$, a relative phase shift of $\pi/2$ occurs between them. Conversely, if the modulus is 0, those harmonics are completely cancelled.

Table 2
Modulus of $\left[1 + e^{jn\delta}\right]$ derived from (6) for different DTP configurations.

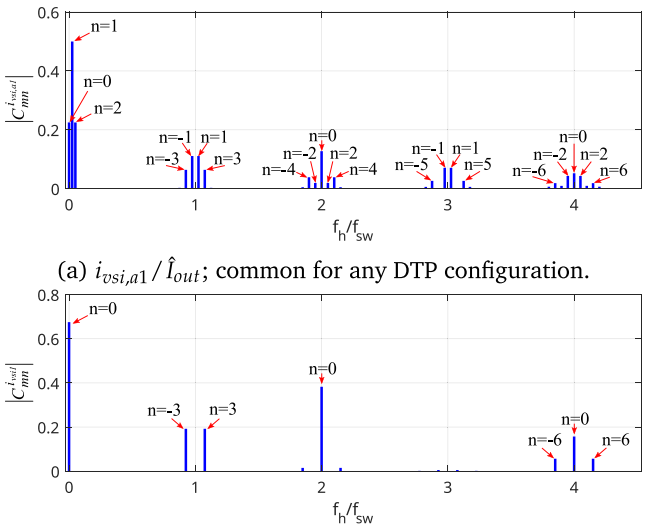
n	S0-DTP	A30-DTP	S60-DTP
$0, \pm12, \pm24 \ldots$	2	2	2
$\pm\mathbf{3}, \pm9, \pm15 \ldots$	2	$\sqrt{2}$	**0**
$\pm\mathbf{6}, \pm18, \pm30 \ldots$	2	**0**	2

Note: The most relevant harmonics inherent to DZSI-PWM techniques that are cancelled are emphasized in **bold**.

Therefore, the harmonic cancellation effects inherent to each DTP configuration can be summarized as follows:

- S0-DTP does not cancel any extra harmonic.
- A30-DTP cancels n = ±6 and n = ±18. However, these i_{vsi} harmonics are not relevant for any DZSI-PWM because their amplitudes are negligible compared to other harmonics.
- S60-DTP cancels inherently n = ±3 sideband harmonics, which are dominant for D-PWM1 and D-PWM3.

As an example, Figs. 5 and 6 show the normalized input current spectrum amplitudes for the leg 'a' of the VSI_1, the whole VSI_1, and for S0-DTP, A30-DTP and S60-DTP, respectively, applying the SPWM technique, $M = 0.9$ and $\cos\phi = 1$. These plots reveal that $n = 0, 3, 6, 9$



(a) $i_{vsi,a1}/\hat{I}_{out}$; common for any DTP configuration.

(b) $i_{vsi1}/\hat{I}_{out}$; common for any DTP configuration.

Fig. 5. Normalized input current harmonics for the leg 'a' of the VSI_1 ($i_{vsi,a1}/\hat{I}_{out}$) and the whole VSI_1 ($i_{vsi1}/\hat{I}_{out}$) using double Fourier integral formalism: $\left(|C^{i_{vsi,a1}}_{mn}|\right)$ and $\left(|C^{i_{vsi1}}_{mn}|\right)$, under SPWM, $M = 0.9$ and $\cos\phi = 1$.

harmonics are the only harmonics arising in i_{vsi1} and i_{vsi} for any DTP configuration. Fig. 6 also depicts that S0-DTP, A30-DTP and S60-DTP exhibit different i_{vsi} current harmonics due to the phase displacement δ between the two three-phase sets. It is highly remarkable that $(1, \pm 3)$ sideband harmonics are cancelled for S60-DTP 6(c).

Since the worst-case scenario for the DC-Link capacitor occurs when all the ripple of this i_{vsi} flows through it,

$$I_{cap,rms} = \sqrt{I^2_{vsi,rms} - I^2_{vsi,avg}}\,, \tag{7}$$

where the rms value of the input current is

$$I_{vsi,rms} = \sqrt{\sum_{n=0}^{\infty}\left(\frac{\left|C^{i_{vsi}}_{0n}\right|}{\sqrt{2}}\right)^2 + \sum_{m=1}^{\infty}\sum_{n=-\infty}^{\infty}\left(\frac{\left|C^{i_{vsi}}_{mn}\right|}{\sqrt{2}}\right)^2}, \tag{8}$$

and from the principle of power conservation, the average value of the input current of any DTP configuration results

$$I_{vsi,avg} = \frac{6}{4} M \hat{I}_{out} \cos\phi. \tag{9}$$

3. Interleaving schemes to reduce the DC-link current stress in DTP configurations

Applying the concept of interleaving (Fig. 1-④) to the Fourier double integral formalism of i_{vsi2} yields

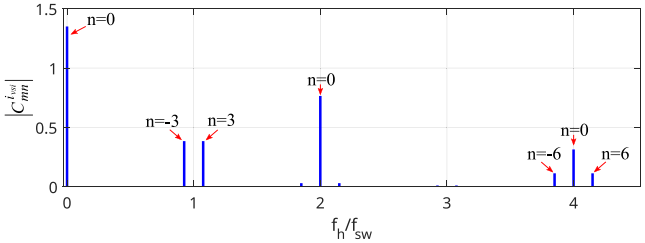
$$C^{i_{vsi2}}_{mn} = C^{i_{vsi,a1}}_{mn} \cdot \left[1 + 2\cos\left(n\frac{2\pi}{3}\right)\right] \cdot e^{jn\delta} \cdot e^{jm\zeta}, \tag{10}$$

where $e^{jm\zeta}$ corresponds to interleaving; i.e. the additional phase shift of the second carrier signal (Fig. 1, v_{cr2}), which involves replacing mx with $m(x + \zeta)$ in (1). Consequently, this new parameter affects $C^{i_{vsi}}_{mn}$ of (6), leading to

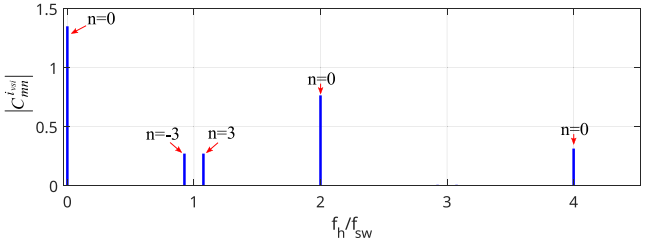
$$C^{i_{vsi}}_{mn} = C^{i_{vsi,a1}}_{mn} \cdot \left[1 + 2\cos\left(n\frac{2\pi}{3}\right)\right] \cdot \left[1 + e^{j(n\delta + m\zeta)}\right]. \tag{11}$$

Now, making the second term of (11), $\left[1 + e^{j(n\delta+m\zeta)}\right]$, equal to zero, interleaving angle values equalling

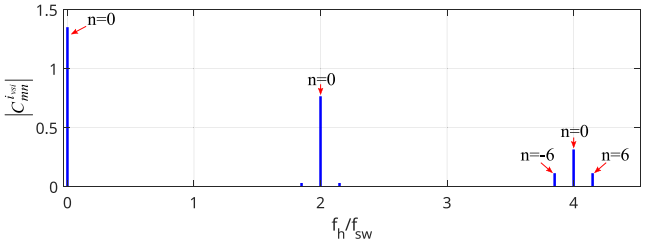
$$\zeta = \frac{(2k+1)\cdot\pi - n\delta}{m} \qquad \forall k \in \mathbb{Z}^+ \tag{12}$$



(a) $i_{vsi}/\hat{I}_{out}$; specific for S0-DTP configuration.

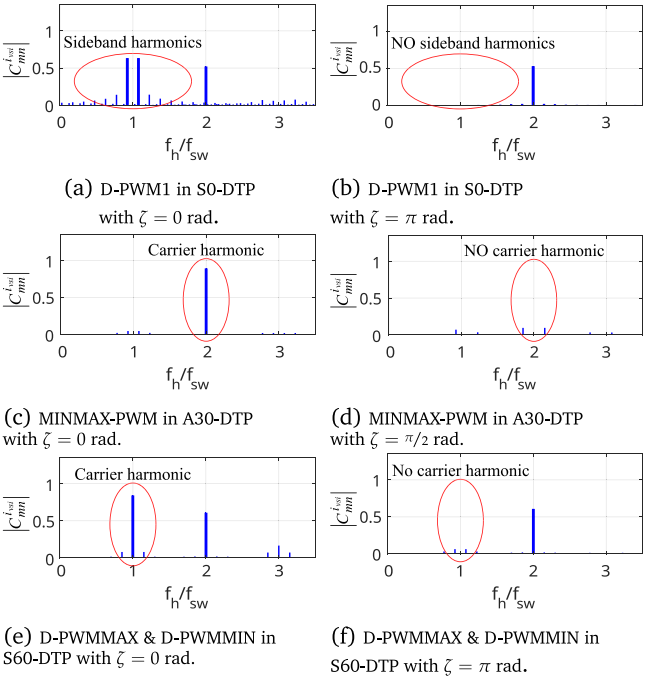


(b) $i_{vsi}/\hat{I}_{out}$; specific for A30-DTP configuration.



(c) $i_{vsi}/\hat{I}_{out}$; specific for S60-DTP configuration.

Fig. 6. Normalized input current harmonics ($i_{vsi}/\hat{I}_{out}$) using double Fourier integral formalism $\left(|C^{i_{vsi}}_{mn}|\right)$, for S0-DTP, A30-DTP and S60-DTP respectively, under SPWM, $M = 0.9$ and $\cos\phi = 1$.



(a) D-PWM1 in S0-DTP with $\zeta = 0$ rad.

(b) D-PWM1 in S0-DTP with $\zeta = \pi$ rad.

(c) MINMAX-PWM in A30-DTP with $\zeta = 0$ rad.

(d) MINMAX-PWM in A30-DTP with $\zeta = \pi/2$ rad.

(e) D-PWMMAX & D-PWMMIN in S60-DTP with $\zeta = 0$ rad.

(f) D-PWMMAX & D-PWMMIN in S60-DTP with $\zeta = \pi$ rad.

Fig. 7. Normalized input current harmonic ($i_{vsi}/\hat{I}_{out}$) cancellation using double Fourier integral formalism $\left(|C^{i_{vsi}}_{mn}|\right)$, through interleaving schemes, for S0-DTP, A30-DTP and S60-DTP, under some DZSI-PWM techniques, $M = 0.9$ and $\cos\phi = 1$.

Table 3
Most relevant cancelled DTP input current harmonics depending on the interleaving angle ζ according to (12).

	Interleaving (ζ)	S0-DTP	A30-DTP	S60-DTP
$C_{mn}^{i_{vsi}}$	0 rad	–	$(m, \pm 6)$	$(m, \pm 9)$ $(m, \pm 3)$
	$\pi/2$ rad	$(2, n)$	$(1, -9)$ $(1, +3)$ $(2, 0)$ $(3, -3)$	$(2, \pm 6)$ $(2, 0)$ $(4, \pm 9)$ $(4, -3)$
	π rad	$(1, n)$	$(1, 0)$ $(2, \pm 6)$ $(3, 0)$ $(4, \pm 6)$ – –	$(1, \pm 6)$ $(1, 0)$ $(2, -9)$ $(2, -3)$ $(3, \pm 6)$ $(3, 0)$

m = any carrier index e.g. $1, 2, 3, \ldots$.
n = any baseband index e.g. $0, \pm 3, \pm 6, \pm 9, \ldots$.

Table 4
Parameters of the test rig.

Parameter	Symbol	Value	Units
Resistance	R	5.1	Ω
Inductance	L	1.93	mH
DC-Link voltage	V_{DC}	40	V
Switching frequency	f_{sw}	2	kHz
Fundamental frequency	f_1	50	Hz
Power factor of fundamental	$\cos\phi$	0.98	p.u.

that cancels some specific (m, n) input current harmonics can be obtained. In this sense, and because the dominant harmonic is the most important component when it comes to computing the RMS value of the whole current spectrum through the DC-Link capacitor, the interleaving angle can and will be exploited to remove this dominant harmonic.

Table 3 summarizes the most significant interleaving angles and the harmonic orders being cancelled. This table shows that, while A30-DTP and S60-DTP cancel specific (m, n) harmonics, S0-DTP cancels the entire sidebands around a carrier frequency index (m). Using the information from this table along with the dominant i_{vsi1} harmonics depicted in Fig. 4, it is possible to identify which combination of machine (δ) and interleaving angle (ζ) is most effective in reducing the RMS current through the DC-Link capacitor, thanks to the cancellation of the DTP current harmonics.

Thus, for an S0-DTP machine, an angle of $\zeta = \pi/2$ rad is the best choice for continuous PWMs as it removes $(2, n)$, whereas $\zeta = \pi$ rad is better for discontinuous techniques by removing $(1, n)$. For the A30-DTP machine, $\zeta = \pi/2$ rad benefits continuous PWMs, as well as D-PWM1 and D-PWM3, since $(2, 0)$ and $(1, 3)$ are cancelled. $\zeta = \pi$ rad is best choice for D-PWMMAX and D-PWMMIN in this kind of machines since it removes the dominant harmonic $(1, 0)$. Finally, the S60-DTP without interleaving benefits D-PWM1 and D-PWM3 because it removes inherently all $(m, \pm 3)$ harmonics. When a phase shift of $\zeta = \pi/2$ rad is applied, continuous PWMs are benefited by eliminating the harmonic $(2, 0)$, and a phase shift of $\zeta = \pi$ rad is best option for D-PWMMAX and D-PWMMIN, as it removes $(1, 0)$.

Fig. 7 depicts three significant examples of input current harmonic cancellation using interleaving schemes, one case for each DTP machine. These examples match (12) and Table 3. A collateral effect of cancelling an existing harmonic is that other harmonics can increase their amplitude; $\left[1 + e^{j(n\delta + m\zeta)}\right] \in [0, 2]$. This suggests that the angle which removes the dominant input current harmonic and the one that minimizes $I_{cap,rms}$ may differ. This is analysed and demonstrated in the following section.

4. Experimental validation

The experimental validation of the current through the DC-Link capacitor was conducted using the specific hardware setup described in Fig. 8 and Table 4. The employed test rig consisted of an RL load, which met the requirements outlined in the mathematical development of Section 2, where only sinusoidal output currents and a high switching frequency relative to the fundamental frequency ($f_{sw} \gg f_1$) are required. Furthermore, two three-phase VSIs were used, which together are equivalent to a six-phase VSI in terms of input current ($i_{vsi} = i_{vsi1} + i_{vsi2}$).

In this experimental setup, i_{vsi1} and i_{vsi2} were reconstructed through the measured currents i_{cap1}, i_{cap2}, i_{bat1}, and i_{bat2}, since the bus bar structure of commercial VSIs prevents their direct measurement. After obtaining these variables, the two currents were added to obtain the equivalent input current of the DTP-specific VSI (i_{vsi}). Then, since the worst-case scenario for the DC-Link capacitor happens when all the ripple current i_{vsi} flows through it, $I_{cap,rms}$ was determined using (7). Additionally, in order to normalize $I_{cap,rms}$, it is necessary to divide it by the amplitude of the output current fundamental, obtained applying a Fast Fourier Transform to the measured output current.

Fig. 9 shows the RMS value of the normalized DC-Link current ($I_{cap,rms}/\hat{I}_{out}$) as a function of the modulation index (M) for the most relevant interleaved and non-interleaved DZSI-PWM techniques and symmetrical and asymmetrical DTP configurations (S0-DTP: $\delta = 0°$; A30-DTP: $\delta = 30°$; S60-DTP: $\delta = 60°$). This figure contains both theoretical values (as continuous lines) and experimental measurements ('*' markers). Fig. 9 also shows $I_{cap,rms,min}$ obtained by performing a sweep over the interleaving angle, as mentioned in Section 3. There are some specific combinations of modulation techniques, modulation indexes, and DTP winding configurations where the interleaving angle that minimizes $I_{\text{cap,rms}}$ is neither $\zeta = \pi/2$ rad nor $\zeta = \pi$ rad. A strong correspondence can be observed between the experimentally obtained results and the mathematical developments of this study. From these data, Table 5 summarizes the suggested interleaving angles depending on the DZSI-PWM technique for S0-DTP, A30-DTP and S60-DTP. Besides, it shows their respective $I_{cap,rms}$ reduction compared with their non-interleaved operations.

In case interleaving is not feasible or desired:

(a1) S60-DTP machine combined with D-PWM1 and D-PWM3 results in a reduction in $I_{cap,rms}$ up to a 79.6% compared to MINMAX-PWM. This occurs due to the elimination of the $(m, \pm 3)$ sideband harmonic pairs.
(a2) If a continuous modulation or D-PWMMAX (behaving as continuous modulation in terms of $I_{cap,rms}$) is chosen, there are no significant differences among any of these DTP configurations. Although the improvement is minimal, for SPWM, the machine with the lowest $I_{cap,rms}$ is the S60-DTP, whereas for MINMAX-PWM and D-PWMMAX, the A30-DTP prevails.

In the scenario where interleaving is feasible or preferred:

(b1) For continuous modulations, it is recommended to use an interleaving angle of $\zeta = \pi/2$ rad, regardless of the DTP configuration, as it significantly reduces $I_{cap,rms}$ e.g. almost up to 80% for MINMAX-PWM (Figs. 9(d)–9(f)).
(b2) For D-PWM1, $\zeta = \pi$ rad interleaving is recommended for the S0-DTP machine, $\zeta = \pi/2$ rad for the A30-DTP, and non-interleaved operation for the S60-DTP.
(b3) For D-PWM3 and D-PWMMAX, the analysis becomes more complex as the interleaving angle that minimizes $I_{cap,rms}$ depends on the modulation index applied at that moment. For the S0-DTP with D-PWM3 and D-PWMMAX modulations, a combination of $\zeta = \pi$ rad and $\zeta = \pi/2$ rad is recommended, as observed in Figs. 9(j) and 9(m). In contrast, for the S60-DTP, a combination of non-interleaved operation and $\zeta = \pi/2$ rad is recommended. For the A30-DTP modulated by D-PWM3, $\zeta = \pi/2$ rad is enough to reduce $I_{cap,rms}$ on the whole range of M, and for D-PWMMAX, a combination of $\zeta = \pi$ rad and $\zeta = \pi/2$ rad is again chosen.

Table 5
Suggested interleaved DZSI-PWM variants and their Max. $I_{cap,rms}$ reduction compared with their non-interleaved operations for S0-DTP, A30-DTP and S60-DTP.

DZSI-PWM	S0-DTP		A30-DTP		S60-DTP	
	ζ [rad]	Max. $I_{cap,rms}$ reduction [%]	ζ [rad]	Max. $I_{cap,rms}$ reduction [%]	ζ [rad]	Max. $I_{cap,rms}$ reduction [%]
SPWM	$\pi/2$	66.2	$\pi/2$	62.7	$\pi/2$	62.5
MINMAX-PWM	$\pi/2$	79.0	$\pi/2$	85.0	$\pi/2$	78.8
D-PWM1	π	80.0	$\pi/2$	28.3	0	0.0
D-PWM3	π and $\pi/2$[a]	78.3	$\pi/2$	35.1	0 and $\pi/2$[a]	22.0
D-PWMMAX D-PWMMIN	π and $\pi/2$[a]	79.0	π and $\pi/2$[a]	85.0	0 and $\pi/2$[a]	78.9

[a] Depends on the modulation index (M).

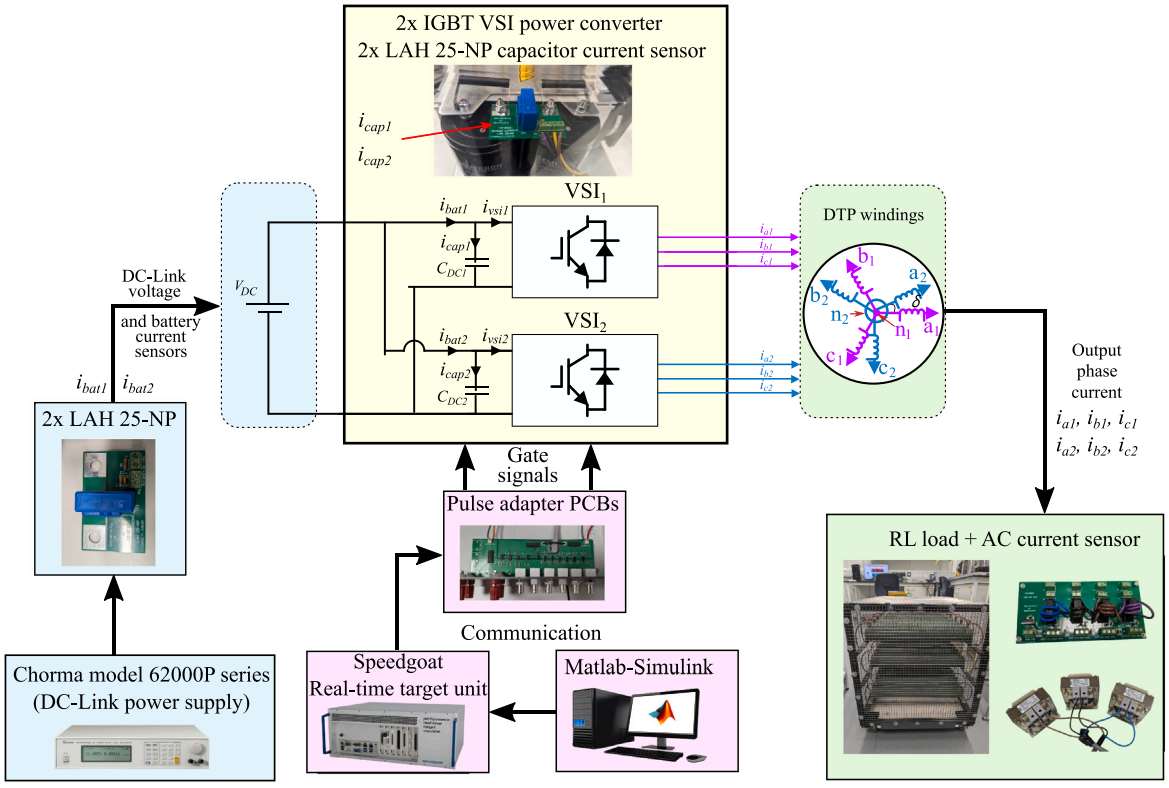


Fig. 8. Hardware and electrical schematics of the experimental set-up.

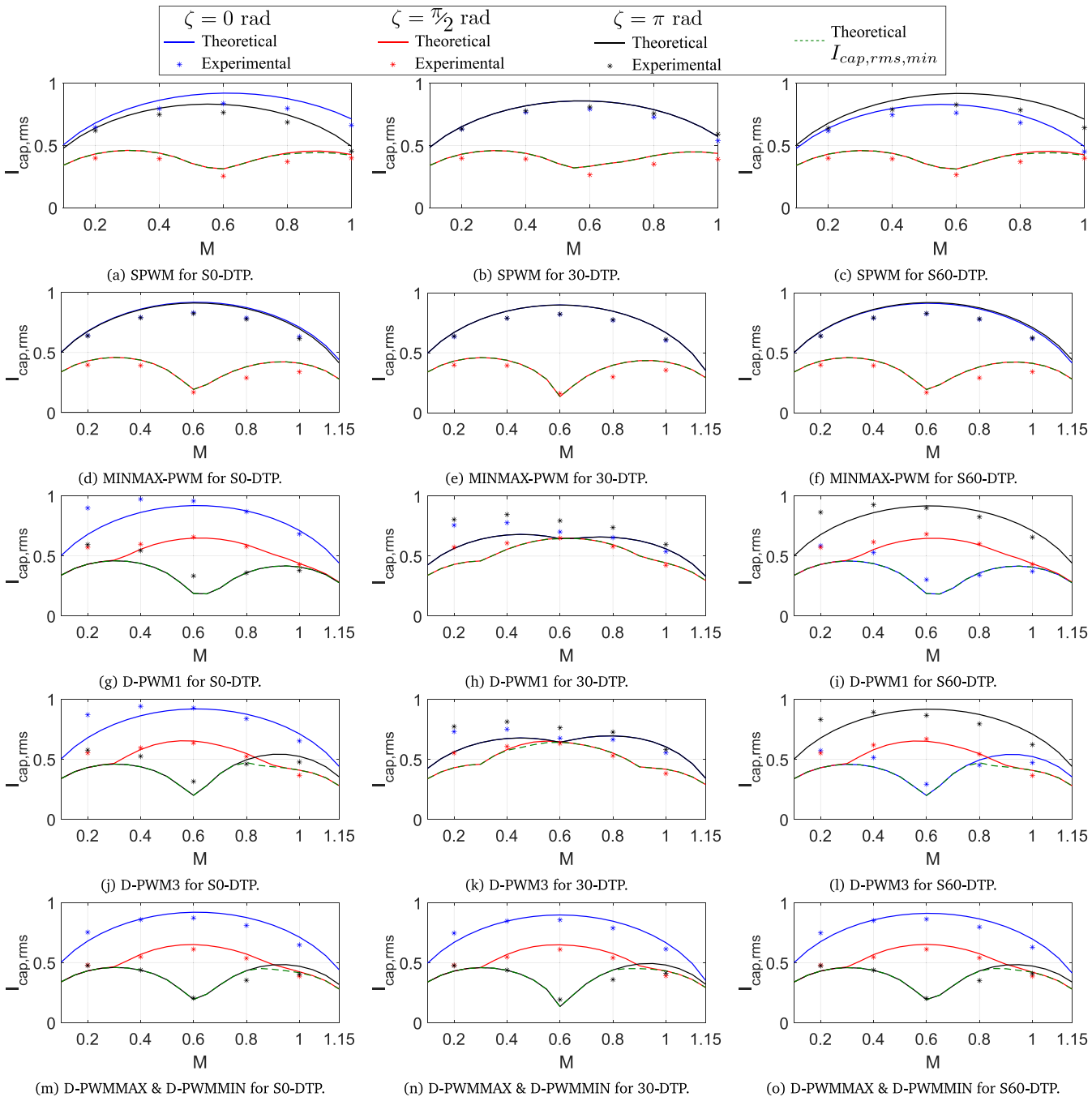
5. Conclusions

The impact of DTP winding configurations, along with interleaved or non-interleaved DZSI-PWMs, on the current through the DC-Link capacitor has been analysed. The aim of this work is to reduce the current stress on this bulky and failure-prone component without using any additional hardware. To achieve this goal, the input current spectra of these DTP configurations has been determined using the Double Fourier Integral formalism. While each phase of the multiphase VSI introduces specific input current harmonics, the interaction between different phases inherent to the chosen DTP configuration mitigates these harmonics and alters the amplitude of some. These current spectra are utilized to obtain $I_{cap,rms}$, a key figure-of-merit related to DC-Link capacitor.

Results from theoretical calculations and experimental measurements reveal that in S60-DTPs, without employing advanced interleaving techniques, but with discontinuous technique like D-PWM1 or D-PWM3, reductions up to a 79.6% in the aforementioned current compared to MINMAX-PWM are achieved. If continuous modulations are preferred, an interleaving angle of $\zeta = \pi/2$ rad is recommended as it considerably reduces $I_{cap,rms}$, regardless of the DTP winding configuration. In contrast, for discontinuous modulations, each machine has its own approach to reduce this metric depending on the modulation index. S0-DTP and A30-DTP machines should employ combinations of $\zeta = \pi/2$ rad and $\zeta = \pi$ rad; whereas S60-DTP should utilize a combination of non-interleaved and $\zeta = \pi/2$ rad schemes.

In conclusion, this work identifies and determines mathematically, through simulation, and via experimental results which combination of DTP configuration (δ) and DZSI-PWM technique, along with its interleaving angle (ζ), is most effective in reducing the RMS current through the DC-Link capacitor. This reduction is achieved by cancelling the dominant DTP input current harmonics, thereby enhancing the reliability of the power converter.

The results obtained in this work pave the way for future research in several directions. A detailed analysis of the effect of each harmonic component represented in this work on the thermal behaviour of the capacitor, considering the frequency dependence of the Equivalent Series Resistance (ESR), would allow for a more accurate correlation between RMS current reduction and capacitor lifespan. Additionally, exploring hybrid modulations and optimizing the interleaving angle could simultaneously improve multiple figure-of-merits of the DTP system. Finally,



(a) SPWM for S0-DTP. (b) SPWM for 30-DTP. (c) SPWM for S60-DTP.

(d) MINMAX-PWM for S0-DTP. (e) MINMAX-PWM for 30-DTP. (f) MINMAX-PWM for S60-DTP.

(g) D-PWM1 for S0-DTP. (h) D-PWM1 for 30-DTP. (i) D-PWM1 for S60-DTP.

(j) D-PWM3 for S0-DTP. (k) D-PWM3 for 30-DTP. (l) D-PWM3 for S60-DTP.

(m) D-PWMMAX & D-PWMMIN for S0-DTP. (n) D-PWMMAX & D-PWMMIN for 30-DTP. (o) D-PWMMAX & D-PWMMIN for S60-DTP.

Fig. 9. RMS value of the normalized DC-Link current ($I_{cap,rms}/\hat{I}_{out}$) as a function of the modulation index (M) for the most relevant interleaved and non-interleaved DZSI-PWM techniques and DTP configurations (S0-DTP: $\delta = 0°$; A30-DTP: $\delta = 30°$; S60-DTP: $\delta = 60°$). It contains both theoretical values (as continuous lines) and experimental measurements ('*' markers), along with the theoretical minimum normalized DC-Link current ($I_{cap,rms,min}/\hat{I}_{out}$) obtained by sweeping the interleaving angle (ζ).

validating these strategies in real-world applications, such as electric vehicle propulsion systems, would provide a more comprehensive assessment of their impact under real operating conditions.

CRediT authorship contribution statement

Ander DeMarcos: Writing – review & editing, Writing – original draft, Visualization, Validation, Software, Methodology, Investigation, Funding acquisition, Formal analysis, Data curation, Conceptualization. **Milijana Odavic:** Writing – review & editing, Supervision, Software, Resources, Investigation, Funding acquisition, Conceptualization. **Endika Robles:** Writing – review & editing, Visualization, Methodology, Data curation. **Unai Ugalde:** Writing – review & editing, Visualization, Validation, Supervision, Project administration, Data curation. **Jon Andreu:** Writing – review & editing, Visualization, Supervision, Resources, Project administration, Methodology, Investigation, Funding acquisition, Data curation, Conceptualization.

Declaration of competing interest

The authors declare that they have no known competing financial interests or personal relationships that could have appeared to influence the work reported in this paper.

Acknowledgements

This work has been supported in part by the Government of the Basque Country within the fund for research groups of the Basque University system IT1440-22, Elkartek Cipeme KK-2024/00053 project, as well as the support of the UPV/EHU pre-doctoral programme (PIF20-305). The authors wish to express their gratitude to UPV/EHU and the University of Sheffield for the valuable access to their infrastructure and the availability of technical resources provided by these universities to obtain the results presented in this work.

References

[1] 2021 Electrification Annual Progress Report, Tech. Rep., Vehicle Technologies Office - Department of Energy (DOE), 2022, https://www.energy.gov/eere/vehicles/articles/2021-electrification-annual-progress-report.

[2] M. Zhang, M. Yuan, J. Jiang, A comprehensive review of the multiphase motor drive topologies for high-power electric vehicle: current status, research challenges, and future trends, IEEE Trans. Transp. Electrif. 11 (1) (2025) 3631–3654, https://doi.org/10.1109/TTE.2024.3443926.

[3] W. Taha, P. Azer, A.D. Callegaro, A. Emadi, Multiphase traction inverters: State-of-the-art review and future trends, IEEE Access 10 (2022) 4580–4599, https://doi.org/10.1109/ACCESS.2022.3141542.

[4] Z. Nie, Multiphase Power Electronic Converters for Electric Vehicle Machine Drive Systems (Ph.D. thesis), McMaster University, 2018, https://macsphere.mcmaster.ca/handle/11375/22851.

[5] G. Yang, H. Hussain, S. Li, J. Zhang, J. Yang, A unified fault-tolerant strategy for multiphase machine with minimum losses in full torque operation range based on closed-form expressions, IEEE Trans. Power Electron. 37 (10) (2022) 12463–12473, https://doi.org/10.1109/TPEL.2022.3172389.

[6] A.G. Yepes, O. Lopez, I. Gonzalez-Prieto, M.J. Duran, J. Doval-Gandoy, A comprehensive survey on fault tolerance in multiphase AC drives, part 1: General overview considering multiple fault types, Machines 10 (3) (2022) 1–134, https://doi.org/10.3390/machines10030208.

[7] S. Rubino, O. Dordevic, R. Bojoi, E. Levi, Modular vector control of multi-three-phase permanent magnet synchronous motors, IEEE Trans. Ind. Electron. 68 (10) (2021) 9136–9147, https://doi.org/10.1109/TIE.2020.3026271.

[8] A.A. Rahman, A. Galassini, M. Degano, G. Buticchi, G. Cristián Pesce, C. Gerada, S. Bozhko, H.A. Almurib, Open and short circuit post-fault control strategies for multi-three-phase interior permanent magnet machines, IEEE Trans. Energy Convers. 37 (1) (2022) 163–174, https://doi.org/10.1109/TEC.2021.3090982.

[9] S. Padmanaban, G. Grandi, F. Blaabjerg, J. Olorunfemi Ojo, P.W. Wheeler, Power sharing algorithm for vector controlled six-phase ac motor with four customary three-phase voltage source inverter drive, Eng. Sci. Technol. an Int. J. 18 (3) (2015) 408–415, https://doi.org/10.1016/j.jestch.2015.02.002.

[10] S. Padmanaban, M. Pecht, An isolated/non-isolated novel multilevel inverter configuration for a dual three-phase symmetrical/asymmetrical star-winding converter, Eng. Sci. Technol. Int. J. 19 (4) (2016) 1763–1770, https://doi.org/10.1016/j.jestch.2016.08.006.

[11] A.S. Abdel-Khalik, M.S. Abdel-Majeed, S. Ahmed, Effect of winding configuration on six-phase induction machine parameters and performance, IEEE Access 8 (2020) 223009–223020.

[12] A. Shawier, M.S. Abdel-Majeed, W.E. Abdel-Azim, A.S. Abdel-Khalik, M.S. Hamad, S. Ahmed, E. Hamdan, N.A. Elmalhy, Effect of winding design on the performance of predictive current control of six-phase induction machine-based propulsion systems, IEEE Access 10 (2022) 80587–80599, https://doi.org/10.1109/ACCESS.2022.3194893.

[13] A. González-Prieto, I. González-Prieto, A.G. Yepes, M.J. Duran, J. Doval-Gandoy, On the advantages of symmetrical over asymmetrical multiphase AC drives with even phase number using direct controllers, IEEE Trans. Ind. Electron. 69 (8) (2022) 7639–7650, https://doi.org/10.1109/TIE.2021.3104588.

[14] D.G. Holmes, T.A. Lipo, Pulse width modulation for power converters: Principles and practice, Wiley-IEEE Press, 2003, https://search.worldcat.org/es/title/52901629.

[15] A.M. Hava, R.J. Kerkman, T.A. Lipo, Simple analytical and graphical methods for carrier-based PWM-VSI drives, IEEE Trans. Power Electron. 14 (1) (1999) 49–61, https://doi.org/10.1109/63.737592.

[16] X. Wang, H. Yan, G. Sala, G. Buticchi, C. Gu, W. Zhao, L. Xu, H. Zhang, Selective torque harmonic elimination for dual three-phase PMSMs based on PWM carrier phase shift, IEEE Trans. Power Electron. 35 (12) (2020) 13255–13269, https://doi.org/10.1109/TPEL.2020.2991264.

[17] W. Zhang, Y. Xu, H. Huang, J. Zou, Vibration reduction for dual-branch three-phase permanent magnet synchronous motor with carrier phase-shift technique, IEEE Trans. Power Electron. 35 (1) (2020) 607–618, https://doi.org/10.1109/TPEL.2019.2910311.

[18] K. Cui, C. Wang, M. Zhou, S. Sun, Comprehensive investigation of space-vector PWM including novel switching sequences for dual three-phase motor drives, IEEE Trans. Transp. Electrif. 9 (1) (2023) 1350–1362, https://doi.org/10.1109/TTE.2022.3198718.

[19] B. Zheng, J. Zou, Y. Xu, G. Yu, L. Wang, P. Zanchetta, High-frequency current harmonic analysis and suppression in dual three-phase PMSMs with advanced carrier phase-hift PWM, IEEE Trans. Power Electron. 39 (2) (2024) 2569–2581, https://doi.org/10.1109/TPEL.2023.3330934.

[20] Z. Shen, D. Jiang, Z. Liu, D. Ye, J. Li, Common-mode voltage elimination for dual two-level inverter-fed asymmetrical six-phase PMSM, IEEE Trans. Power Electron. 35 (4) (2020) 3828–3840, https://doi.org/10.1109/TPEL.2019.2933446.

[21] X. Lyu, Y. Li, D. Cao, DC-link RMS current reduction by increasing paralleled three-phase inverter module number for segmented traction drive, IEEE J. Emerg. Sel. Top. Power Electron. 5 (1) (2017) 171–181, https://doi.org/10.1109/APEC.2017.7930804.

[22] M.-G. Jeong, H.U. Shin, J.-W. Baek, K.-B. Lee, An interleaving scheme for DC-Link current ripple reduction in parallel-connected generator systems, J. Power Electron. 17 (4) (2017) 1004–1013, https://doi.org/10.6113/JPE.2017.17.4.1004.

[23] M. Schiedermeier, F. Schlamp, C. Rettner, M. März, Analytical calculation of the RMS value and the spectrum of the DC-link current of a dual-inverter, IEEE Trans. Power Electron. 37 (1) (2022) 782–794, https://doi.org/10.1109/TPEL.2021.3095520.

[24] B. Yao, Z. Tang, D. Kumar, H. Wang, H. Wang, Optimal modulation strategy for ripple current reduction of DC-link capacitor in multi-drive systems, IEEE Trans. Power Electron. 38 (9) (2023) 1–14, https://doi.org/10.1109/TPEL.2023.3284711.

[25] H. Wen, W. Xiao, X. Wen, P. Armstrong, Analysis and evaluation of DC-link capacitors for high power density electric vehicle drive systems, IEEE Trans. Veh. Technol. 61 (7) (2012) 2950–2964, https://doi.org/10.1109/TVT.2012.2206082.

[26] A. Salem, M. Narimani, A review on multiphase drives for automotive traction applications, IEEE Trans. Transp. Electrif. 5 (4) (2019) 1329–1348, https://doi.org/10.1109/TTE.2019.2956355.

[27] A. Rodionov, A. Acquaviva, Y. Liu, Sizing and energy efficiency analysis of a multi-phase FSCW PMSM drive for traction application, in: Proc. of the Annual Conference of the IEEE Industrial Electronics Society, IECON, 2020, pp. 2069–2074, https://doi.org/10.1109/IECON43393.2020.9254544.

[28] S. Yang, A. Bryant, P. Mawby, D. Xiang, L. Ran, P. Tavner, An industry-based survey of reliability in power electronic converters, IEEE Trans. Ind. Appl. 47 (3) (2011) 1441–1451, https://doi.org/10.1109/ECCE.2009.5316356.

[29] H. Wang, M. Liserre, F. Blaabjerg, Toward reliable power electronics: challenges, design tools, and opportunities, IEEE Ind. Electron. Mag. 7 (2) (2013) 17–26, https://doi.org/10.1109/MIE.2013.2252958.

[30] A. Tcai, I.M. Alsofyani, I.-Y. Seo, K.-B. Lee, DC-link ripple reduction in a DPWM-based two-level VSI, Energies 11 (11) (2018) 1–16, https://doi.org/10.3390/en11113008.

[31] S. Bhattacharya, D. Mascarella, G. Joos, Interleaved SVPWM and DPWM for dual three-phase inverter-PMSM: An automotive application, in: Proc. of the IEEE Transportation Electrification Conference and Expo, ITEC, 2014, pp. 1–6, https://doi.org/10.1109/ITEC.2014.6861785.

[32] A. Rodionov, X. Huang, Y. Liu, Analysis of DC Link current and voltage stress for motor drive application in dual three-phase configuration, in: Proc. of the Annual Conference of the IEEE Industrial Electronics Society, IECON, 2020, pp. 1267–1272, https://doi.org/10.1109/IECON43393.2020.9255043.

[33] A. DeMarcos, E. Robles, U. Ugalde, I. Martinez de Alegria, J. Andreu, Interleaving modulation schemes in asymmetrical dual three-phase machines for the DC-link stress reduction, Machines 11 (267) (2023) 1–31, https://doi.org/10.3390/machines11020267.

[34] A.A. Khan, N.A. Zaffar, M.J. Ikram, DC-link ripple reduction for parallel inverter systems by a novel formulation using multiple space vector-based interleaving schemes, Electron. 12 (6) (2023) 1–22, https://doi.org/10.3390/electronics12061496.

[35] A. Chowdhury, M.E. Haque, S. Das, Y. Sozer, Dynamic interleaving strategy to reduce DC-link ripple of dual three-phase permanent magnet synchronous machine drives by using dscontinuous space vector modulation, IEEE Trans. Power Electron. 40 (1) (2025) 1762–1773, https://doi.org/10.1109/TPEL.2024.3456708.

[36] K. Kuang, X. Guo, C. Li, X. Li, A novel lifetime estimation method and structural optimization design for film capacitors in EVs considering material aging and power losses, IEEE Trans. Device Mater. Reliab. 24 (3) (2024) 365–379, https://doi.org/10.1109/TDMR.2024.3407855.

[37] K. Kuang, X. Guo, C. Li, X. Li, X. Xi, H. Fang, A novel multiscale perspective based hotspot temperature assessment method for film capacitor in DC-link applications, IEEE Trans. Ind. Appl. 60 (6) (2024) 9111–9122, https://doi.org/10.1109/TIA.2024.3429303.

[38] Z. Nie, N. Schofield, Multi-phase VSI DC-link capacitor considerations, IET Electr. Power Appl. 13 (11) (2019) 1804–1811, https://doi.org/10.1049/iet-epa.2019.0062.