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InAs n-i-p Diodes Fabricated using S and Si Ion Implantation

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***Abstract*— Planar Indium Arsenide (InAs) electron avalanche photodiodes (e-APDs) can provide significant avalanche gain with negligible excess noise. Reported InAs e-APDs are so far all top-side illuminated p-i-n diodes. Yet back-side illuminated n-i-p diodes are needed to be compatible with focal plane arrays (bump-bonding process). This work reports n-type ion implantation into i-InAs layer grown on p-InAs layers, forming n-i-p diodes for the first time. Electrical and optical characteristics of S and Si implanted mesa and planar photodiodes are investigated both experimentally and through simulation. The mesa InAs n-i-p diodes fabricated from implanted samples exhibit similar dark current densities to previously reported Be implanted mesa InAs p-i-n diodes. A peak responsivity of 1.09 A/W at 2004 nm wavelength was demonstrated using S implanted detectors after rapid thermal annealing at 600°C for 30s. The simple planar diodes exhibit higher dark current compared to Be implanted planar InAs p-i-n diodes. This is attributed to poor junction isolation resulting from n-type unintentional doping in intrinsic InAs layers. This can be mitigated by adding isolation trenches around the diodes or introducing p-type isolation implant. Therefore, we have demonstrated a promising approach for fabricating bump-bonding compatible and back-illuminated InAs n-i-p planar diodes.**

***Index Terms*—Indium Arsenide (InAs), Avalanche Photodiode (APD), Infrared Detectors, Focal Plane Arrays (FPA), Ion Implantation.**

I. INTRODUCTION

INDIUM Arsenide (InAs) has a room temperature bandgap of 0.35 eV, enabling efficient absorption of optical signals across the entire short-wave infrared band, which is ideal for gas sensing applications using Light Detection and Ranging (LIDAR) [1]. For instance, two major greenhouse gasses, CO_2 and CH_4, have strong absorption peaks around 2000 nm [2] and 1640 nm [3]. The former lies beyond the detection limits of conventional InGaAs photodiodes while the latter is within the absorption tail of InGaAs photodiodes [4], so alternative absorption materials are needed. Furthermore, to increase the range and sensitivity of LIDAR, the LIDAR's optical receiver often uses an avalanche photodiode (APD) rather than a photodiode.

InAs APDs are known as electron avalanche photodiodes (e-APDs), because only electrons can impact ionize for electric fields < 70 kV/cm [5]. They offer low excess noise (a maximum value below 2 even at large gains) as well as very high gain-bandwidth products [6]. This makes InAs e-APDs well suited for LIDAR applications at the extended shortwave infrared wavelengths of 1550 to 3400 nm. Thus, focal plane arrays (FPAs) of InAs e-APDs would be desirable for emerging gas sensing techniques, such as LIDAR-based gas concentration imaging [7].

$Hg_{0.7}Cd_{0.3}Te$ is another e-APD exhibiting gains of 100's to 1000's with negligible excess noise while covering wavelengths up to 4.3 µm [8]. However, the narrow bandgap of $Hg_{0.7}Cd_{0.3}Te$ limits operation to 80-100 K. Furthermore, $Hg_{0.7}Cd_{0.3}Te$ FPAs are in small formats and low densities (most commonly reported ones are 16-element arrays with 80 µm pitch [9],[10]). Compared to $Hg_{0.7}Cd_{0.3}Te$, type-II superlattice (T2SL) photodiodes cover similar wavelengths and offer simpler manufacturability. InAs/GaSb [11] and InGaAs/GaAsSb T2SL [12] FPAs with high pixel density have been demonstrated [13]. However, to achieve appreciable avalanche gain, T2SL materials need to be combined with wide-bandgap multipliers, greatly complicating wafer growth [14]. Hence, InAs is a potential alternative to $Hg_{0.7}Cd_{0.3}Te$ and T2SL APDs for the extended shortwave infrared wavelengths of 1550 to 3400 nm.

Notwithstanding the excellent optoelectronic properties, there are significant design and fabrication challenges for InAs e-APD arrays. Very thick intrinsic regions (in excess of 6 µm) are needed to achieve high gain and low tunneling currents [15]. Using a mesa topology for such thick devices require very deep etches. Yet using the preferred wet chemical etching solutions for InAs produces significant mask undercutting, severely limiting downscaling of mesa device sizes. Dry etching InAs can produce desirable vertical mesa sidewalls but leaves surface defects that increase surface leakage currents [16]. To circumvent this issue planar InAs e-APDs have been investigated.

Planar InAs e-APD fabrication has been improving in recent years. The first planar InAs p-i-n diodes were produced using Be ion implantation [17], followed by planar InAs e-

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APDs with 8 μm of depletion width and an avalanche gain of 330 at 200 K [18]. Utilizing the improved fabrication procedure (Be implantation energy and annealing condition as well as surface treatments) reported in [19], 128-pixel linear arrays of InAs e-APDs with highly uniform gains and responsivities down to 200 K were demonstrated [20]. More recently, high gain, planar InAs APDs with a low noise equivalent power of 45 fW $Hz^{-1/2}$ were used to detect weak optical signals down to < 70 photons per pulse at 1550 nm wavelength [21].

Large format FPAs however bring additional fabrication challenges compared to single-element InAs e-APDs. Integration of FPAs with read out integrated circuits (ROICs) requires bump bonding the InAs APDs to the ROIC, mandating the use of back-illumination for the APDs. This necessitates InAs n-i-p APDs as opposed to the InAs p-i-n APDs demonstrated so far. Ensuring absorption of optical signals in the p-doped region produces electron injection into the avalanche region, maintaining the desirable properties of InAs e-APDs. Hence further FPA progress requires producing n-InAs by ion implantation.

Sulphur and silicon ions were implanted into p-type InAs to form planar n-p junctions by previous authors. For S ions, implantation energy of 400 keV and dose of 8×10^{14} ions/cm^2 were used, followed by annealing at 400 °C for two hours [22]. Later, a wider range of doses (5×10^{14} to 1×10^{16} ions/cm^2) at a fixed energy of 250 keV for S ion implantation into p-type InAs was reported in [23]. Ar implantation was also used in this study to decouple n-type behavior from disordered layers and chemical doping from S implantation. An energy of 250 keV was used with varying doses from 5×10^{14} to 1×10^{16} ions/cm^2. A peak S activation efficiency of 0.3 was obtained using a dose of 5×10^{14} ions/cm^2 and post-implant annealing at 350 °C for 30 minutes. Activation of Si ions in p-type InAs was observed following post-implant annealing between 400 and 700 °C for up to 90 seconds, using samples implanted at energy of 20 keV and doses from 1×10^{14} to 1×10^{15} ions/cm^2 [24]. It is noted that diffusion of S or Si into InAs is rarely pursued because of significant cost and process development. Also, S and Si implant profiles do not redistribute significantly even when annealed up to 550 °C and 700 °C respectively [25], [26], suggesting that higher temperatures may be required for successful donor diffusion. This could cause undesirable acceptor diffusion if Be [17] or Zn [27] are present in the structure. To the best of our knowledge, there has been no report of ion implantation into intrinsic InAs to form n-i-p diodes with a thick intrinsic region required for InAs e-APD FPAs.

In this paper, we report on the implantation and annealing conditions required to form InAs n-i-p diodes. Our experimental conditions used S and Si ions because these are the two lightest dopants, which have yielded n-InAs in previous works. We also investigated the feasibility of using patterned implants to produce planar n-i-p diodes and explored ways of improving planar n-i-p diodes. The data reported in this manuscript is available from ORDA digital repository [28].

II. Experimental Details

The InAs wafer used in this work was grown by molecular beam epitaxy (MBE) at 480 °C. The wafer consisted of a 2 µm p-type InAs layer, doped to 1×10^{18} cm^{-3}, followed by a 3.7 µm unintentionally doped InAs layer. A total of 12 samples from this wafer were used in this work. Selections of implantation conditions relied on implantation and damage profiles simulated using Transport of Ions in Matter (TRIM) [29]. Due to similar mass and radius, the TRIM profiles simulated for S and Si ions were very similar so identical conditions were used for the two ions in this work.

Four sample pieces cleaved from the wafer were labelled as follows: Si.1 and Si.2 for Si implantation; S.1 and S.2 for S implantation. All four pieces were capped with 40 nm thick SiO_2. Ion implantation for Si.1 and S.1 took place without patterning on the sample, whereas Si.2 and S.2 were masked with photoresist to facilitate selective area implants.

TABLE I
Implantation conditions for S and Si ions.

Sample	Annealing Temperature (°C)	Patterned for implantation?
S.1-control	-	
S.1-450	450	
S.1-500	500	
S.1-550	550	
S.1-600	600	No (fabricated into mesa diodes)
Si.1-control	-	
Si.1-450	450	
Si.1-500	500	
Si.1-550	550	
Si.1-600	600	
S.2-500	500	Yes (fabricated into planar diodes)
Si.2-500		

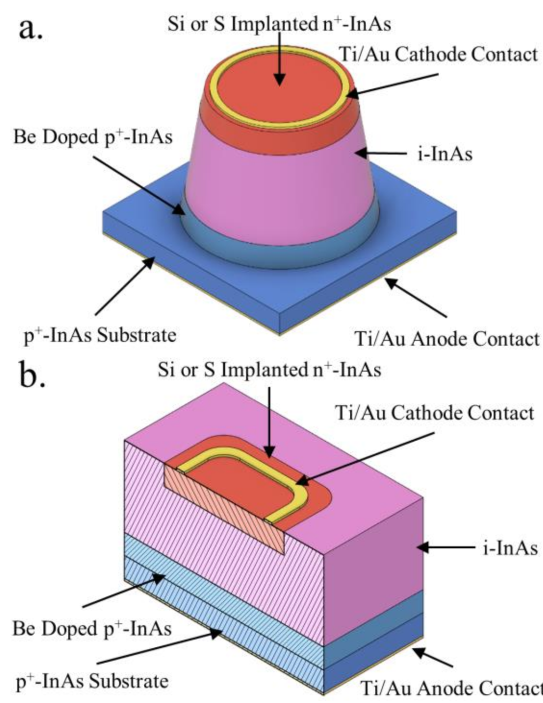

Fig. 1. Illustration of mesa diodes from sample Si.1 and S.1 (a) and planar diodes from sample Si.2 and S.2 (b).

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Samples Si.1 and Si.2 (or S.1 and S.2) were subjected to a double Si (or S) ion implantation with energies of 190 keV and 60 keV and doses of 3×10^{14} ions/cm^2 and 5×10^{13} ions/cm^2 respectively at a tilt angle of 7 °. The higher energy implant would produce a projected range of ~ 200 nm and a peak ion concentration of 1×10^{19} ions/cm^3. The lower energy implant would ensure high dopant concentration extending to the surface, facilitating Ohmic contacts in subsequent fabrication steps.

Following double implantations, samples Si.1 and S.1 were sub-divided into 5 samples each. These were used in post-implantation annealing temperature studies. Control samples were S.1-control and Si.1-control which did not have post-implantation annealing. The remaining samples were annealed at 450, 500, 550, or 600 °C for 30 seconds using a rapid thermal annealing system (RTA). Implantation and fabrication conditions for the 12 samples studied are summarized in Table 1.

Device fabrication was carried out using the un-annealed and annealed samples to produce different-sized mesa diodes (radii of 210, 110, 60 and 35 µm) with Ti/Au top and bottom contacts, as illustrated in Fig. 1(a). Standard contact photolithography, metal deposition and wet etching were used. The mesa etching solution was a 1:1:1 mixture of phosphoric acid, hydrogen peroxide and deionized water. A finishing etch using a 1:8:80 mixture of sulfuric acid, hydrogen peroxide and deionized water was used to limit surface leakage currents. There was no anti-reflection coating on the diodes. Once an optimum annealing temperature was found from samples Si.1 and S.1, this temperature (500 ºC) was used to anneal Si.2 and S.2 which were subsequently used to fabricate planar diodes illustrated in Fig. 1(b).

The S and Si ion profiles of the implanted samples were extracted using secondary ion mass spectroscopy, carried out by Loughborough Surface Analysis LLC, UK. All device characterization was carried out at room temperature. Dark current-voltage characteristics of the fabricated mesa and planar diodes were measured using an Agilent B1500A semiconductor device parameter analyzer. Responsivity and External Quantum Efficiency (EQE) of a given InAs diode was measured at 2004 nm wavelength using 0.1 V reverse bias and a semiconductor diode laser (illuminating the top side of the device). Phase sensitive detection technique was implemented using a SR830 lock-in amplifier and modulated laser light to measure the resultant photocurrent reliably. Sentaurus TCAD was employed for simulating the electric field profiles in the InAs diodes.

III. Results and Discussion

Fig. 2 compares the experimental and simulated profiles for the un-annealed S and Si implanted InAs. The implant profiles of S and Si ions are very similar, as expected from their similar mass and radius. For both S and Si ions, the experimental and the simulated profiles disagree in terms of straggling of the implanted ions. Similar discrepancies were reported in S-implanted InAs (dose of 10^{15} cm^{-2} and energy of 250 keV) with 36 % higher straggling than TRIM simulations [25].

Room temperature reverse current-voltage data for mesa diodes fabricated from Si.1 and S.1 are presented in Fig. 3. As shown in Fig. 3a, the dark current densities for a given reverse bias from different-sized devices agree, confirming the dominance of bulk dark current. Each individual curve in Fig. 3b is the average of 10 devices, with 110 µm radii. They were found to be very uniform. For both ion species diode rectification was observed in annealed and un-annealed devices. For the Si implanted devices, the dependence of the current-voltage characteristic upon post-implant annealing temperature was modest. Even less dependence on annealing temperature was observed from the S implanted samples. There are two plausible explanations for the modest or lack of dependence. Firstly, intrinsic InAs grown by either MBE [30] or metal-organic vapor phase epitaxy (MOVPE) [31] tends to be slightly n-type, resulting in a junction forming between the p-type and intrinsic layers prior to any implantation. Secondly, radiation defects induced by ion implantation have a tendency to become electrically active in narrow bandgap InAs resulting in n-type layers even before post-implant annealing [32].

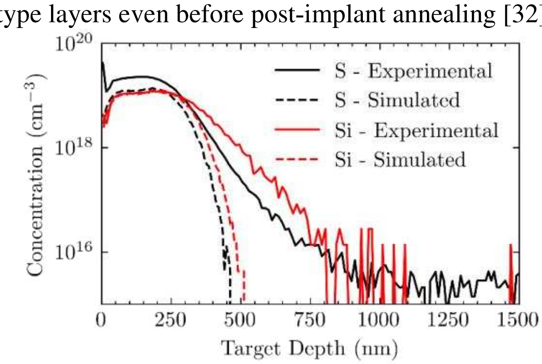

Fig. 2. Experimental and simulated profiles for Si and S ions in the un-annealed implanted InAs samples.

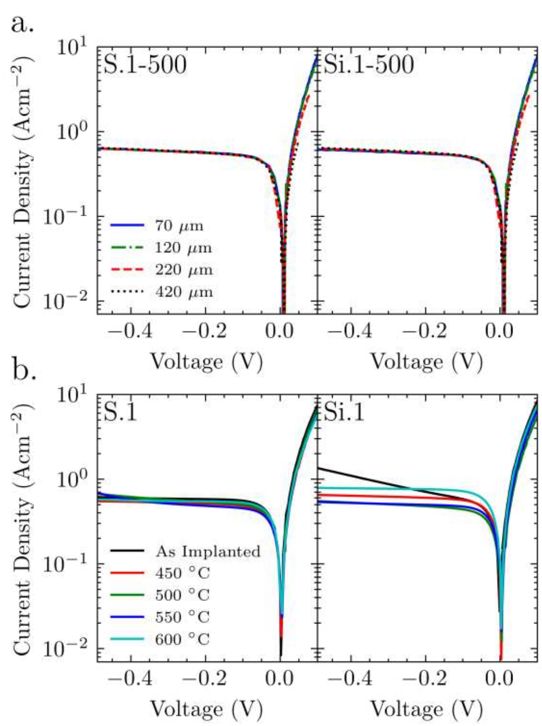

Fig. 3. Room temperature current density of InAs mesa diodes produced using S and Si ion implantation for different device diameters annealed at 500 °C (a) and 220 µm diameter devices annealed at different temperatures (b).

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Room temperature responsivity and EQE values at 2004 nm wavelength for devices with different post-implant annealing temperatures are compared in Fig. 4. Each data point represents the mean value from 10 devices and the error bars represent the standard deviation. For Si implanted devices responsivity increases with annealing temperature up to 500 °C after which the value remained at ~0.95 A/W (EQE ~ 59 %). Responsivity values of S implanted devices show less dependence on annealing temperature, with a maximum responsivity at 1.09 A/W (EQE ~ 68 %) from sample with 600 °C post-implant annealing. The increase in responsivity with annealing temperature may indicate longer minority carrier diffusion lengths in samples annealed at higher temperatures, suggesting that some of the implant damage has been annealed. The peak EQE from this work is 13 % higher than that of Be implanted InAs APDs [20].

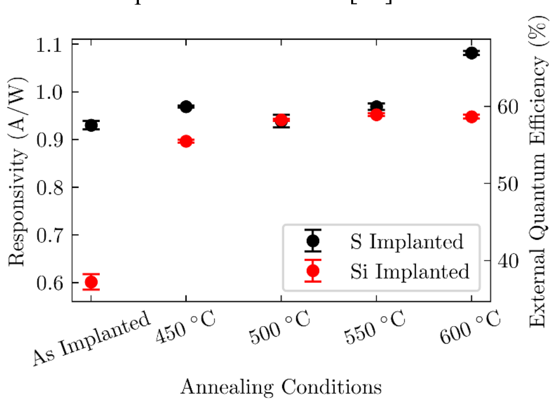

Fig. 4. Responsivity (left axis) and EQE (right axis) at 2004 nm wavelength for S and Si implanted InAs samples with different post-implant annealing temperatures.

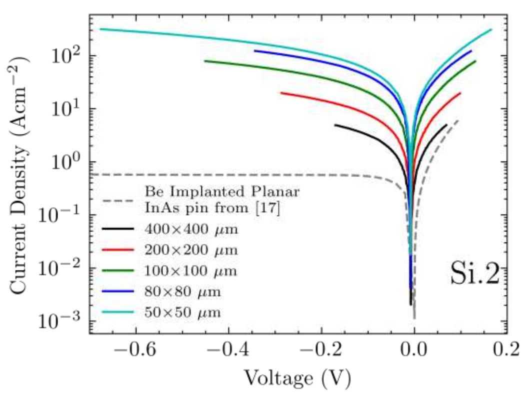

Fig. 5. Current-voltage curves from Si implanted planar nip diodes. Data from [17] for a Be implanted planar pin diode is included for reference.

Dark current densities of planar InAs diodes fabricated from sample Si.2 (annealed at 550 °C) are compared in Fig. 5. The dark current density increases with decreasing intended device area and the same trend was observed for sample S.2. This observation indicates insufficient diode isolation between neighboring planar diodes, which is attributed to the n-type unintentional doping of the epitaxially grown intrinsic layer. In contrast, the reference Be implanted pin diode exhibits strong diode rectifying characteristics. In the p-i-n diode, a p-n junction is formed between the Be-implanted InAs region and the unintentionally n^--InAs layers. This results in significant differences in the electric field profiles of the pin diode (of prior works [17]) and the nip diodes of this work. This is supported by electric field simulations of planar n-i-p diodes with either n or p-type unintentional doping in the i-InAs layer presented in Fig. 6.

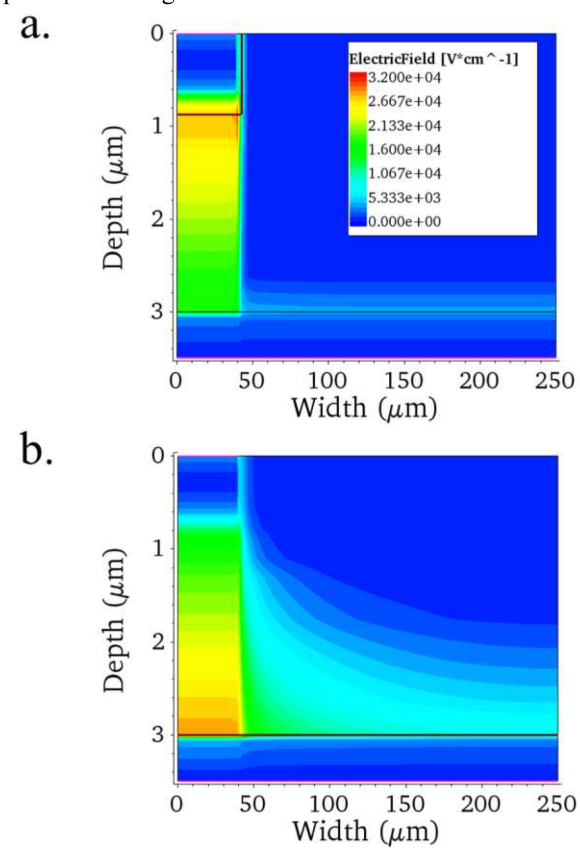

Fig. 6 Simulated cross-sectional electric field profiles for InAs planar n-i-p diodes with top n-implant regions created in i-InAs layer with p-type (a) or n-type (b) unintentional doping.

The electric field simulations assumed that an unintentional doping concentration in the i-InAs layer is 5×10^{14} cm^{-3}, a fairly typical value for epitaxially grown intrinsic InAs [15], [21]. Fig. 6 shows the cross-sectional electric field profiles of the planar n-i-p diodes when the unintentional doping is p-type (a) or n-type (b). With n-type doping in the i-InAs layer, a junction forms away from the top semiconductor surface between the epitaxially grown p-type layer and the intrinsic layer. As a result, the depletion region extends laterally, increasing the device area well beyond the implanted area. Conversely, when the background doping is p-type, a p-n junction forms between the implanted n-type layer and the intrinsic layer resulting in much stronger electric field confinement. Although it is possible to use compensation doping to improve junction isolation, this approach is unlikely to result in good e-APD performance. This is because the unintentional doping levels in InAs layers could fluctuate and compensation doping to levels $<1\times10^{15}$ cm^{-3} (required for wide depletion regions [18]) is difficult to control repeatedly.

Experimental evidence confirms that the high dark current was due to the lack of depletion region confinement. Isolation trenches (down to the epitaxial p-type layer) were etched around each diode in sample Si.2, in an attempt to confine the electric field, as illustrated in Fig. 7(a). Dark current of the resultant diodes reduces significantly (by two orders of magnitude) compared to diodes without isolation trenches, as shown in Fig. 7(b).

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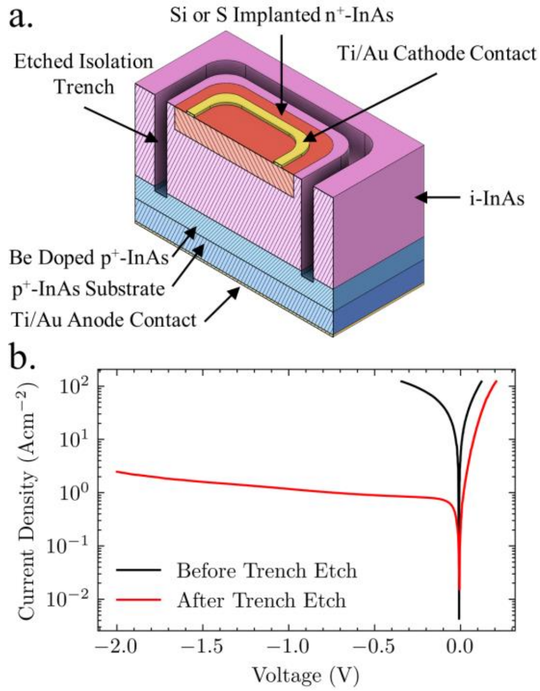

Fig. 7. Schematic of etched devices with isolation trenches (a). Current-voltage curves for 80×80 μm² devices with and without isolation trenches (b).

Although the isolation trench is effective in reducing the dark current, the deep etch will introduce a sidewall slope that necessitates a larger gap between planar pixels, which is undesirable for FPAs. Furthermore, when normalized to the implant 80×80 μm² implant area as opposed to the 90×90 μm² trench area, the dark current density is slightly higher than that of the mesa diodes. This suggests that this un-optimized trench etch has produced diodes that behave more similarly to mesa diodes with some possible surface leakage contribution. Therefore, we propose n on p planar InAs e-APDs utilizing a p-type isolation implant as illustrated in Fig. 8(a). The p-type isolation implant differs slightly from guard rings often used in planar diodes. Guard rings are typically (i) of the same dopant type as the implanted/diffused contact layer and (ii) their depths do not extend beyond the intrinsic layers. In contrast, to achieve the optimum field confinement and low dark current, the proposed isolation implant needs to be (i) p-type (i.e. opposite to the shallow n-implanted contact layer) and (ii) extend down to the epitaxially grown p-type layer. Note that the p-contact is placed onto the top side of the device to facilitate optical illumination from the substrate-side. Electric field simulations suggest successful confinement of the depletion region as shown in Fig. 8(b). Simulated dark current data for the proposed structure with and without isolation implants are compared in Fig. 8(c). The presence of the p-type isolation implant restores the dark current down to a level similar to that of our experimental results for planar diodes with etched isolation trenches. A similar approach for fabrication of InAs e-APDs was used to form lateral devices [33]. Although the p-type implant region did not extend to the p-type epitaxial layer, a fully rectifying diode with well-defined reverse dark current characteristics suggested that the depletion region was well-confined.

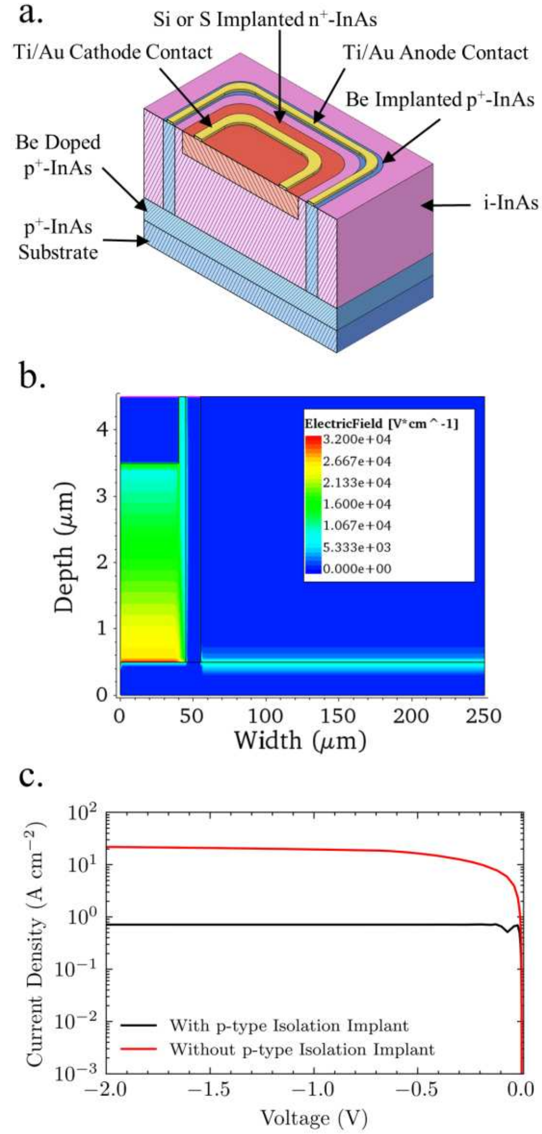

Fig. 8. Schematic of suggested planar n-i-p structure utilising an p-type isolation implant (a). Simulated electric field profile for an n-implanted InAs n-i-p diodes with n-type unintentional doping and an additional p-type isolation implant (b). Comparison of simulated dark currents for devices with and without p-type isolation implants (c).

Since the best quality InAs e-APDs are grown on InAs substrates, substrate removal is also required to facilitate optical illumination from the substrate-side. Substrate removal can be achieved using etch-stop or undercut layers at the bottom of the device structure. $AlAs_{0.16}Sb_{0.84}$ or lattice matched compositions of $Al_xIn_{1-x}As_ySb_{1-y}$ potential candidate for such layers with a wide range of selective etches reported [16]. Therefore, fabrication of planar n-i-p InAs diodes with the additional p-type isolation implant and a bottom etch stop layer will be the next development step to achieve InAs eAPDs that are fully compatible bump-bonding process.

IV. Conclusion

We have successfully fabricated mesa and planar n-i-p InAs diodes, using double S or Si ions implants and post-implant annealing. A post-implant annealing temperature of 500°C appears to optimize diode characteristics of reverse dark current and responsivity. Planar n-i-p diodes produced using S and Si implants alone, however, suffer from poor electrical isolation caused by i-InAs layers being n-type. To circumvent this significant issue, we demonstrated significantly improved diode characteristics by adding isolation trenches around the diodes or introducing a p-type isolation implant. Our findings will help in designing and producing planar n-i-p diodes that exhibit low reverse dark currents and are suitable for back-side illumination.

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