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Microwave Subsampler Using Cascaded Cold pHEMTs

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***Abstract*—We propose a concept using cascaded cold pHEMTs to implement a microwave sampler for subsampling use. The MMIC concept supports slewed control voltages as well as digital square-wave control signals. As such, the control voltages could be from oscillator sources, or from logic signals that have poor fidelity caused by PCB parasitics, etc. Sampling losses of circa 14 dB have been simulated in subsampling mode with RF input at 10th harmonic of the sampling frequency.**

I. INTRODUCTION

THE use of samplers in microwave and mmWave systems allows an incoming RF signal to be downconverted, through the sampling process, to a lower IF. This is an alternative strategy to RF mixing.

There is currently much research investigating new architectures for 6G [1], with new data converter topologies an important area of research for future SDR [2]. Subsampling is an important way to support digitization of RF signals, by using sampling images from data converters, benefiting from novel and fast sample and hold architectures [3], [4], [5], [6]. Sample and hold circuits are also useful as subsamplers on their own by offering an alternative to RF mixing, enabling new or simplified RF front-end architectures [7].

Sampling theoretically requires a digital control signal with a very short pulse duration, approximating an impulse. When sampler control signals exceed a few hundred MHz it becomes increasingly difficult to generate impulse-like signals, due to their implicit wide bandwidth requirements. This makes realizing a sampler for high GHz use, with GHz control signals, very hard. Traditional sampling techniques, such as diode samplers, often require significant drive current.

In this new work we propose a low power concept where two separate cold FET switches are cascaded, together forming a sampling gate to feed a sampling capacitor. By using two FETs we can drive each FET gate with a slower control signal and control the amount of joint on-time overlap of each switch. Hence the combined on-state for both switches can be controlled by the phase between the two controlling signals. This overlap can be used to approximate a short duration sampling pulse. The circuit concept is shown in Fig. 1.

This approach supports the use of simpler controlling waveforms that are not square, due to parasitic loading and PCB trace parasitics, from an FPGA or similar. The phasing between the two FETs is then controlled by timing within the FPGA, which can also compensate for signal delay on the PCB. Alternatively, the controlling signals can be from an oscillator, requiring just a trimmable delay between the signals to each gate to define a joint pHEMT on-time to charge the capacitor.

We have implemented the cascaded sampler concept in a GaAs MMIC using the UMS PH10 process, designed using Keysight ADS. The test chip attached to a PCB is shown in Fig. 2. The built MMIC test PCB is shown in Fig. 3.

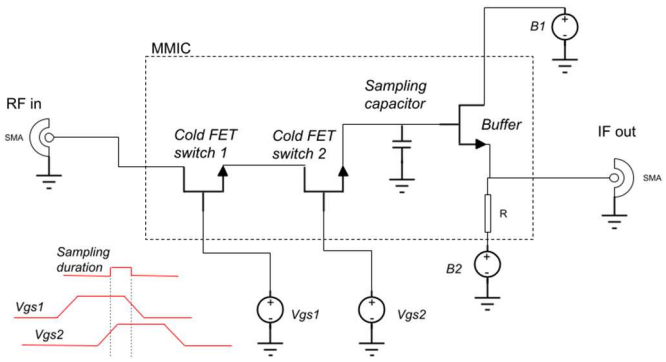

Fig. 1. Cascaded pHEMT sampler concept (2 pF on-chip sampling capacitor).

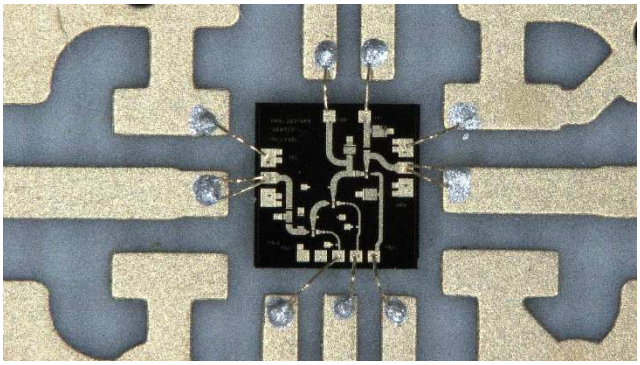

Fig. 2. Sampler MMIC bonded to the test PCB.

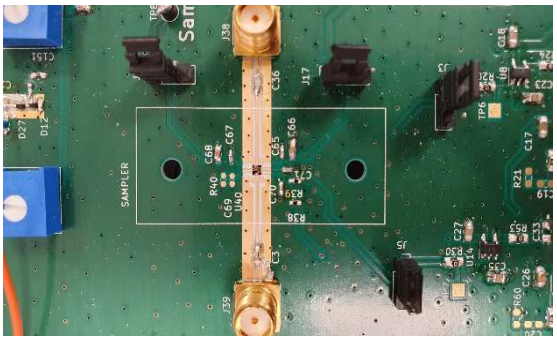

Fig. 3. Sampler test PCB (MMIC visible at centre) with SMA input & output ports.).

II. RESULTS

We have simulated and performed initial testing on the sampler MMIC at [8]. Table 1 presents ADS co-simulation results from the MMIC with various RF input frequencies and sampling frequencies (*Fs*). Table 2 presents initial lab measured results. The controlling signals were arranged by an FPGA to create an overlap between the switch pHEMT gates, when both would turn on and charge the on-chip sampling capacitor. An example control waveform from the FPGA at 300 MHz is shown in Fig. 4. Fig. 5 shows the output from MMIC simulation

when working as a conventional sampler, as reference. Voltage spikes due to capacitor charge / discharge at *Fs* are evident.

TABLE 1. ADS CO-SIMULATION RESULTS OF SAMPLER MMIC (ON-CHIP 2PF SAMPLING CAPACITOR).

Fs (MHz)	RF in (MHz)	Simulated sampling loss (dB)	Mode
100	10	7.1	Sampling
3000	10	8.9	Sampling
100	*Fs* + 10	8.0	Subsampling
35	10*Fs* + 10	14.2	Subsampling
100	10*Fs* + 10	14.4	Subsampling
300	10*Fs* + 10	20.9	Subsampling
3000	4*Fs* + 100	17.7	Subsampling
6000	3*Fs* + 100	22.9	Subsampling
3000	10*Fs* + 100	31.2	Subsampling
6000	5*Fs* + 100	22.8	Subsampling

TABLE 2. MEASURED RESULTS OF SAMPLER MMIC (FPGA CONTROLLED DELAY BETWEEN GATE CONTROL SIGNALS).

Fs (MHz)	RF in (MHz)	Measured sampling loss (dB)	Mode
35	10*Fs* + 10	20	Subsampling
35	20*Fs* + 10	25	Subsampling
35	30*Fs* + 10	30	Subsampling
100	*Fs* + 10	12	Subsampling
100	5*Fs* + 10	17	Subsampling
100	10*Fs* + 10	24	Subsampling
100	20*Fs* + 10	42	Subsampling
100	30*Fs* + 10	59	Subsampling
300	2*Fs* + 10	29	Subsampling
300	5*Fs* + 10	37	Subsampling
300	10*Fs* + 10	35	Subsampling

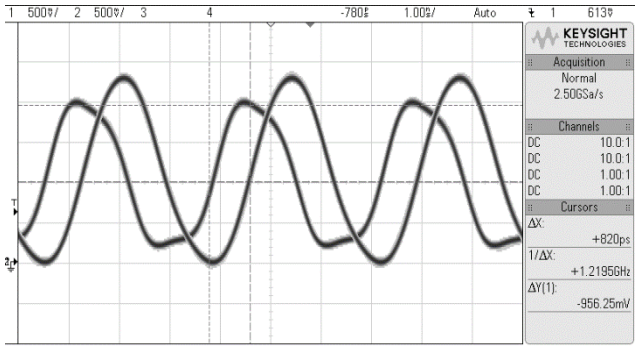

Fig. 4. Trial FPGA gate control waveforms for 300 MHz *Fs* signal with 90-degree overlap - arranged to create a 'both-on' period to charge the cap'.

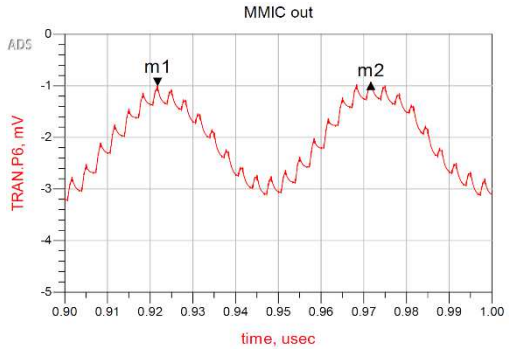

Fig. 5. Simulated MMIC sampled waveform showing basic sampler operation (*Fs* = 300 MHz, RF in = 20 MHz, external 18 pF cap. Sampling loss = 15 dB).

The simulation results predict acceptable operation of the MMIC as a subsampler with *Fs* up to 6 GHz and RF inputs up to 30 GHz. Some of the simulation results shows sampling loss comparable to conventional passive mixer conversion loss.

In lab tests the sampler chip was mounted on the test PCB and controlled by an Intel MAX 10 FPGA EK-10M50F484, clocking internally at 400 MHz. Table 2 reports the measured results when the MMIC is used as a sampler, or subsampler up to the 30th harmonic of *Fs* as the RF input Nyquist zone. At 35 MHz *Fs* the FPGA control signals have good approximation to square waves. When a 100 MHz *Fs* is used, the gate control voltages have poorer fidelity and approximate sinusoids, as expected. However, in several scenarios, subsampling use up to at least the 5th or perhaps the 10th sampling harmonic appears viable.

The measured results are notably worse at 300 MHz and this is likely due to sub-optimal gate timings in the current system at this *Fs*. However, subsampling an input at 3 GHz with a 300 MHz *Fs* is demonstrated, with loss.

Some measured results are circa 10 dB worse than simulation. This could be due to additional losses on the PCB, control waveform issues, or MMIC input matching issues on the PCB. MMIC input return loss (average of 20 dies) was 14 dB at 5 GHz, when measured on the dies. The MMIC buffer draws 2.8 mA from 3V, though this could be reduced.

III. SUMMARY

We present a concept cascaded FET switch as a subsampler circuit, with initial simulation and test results reported. Initial results confirm operation using non-rectangular signals (such as an artefact of parasitics on digital control lines). Nyquist zones of up to 10x*Fs* seem viable, depending on acceptable loss. RF sampling of a 30 GHz RF signal with a 6 GHz *Fs* also seems possible. More testing is needed to find the minimum acceptable waveform shape and optimum delay between sampling control lines. The off-chip sampling hold capacitor value can also be explored.

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