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CMOS-Compatible Short-Wave Infrared Linear Arrays of Ge-on-Si Avalanche Photodiodes

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Germanium-containing short-wave infrared (SWIR) avalanche photodiode (APD) arrays on silicon platforms have the potential for monolithic integration into complementary metal-oxide-semiconductor (CMOS) integrated circuits, making them mass-manufacturable, high-performance, arrayed optical detectors operating at wavelengths beyond the silicon cut-off wavelength. Here, the first high-performance, surface-illuminated, 10-pixel linear array of pseudo-planar geometry germanium-on-silicon (Ge-on-Si) APDs operating at 1550 nm wavelength and at temperatures up to 378 K are demonstrated. At room temperature, the dark current, avalanche gain, responsivity, and avalanche breakdown of the devices show good uniformity. Array A exhibits a mean dark current density of 198 $\pm$ 62 mA cm^{-2} at 90% of the breakdown voltage. The excess noise factor is less than half that of InP-based SWIR APD arrays, which allows Ge-on-Si devices to operate at a higher avalanche gain. A responsivity of 8.2 A W^{-1} at a gain of 20 and excess noise of 3.3 is achieved when illuminated with 1550 nm wavelength light. The detector array also demonstrates stable performance at 378 K with a maximum avalanche gain of 24. This device architecture will be applicable for the design of large-scale APD arrays on Si platforms for SWIR detection which can be used in imaging, sensing, and optical communication applications.

1. Introduction

Avalanche photodiode (APD) arrays have been used to detect weak optical signals in a wide range of applications; for example, in positron emission tomography,[1] 3D laser radar and 3D flash light detection and ranging (LiDAR),[2,3] free space optical communication,[4] and medical applications.[5] In comparison to conventional photodiodes, the signal-to-noise ratio (SNR) in an APD-based optical receiver can be improved by the internal multiplication gain when the dominant noise is produced by the preamplifier, as expressed by

$$\mathrm{SNR} = \frac{I_{\mathrm{ph}}}{2q(I_{\mathrm{ph}} + I_{\mathrm{d}})F(M)B + (u^2/M^2)} \quad (1)$$

where q is the electron charge, I_{ph} is the photocurrent, I_{d} is the dark current, F is the excess noise factor, B is the bandwidth, and u^2 is the root-mean-square noise of the amplifier circuit. The preamplifier noise current is reduced by the square of the avalanche multiplication gain, M^2, leading to a significantly increased SNR, provided that F increases slowly with M. Silicon (Si) is one of the semiconductor materials which has a small ratio between the hole (β) and electron (α) ionization coefficients ($k = \beta/\alpha$ for avalanche initiated by electrons) and can produce low-noise APDs, as described by McIntyre.[6]

The significant increase in demand for 3D imaging and free space optical communication in the short-wave infrared (SWIR) region necessitates surface-illuminated APD arrays. Operating in the SWIR spectral region reduces atmospheric attenuation and solar background and increases eye-safety thresholds compared

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to systems using visible and near-infrared light. Currently, InGaAs/InP APD arrays are commercially available[7] and InGaAs/InAlAs APD arrays have been reported and demonstrated in free space-based applications at 1550 nm wavelength and room temperature.[4,8] 1×128 pixel linear arrays of InAs planar APDs have also been demonstrated at 1550 nm wavelength and room temperature,[9] and HgCdTe APD arrays show extremely high performance in the detection of infrared light.[10] However, these devices still face the drawbacks of high cost and challenges in compatibility with CMOS integration.

Si has been widely used in the design of high-performance megapixel APD arrays which can be inexpensively manufactured by foundries and integrated with CMOS electronics and/or Si photonics. The bandgap of Si, however, prevents such devices from operating in the SWIR region. Adding Ge as an absorber layer in a separate absorption and multiplication APD configuration has been shown to extend the operational wavelength out to SWIR wavelengths and provides a low-cost, easily integrated alternative at the strategically important wavelengths of 1310 and 1550 nm.[11–14] Over the last two decades, the challenges in the Ge/Si material system, such as 1) the 4.2% lattice mismatch leading to a high threading dislocation density; 2) detector sensitivity and noise; and 3) device robustness, have been tackled, while there has been progress on expanding individual Ge-on-Si APD detectors into arrays. In 2019, Li et al. reported Ge-on-Si APD arrays of up to 10×10 pixels with a responsivity of 3.3 A W^{-1} at 90% of the breakdown voltage and 1550 nm wavelength.[15] Liu et al. presented a cascaded Ge-on-Si APD array with sub-nA dark currents[16] and a three-electrode Ge-on-Si APD array operating in SWIR.[17] Ge-on-Si APDs using a pseudoplanar design were recently developed and this geometry exhibits high single-photon detection efficiency when operating in the Geiger mode at temperatures of $\leq$175 K and at a wavelength of 1310 nm.[18–20] The following development focuses on improving device sensitivity at longer wavelengths by building on recently published work where we demonstrated a high-performance single-pixel Ge-on-Si APD at 1550 nm wavelength.[21] Up until now, it was unclear whether this recently demonstrated pseudoplanar structure and its fabrication techniques are robust and reliable enough to allow the realization of uniform high-performance SWIR detector arrays, which could be deployed in emerging applications such as LiDAR systems for autonomous driving.

In this work, we demonstrate the first high avalanche gain and low excess noise Ge-on-Si APD arrays operating at 1550 nm wavelength. Two arrays have been fabricated and investigated, and device characterizations at room temperature, including dark currents, photomultiplication, responsivity, and avalanche breakdown, indicate good uniformity across the arrays. The APD arrays also demonstrate robust performance at an increased operating temperature of 378 K and demonstrate a temperature dependence of the breakdown voltage, C_{bd}, of $\approx$57 mV K^{-1}. The difference in breakdown voltage, V_{bd}, between the two arrays is less than 1 V ($\leq$1.8% of V_{bd}), suggesting high repeatability in the material growth and device fabrication. **Table 1** shows a comparison of state-of-the-art SWIR APD arrays operating at room temperature and 1550 nm wavelength. Our APD array exhibits higher dark currents than some commercially available Si APD arrays[22] and InGaAs/InP APD arrays.[7] Similar dark currents, however, have been reported for another Ge-on-Si APD array[15] and our thicker structure design provides the advantages of high responsivity, high avalanche gain, and low excess noise.

2. Device Fabrication

The wafer used in this work was grown by IQE Silicon UK using an ASM Epsilon 2000E reduced pressure chemical vapor deposition system. Initially, a 1.5 μm-thick i-Si layer, acting as the multiplication region, was grown over an arsenic-doped 150 mm silicon substrate. Subsequently, the charge-sheet regions were defined by photolithography with a diameter of 50 μm at a 100 μm pitch and ion beam implanted with boron at a dose of 3×10^{12} cm^{-2}. After stripping the resist, a 2 μm-thick i-Ge layer acting as the SWIR photon absorber was epitaxially grown over the i-Si layer, followed by a 50 nm-thick heavily boron doped Ge layer to enable the top contact. Devices were fabricated in the James Watt Nanofabrication Centre using a combination of electron-beam lithography and photolithography. Initially a p^{++}-Ge layer was mesa etched using a fluorine-based reactive-ion etching (RIE) process to define an isolated layer for the Ohmic contacts. Then, 250 nm-wide trenches with a depth of 2.5 μm were etched using an inductively coupled plasma–RIE process at a distance of 10 μm from the edge of the implanted charge sheet, to facilitate lateral pixel isolation and reduce the likelihood of electrical crosstalk. The trenches were then thermally oxidized at 550 °C

Table 1. Comparison of proposed and reported SWIR APD arrays operated at room temperature.

Device	Platform	Dark current [A]	Responsivity at $\lambda = 1550$ nm [A W^{-1}]	Excess noise factor	C_{bd} [mV K^{-1}]	Bandwidth [GHz]
Si[22]	Si	4 nA (90% V_{bd})	N/A	N/A	440	N/A
Ge-on-Si[15]	Si	7 μA (90% V_{bd})	3.3 (90% V_{bd})	N/A	29	$\geq$0.7
Three-electrode Ge-on-Si[17]	Si	N/A	1.2 ($M = 7$)	N/A	N/A	0.043
InGaAs/InP[7]	InP	2 nA (90% V_{bd})	10.1 (90% V_{bd})	3.9 ($M = 10$) 7.9 ($M = 20$)	34	5
InGaAs/InAlAs[4]	InP	15 nA (90% V_{bd})	N/A	3.6 ($M = 10$) 6.6 ($M = 20$)	N/A	1.8
InAs[9]	InAs	0.1 mA (−0.5 V)	4.4 ($M = 8$)	1.6	N/A	N/A
This work	Si	4 μA (90% V_{bd})	4.6 (90% V_{bd}) 8.2 ($M = 20$)	2.4 ($M = 10$) 3.3 ($M = 20$)	57	N/A

for 30 min in O_2, creating a GeO_x layer, and then filled with Si_xN_y by plasma-enhanced chemical vapor deposition (PECVD) so that the top contact and bond-pad could be realized. The devices were annealed in forming gas (5% H_2 in N_2) to remove any trap charges in the defined passivation, followed by a Ni–Pd deposition (for the Ohmic contacts) onto the heavily doped Ge layer and Al was deposited for the bond-pads. **Figure 1**a shows the key stages of device processing. Two 1×10 arrays of devices, called Array A and Array B, were fabricated to investigate device uniformity. In array A, the individual devices are denoted as 'A1', 'A2', ..., 'A10' and similarly with Array B as 'B1', 'B2',...,'B10'. An optical image of a Ge-on-Si APD array section with a schematic diagram of a single device is shown in Figure 1b, and Figure 1c shows the scanning electron microscope (SEM) image of the device cross-section.

As described previously, and as shown in Figure 1b, relatively narrow trenches were used such that they could be closed over with a Si_xN_y layer to effectively planarize the device. The presence of GeO_x and SiO_2 passivation on the trench sidewalls was investigated to understand the relatively high leakage currents observed (Table 1). A thin transmission electron microscopy (TEM) specimen was prepared by a focused ion-beam (FIB) lift-out procedure, using a Zeiss Auriga Ga FIB-SEM. The specimen was mounted to a Cu half grid. Scanning TEM (STEM) and energy-dispersive ray spectroscopy (EDS) were performed on this specimen using a Thermofisher Spectra 300, operated at 300 kV, equipped with a Super-X EDS detection system. **Figure 2**a shows a high-angle-annular dark-field (HAADF) STEM image of the device trench region, along with elemental mapping of Si, Ge, N, O, Cu, and Pt in the area. TEM specimen preparation by the FIB causes redeposition of Cu from the grid and Pt from the capping layer. Oxygen mapping indicates that Cu fine particles have been partially oxidized as well. These elements are not likely to be present in the original specimen. The composition profile of areas annotated by the red boxes in HAADF–STEM image of Figure 2a in directions numbered by 1–3 are shown in Figure 2b–d, respectively. Since Cu and Pt originate from the specimen preparation, they have been removed from composition profiles presented in Figure 2b–d, and the compositions renormalized to 100%. Figure 2b, a composition profile over the Ge–Si interface, shows low but detectable concentrations of Si in the Ge layer. No clear Ge peaks were observed in the Si layer and the width of the intermixing region is estimated to be around 7.5 nm. Profile 2 (Figure 2c) passes from the Si epitaxial layer to the trench. While a small amount of oxygen is present near the Si interface, this appears to overlap with the Si_xN_y layer highlighting that the Si was not thermally oxidized at the low growth temperatures used for thermally oxidizing Ge (550 °C). In contrast, Profile 3 (Figure 2d), which passes

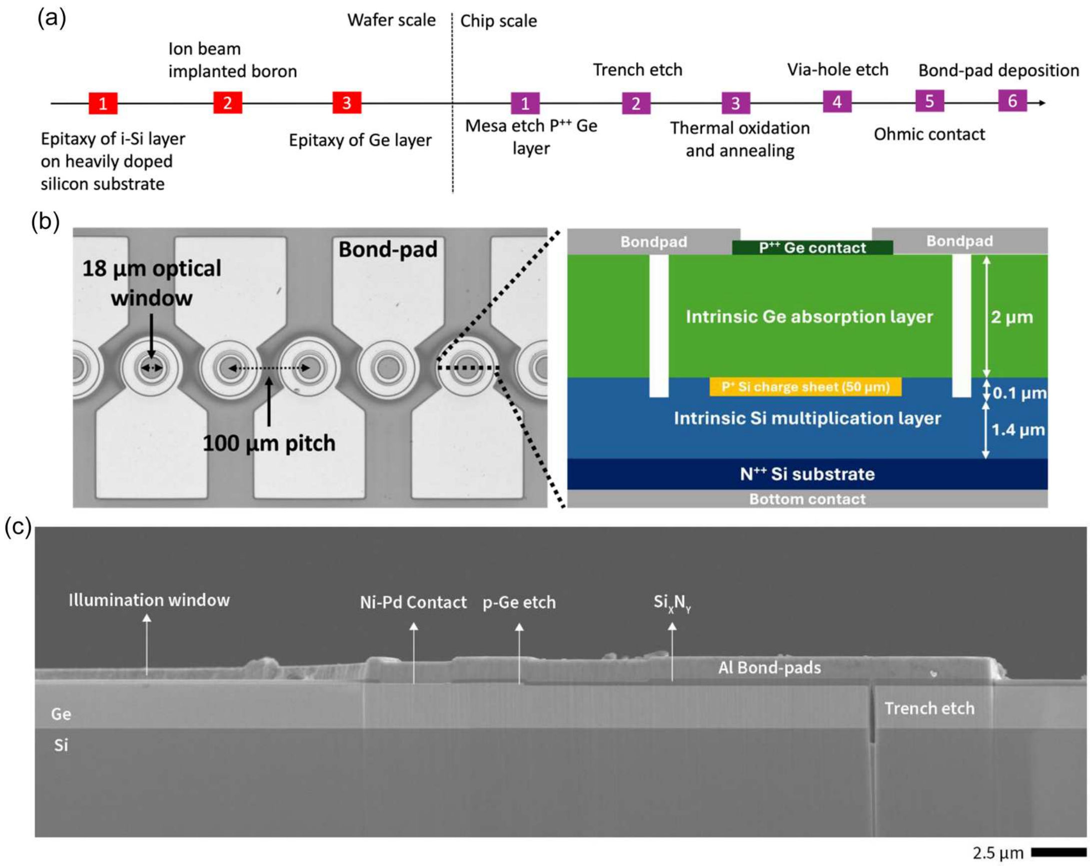

Figure 1. a) Flow diagram showing the different stages of device processing. b) An optical image of a Ge-on-Si APD array section (left) with a schematic diagram of a single device (right). c) Cross-section SEM image of the single-pixel APD device. The top electrode is in contact with Al bond-pads, and the bottom electrode is not shown.

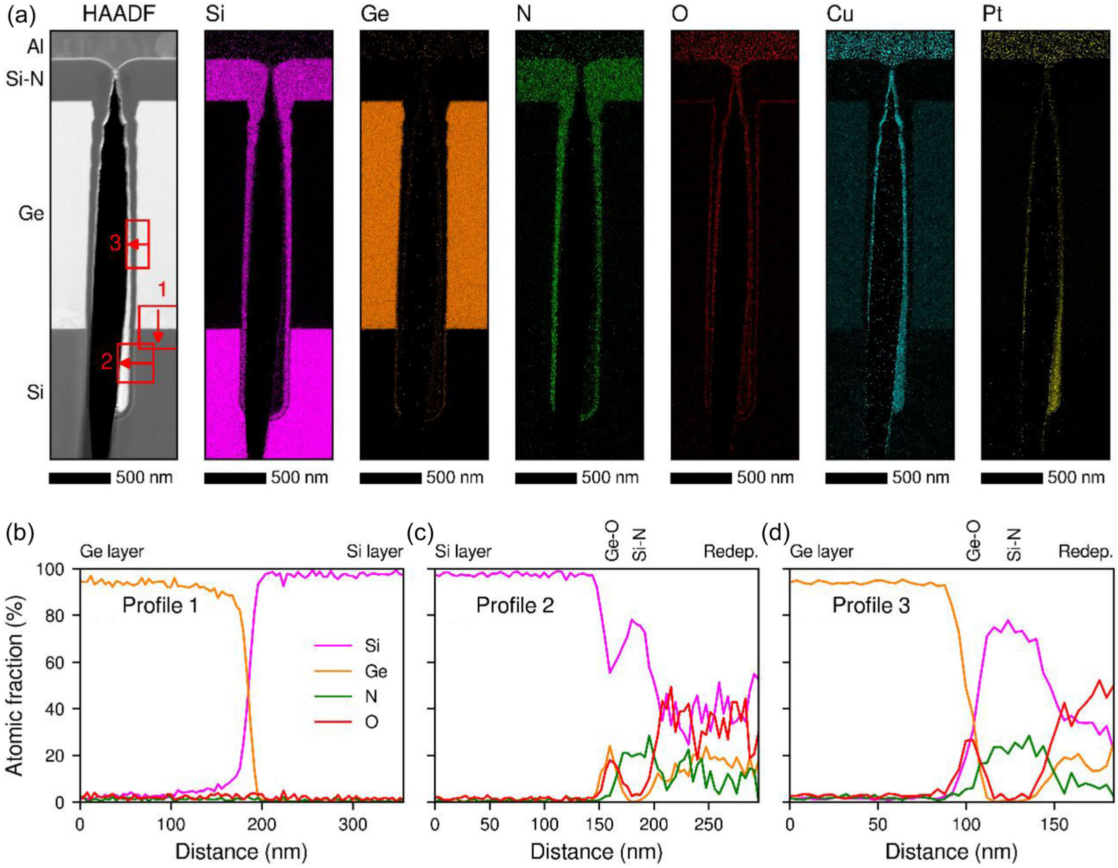

Figure 2. Microscopy characterization of the trench region: a) HAADF–STEM image of the trench, showing Si, Ge, silicon nitride, and Al layers, along with EDS elemental mapping of Si, Ge, N, O, Cu, and Pt; b–d) Composition profiles respectively taken from the red regions-of-interest in directions 1, 2, and 3, annotated in Figure 2a by the red boxes. Note that Cu and Pt originate from the FIB sample preparation by milling of Pt deposition and Cu grid and they do not exist in the original sample. Therefore, Cu and Pt have been removed from composition profiles, and the data is renormalized to 100% atomic fraction.

from the Ge layer to the trench, clearly shows thermal oxidation of the semiconductor layer with a GeO_x layer of ≈25 nm prior to ≈50 nm of Si_xN_y, highlighting that the thermal oxide process can passivate Ge down the trench. It is worth noting, however, that the exposed Si sidewall with only PECVD Si_xN_y passivation could have significant density of interface traps and could contribute to sidewall leakage. In future, passivation strategies that are known to effectively passivate Ge and Si will be employed such as a-Si or Al_2O_3.

3. Results and Discussion

3.1. Room-Temperature Characterization

The dark current as a function of bias voltage was measured at room temperature using a Keithley 2450 Source Measure Unit and is shown in **Figure 3**a,b. Under applied forward bias (dashed lines), the diode ideality factor value lies between 1 and 1.2 and the diode series resistance lies between 1 and 2 kΩ. These values were extracted by fitting the forward current using the diode equation. Under applied reverse bias all devices (solid lines) demonstrate clear avalanche breakdown. The insets in Figure 3a,b show the V_{bd} distribution in Array A and Array B. The V_{bd} (determined when the dark current has reached 100 μA) is 54 ± 1.1 V for Array A and 54 ± 0.4 V for Array B at room temperature. Variation in V_{bd} between the two individual arrays is less than 1 V (≤1.8% V_{bd}). Figure 3c,d shows the comparison of dark current density at a reverse bias of 25 V and at 90% V_{bd} for Array A and Array B, respectively. For Array A, the mean dark current density at a reverse bias of 25 V is 17.3 ± 0.7 mA cm^{-2} and at 90% V_{bd} it is 198 ± 62 mA cm^{-1}. For array B, those values are 21.2 ± 0.7 and 234 ± 133 mA cm^{-2}, respectively. The device 'A7' has the highest dark current density with 356 mA cm^{-2} in Array A and device 'B3' shows the highest dark current density at 613 mA cm^{-2} in Array B, at 90% V_{bd}. It is notable that our dark current is ≈× 1000 higher than commercially available InP-based SWIR APD arrays.[7] This is likely due to the threading dislocations at the Ge/Si interface and leakage from the device's mesa sidewall, potentially including the PECVD-passivated Si region. A previous study addressed this issue using selective area growth of the Ge layer on Si resulting in a lower threading dislocation density which was, in turn, shown to lead to a lower dark current.[23] Various surface passivation

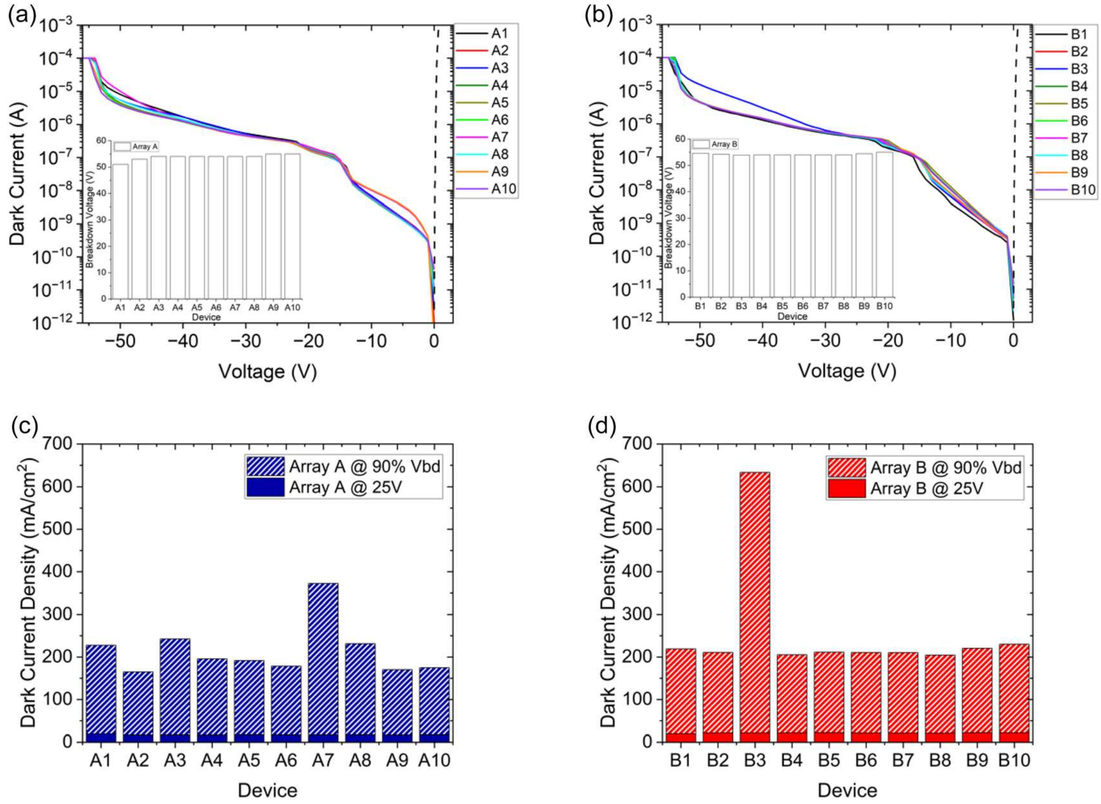

Figure 3. The dark current at room temperature for a) Array A and b) Array B. The insets show the V_{bd} distribution at room temperature. Dark current density distribution for c) Array A and d) Array B at a bias of 25 V and at 90% V_{bd}.

methods for reducing surface leakage in Ge-based devices have also been experimentally investigated.[24,25] Further optimizations to our device structure (such as applying guard rings) and fabrication process (e.g., improving surface passivation) are required to reduce the dark current in order to be comparable to that of InP-based devices.

The photocurrent under applied reverse bias was characterized using a pulsed, supercontinuum laser (NKT Supercontinuum white light laser) with an acousto-optic tunable filter operating at a wavelength of 1550 nm and a phase-sensitive measurement technique (Stanford Research Systems SR830 lock-in amplifier) to remove the DC leakage current. 20 individual pixels were measured, and for each, we repeated the photocurrent measurement at different laser powers to ensure the repeatability of the photomultiplication results. An example of photocurrent results at room temperature is shown in the insets in **Figure 4**a,b. The laser power was constantly monitored using a calibrated Ge photodiode (Newport 818-IR). A reference p–i–n diode with a Ge thickness of 2 μm on a Si substrate has also been measured under the same conditions to identify the primary responsivity (i.e., $M = 1$). The responsivity determined in this reference diode was 0.41 A W^{-1} at 1550 nm wavelength. This primary responsivity is higher than in previous work due to the increased thickness of the Ge absorption layer and could be further improved using methods such as a photon trapping design, as implemented by Cansizoglu et al.[26] although simulations show that care is required when implanting etched photonic crystals in the pseudoplanar geometry.[27] The multiplication gain as a function of reverse bias was calculated using the following relationship: (responsivity at multiple biases)/(responsivity from the reference diode) and is shown in Figure 4a,b for Array A and Array B, respectively. The distribution of reverse bias at a gain of 10, 20, 30, and 40 is presented in Figure 4c,d for Array A and Array B, respectively. The mean values of reverse bias for Array A are 49.36 ± 0.18, 51.87 ± 0.16, 52.65 ± 0.19, and 53.20 ± 0.16 V at M of 10, 20, 30, and 40 and those values for Array B are 49.26 ± 0.35, 51.78 ± 0.26, 52.66 ± 0.27, and 53.32 ± 0.36 V at M of 10, 20, 30, and 40, respectively. Both arrays show a high uniformity of avalanche gain under a given reverse bias. We found that the devices at the array edge require a slightly higher bias to achieve the same gain compared to the devices at the array center. We limited the highest applied reverse bias to protect the devices for measurements at higher temperatures. The highest avalanche gain observed at room temperature was 104 (see Figure 6b). Excess noise measurements were also performed under SWIR illumination and the results of Array A shown in Figure 4e are in good agreement with those presented previously in Ref. [21]. This is expected considering the device structure is identical. Figure 4f shows the measured responsivity versus wavelength of Array A under reverse bias of 16 and 52.5 V. This new array demonstrates a good responsivity beyond a wavelength of 1650 nm at high reverse bias, opening up more application areas, such as the detection of methane. Due to a large capacitance of this design, the device is unsuitable for high-speed APD applications, and the simulation estimates a gain bandwidth

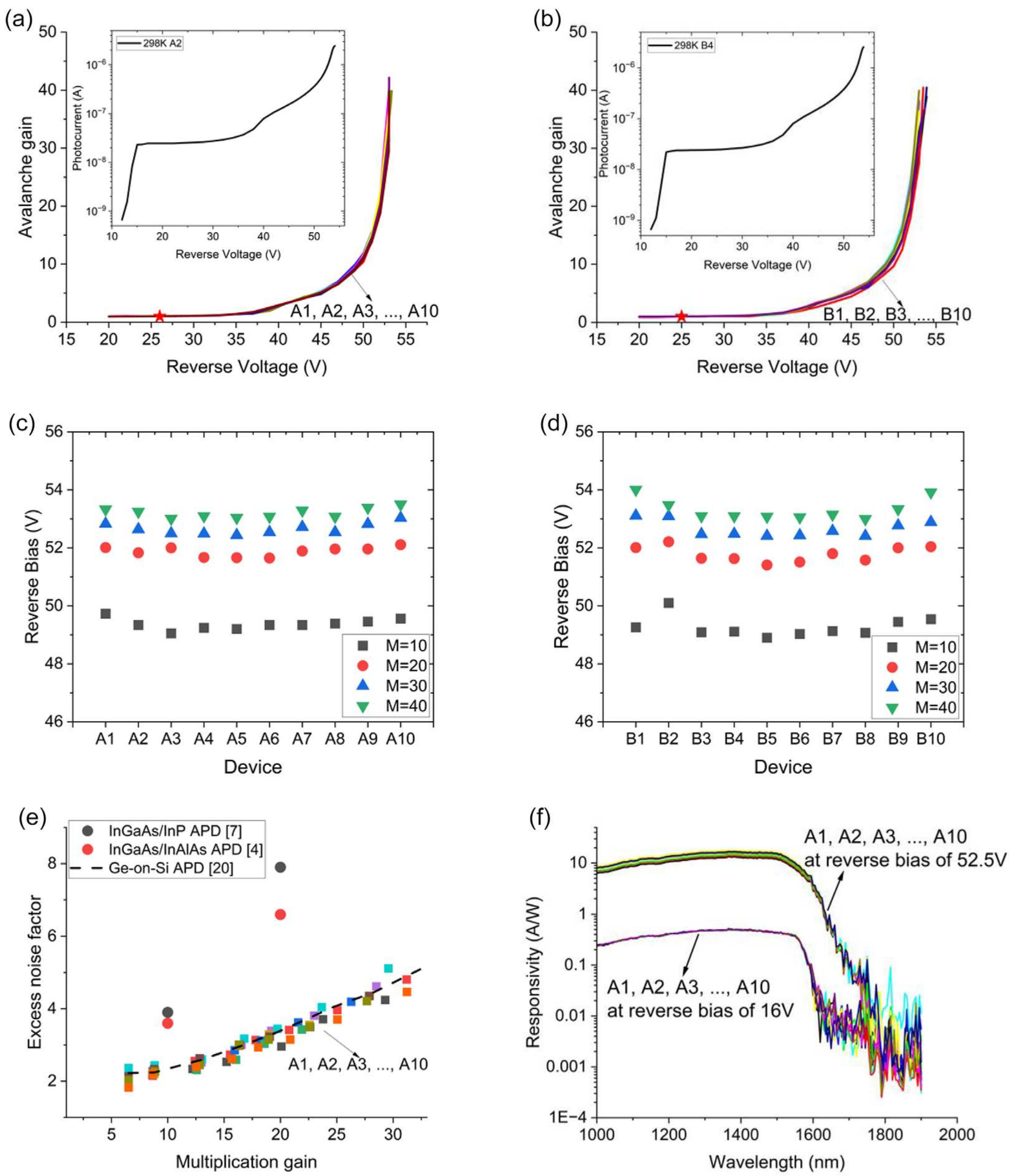

Figure 4. The avalanche gain as a function of the reverse bias under illumination of 1550 nm wavelength laser light for a) Array A and b) Array B. The inset shows an example of the raw photocurrent data at 1550 nm wavelength and the red star indicates the primary responsivity of 0.41 A W^{-1} measured from a Ge reference diode. The reverse bias for each pixel at a gain of 10, 20, 30, and 40 is shown in c) for Array A and in d) for Array B. e) A plot of the excess noise factor at room temperature for Array A. The black circles denote values from an InGaAs/InP APD array,[7] and the red circles denote values from an InGaAs/InAlAs APD array.[4] The dashed line indicates the excess noise factors from recently demonstrated single-pixel Ge-on-Si APDs.[21] f) The responsivity of Array A under a reverse bias of 16 and 52.5 V.

product of 90 GHz at a gain of 25.[28] More details of the simulation assumptions can be found in Ref. [29].

3.2. High-Temperature Characterization

The array stability is assessed by confirming consistency in the dark current and photomultiplication in the pixels in each array above room temperature. A thermistor was used to monitor the real-time device temperature, and three random devices from each array were tested at temperatures between 298 and 378 K.

Figure 5a,b shows the dark current versus bias in devices ‘A2’ and ‘B4’. The device series resistance does not change significantly but the device dark current increases in magnitude more than 31× at a reverse bias of 25 V and 22× at a bias of 90% V_{bd}, as the device is heated from 298 to 378 K. In order to understand the nature of the dark current, the activation energy, E_a, at reverse biases of 10, 20, 30, and 40 V, has been extracted by fitting the Arrhenius equation as shown in Figure 5c. The devices in both arrays show similar E_a’s at various reverse biases. We found that at low reverse bias, the E_a is close to half of the bandgap

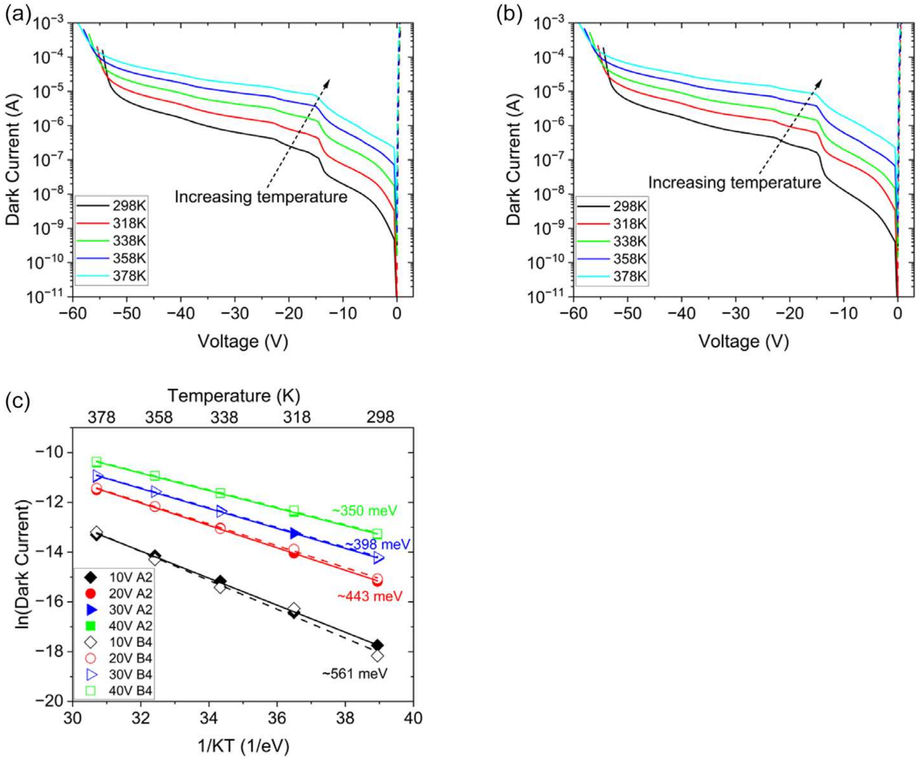

Figure 5. Dark currents at different temperatures for a) 'A2' and b) 'B4'. c) Activation energy at different biases for 'A2' (closed symbols) and 'B4' (open symbols) extracted through fitting.

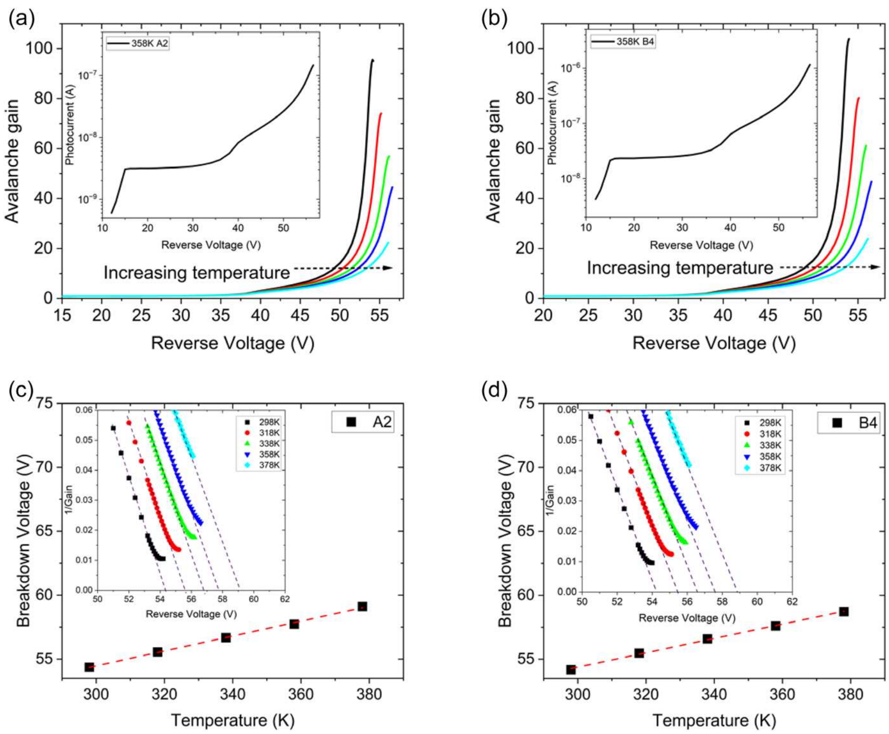

Figure 6. Avalanche gain at temperatures of 298 K (black line), 318 K (red line), 338 K (green line), 358 K (blue line), and 378 K (cyan line) and under illumination of 1550 nm laser light for a) pixel 'A2' and b) 'B4'. The inset shows the photocurrent raw data at 1550 nm wavelength illumination and a temperature of 358 K. The C_{bd} is shown in c) for 'A2' and in d) for 'B4'. The insets in (c) and (d) show the extraction of V_{bd} by extrapolation at different temperatures.

energy of Si ($E_g = 1.114$ eV at 292 K[30]). It then gradually reduces to half of the bandgap energy of Ge ($E_g = 0.664$ eV at 291 K[30]) at a bias close to V_{bd}, suggesting that the generation–recombination center in the Ge layer is the dominant contributor to the dark current under very high reverse biases. We observed this behavior in other pixels tested in both arrays. Very recently, new types of single pixel Ge-on-Si APDs with sub-nA dark currents at room temperature have been achieved using a screening layer[12] and a buffer layer.[31] These studies showed E_a values greater than half of the bandgap energy of Si at very high reverse bias, suggesting that the leakage current is dominated by the Si layer. We also found that the E_a values extracted in this study differ from the values determined in the previous study of the devices that observed <100 meV energies at temperatures below 175 K.[32] Previous studies in III–V-based APDs[33] and GeSn photodetectors[34,35] also reported a decreasing E_a when the devices were cooled. It is likely that trap-assisted tunneling dominates the leakage current when operating at low temperatures.

The avalanche gain versus reverse bias at operating temperatures between 298 and 378 K at 20 K intervals is presented in **Figure 6**a,b for 'A2' and 'B4,' respectively. An example of the photocurrent under illumination of 1550 nm wavelength laser light and at a temperature of 358 K is shown in the insets of Figure 6a–b. The avalanche gain was calculated using the same method described previously. The device was operated at as close to V_{bd} as possible to extract the V_{bd} value at different temperatures. Due to the increase in dark current with increasing temperature, the highest reverse bias that could be applied was limited and the highest avalanche gain value of 24 was measured at a temperature of 378 K. At a given reverse bias, the gain reduces with increasing temperature. Values of C_{bd} and a linear fit are shown in Figure 6c,d, and the inset shows how the V_{bd} are determined by extrapolation of the 1/(multiplication gain) data at various operating temperatures. The V_{bd} determined using this method, with illumination in the center of the device, is consistent with the V_{bd} observed in the dark *I*–*V*. The consistency between these methods is confirmation that edge breakdown is not present in these devices. The C_{bd} is determined to be 58.4 mV K^{-1} in 'A2' and 56.1 mV K^{-1} in 'B4'. Due to a thicker structure design, our C_{bd} values are higher than what was found by Li et al. who reported a C_{bd} of 30 mV K^{-1} in a Ge-on-Si APD array[15] and an InGaAs/InP APD array with a C_{bd} value of 34 mV K^{-1}.[7]

4. Conclusion

We fabricated and characterized two surface-illuminated pseudo-planar Ge-on-Si SWIR APD arrays of 1×10 pixels. The uniformity between pixels was demonstrated by comparisons of the device dark currents, photomultiplication parameters under illumination of 1550 nm wavelength laser light, responsivity, as well as their breakdown voltages. We also performed tests at high temperatures, which demonstrated stable pixel performance up to temperatures of 378 K. These results suggest that the structure and fabrication techniques can produce a uniform high-performance SWIR APD array that could be deployed in emerging applications such as flash-LiDAR or in free-space optical communications. Although the demonstrated arrays have a higher leakage current than InP-based APD arrays that are currently being used in the majority of SWIR applications, this new type of SWIR APD array is fully compatible with CMOS foundry processing and can potentially be integrated with Si-based integrated circuits, making it an ideal candidate for easy implementation and low-cost production. Further studies to improve the performance of the demonstrated detector arrays include 1) investigation of the reduction in dark noise through the reduction of the electric field in the Ge absorption region; investigation of the surface passivation and reduction of the device active area; 2) production of a large-scale Ge-on-Si APD array integrated with CMOS circuitry; and 3) implementation of a thick $Ge_{1-x}Sn_x$ layer to push absorption to wavelengths beyond 2 μm to further expand potential application areas.

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Conflict of Interest

The authors declare no conflict of interest.

Data Availability Statement

The data that support the findings of this study are available from the corresponding author upon reasonable request.

Keywords

arrays, avalanche photodiodes, Ge-on-Si, photodetectors, short-wave infrared

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