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Discrete Tuned Millimeter Wave SIW Resonators in GaAs and on PCB

Edward A. Ball
Department of Electronic and Electrical Engineering
The University of Sheffield
Sheffield, United Kingdom
e.a.ball@sheffield.ac.uk

Sumin David Joseph
Department of Electronic and Electrical Engineering
The University of Sheffield
Sheffield, United Kingdom
s.d.joseph@sheffield.ac.uk

***Abstract*—A concept to digitally tune Substrate Integrated Waveguide resonators using FET switches is presented. Simulation results are provided for designs at 73 GHz on GaAs. Also, simulation and measured results are provided at 23 GHz for a PCB prototype. The 73 GHz design has a tuning range of 580 MHz and an average unloaded Q of 121. The 23 GHz PCB prototype has a measured tuning range of 260 MHz and average unloaded Q of 72.9.**

Keywords—substrate integrated waveguide, millimeter wave resonators, tunable filters, millimeter wave oscillators, FETs.

I. Introduction

Resonators are a critical aspect in all oscillator designs. There is a perpetual need to find new high Q resonators that are tunable, but balance tunability and phase noise requirements. As the operating frequency increases it becomes steadily harder to make high Q resonators, due to increasing losses. On chip resonators become essential for oscillators above X band and into millimeter wave (mmWave) bands, due to the coupling loss for signals transitioning off chip to a separate resonator. Matching considerations due to bond wire impedances also becomes problematic.

One class of resonator that has shown good Q and is easy to design is the Substrate Integrated Waveguide (SIW) resonator, which is based on waveguide concepts. The SIW has been demonstrated for use in microwave oscillators [1]. The conventional SIW is a fixed frequency resonator, but methods have been explored to electrically tune it using varactors [2]. Conventional SIW designs have used rectangular cavities, but circular cavities have also been investigated at low mmWave [3]. The SIW is inherently a narrow band device, but some works have demonstrated that wide tuning ranges are possible, though requiring varactors placed in the centre of the SIW on special coupling structures [4].

GaAs MMICs are commonly used at mmWave frequencies and so on-chip oscillators remain an important research topic. However, there has been little research into tunable or fixed SIW resonators on GaAs, though in related topics a W band filter was presented in [5].

In this work we present initial design, simulation results and prototype tests of a digitally tuned SIW using 'cold FET' switches. This allows the resonator to be tuned digitally, in quantised frequency steps, without the need for varactors and associated analogue control voltages. We present designs and test results at 23 GHz and 73 GHz.

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II. SIW Design

The design of a simple SIW can start using the equations based on a TE101 mode waveguide. The key design equations for SIW resonance in a defined structure size are given by (1) – (3) [1].

$$F_{TE101} = \frac{C_0}{2\sqrt{\epsilon_r}}\sqrt{\left[\frac{1}{W_{eff}}\right]^2 + \left[\frac{1}{L_{eff}}\right]^2} \quad (1)$$

In (1) C_0 is the speed of light in vacuum and ε_r is the relative permittivity of the substrate material. The relationship between electrical (effective) size and physical size is given by (2) - (3), where W is the physical width, L is the physical length of the SIW cavity, D is the via diameter and S is the via spacing (centre-centre pitch). The perimeter vias should be packed closely, to form a wall and so forming the waveguide.

$$W_{eff} = W - \frac{D^2}{0.95S} \quad (2)$$

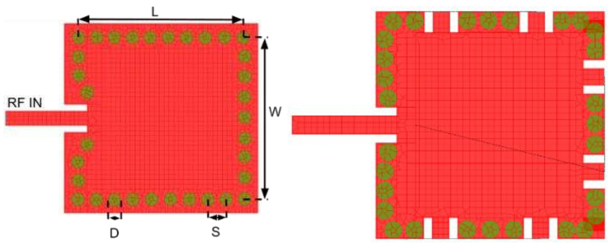
$$L_{eff} = L - \frac{D^2}{0.95S} \quad (3)$$

There are several techniques for coupling signals into a SIW, in this paper we couple in through a simple microstrip line. The initial example SIW concept is shown in Fig.1 (a).

A. Cold FET Switched SIW Design

In our investigation we have used six Tuning Access Ports (TAPs) equally spaced around the SIW perimeter, also removing the grounding vias at these points. An example showing the TAPs with a short length of inset line is shown in Fig. 1 (b).

Rather than use a varactor to tune the SIW we have investigated using a 'cold FET' switch to provide quantised tuning. In a cold FET switch, the drain and source are biased at 0 V and only V_{gs} is varied, usually between two states. Hence V_{gs} effectively defines an ON impedance and an OFF impedance between the drain and source corresponding to the applied gate control voltage.



(a) (b)

Fig. 1. Layout of a simple SIW: a) key dimensions, b) vias removed where TAPs added.

If the FET drain is then connected to the TAP of the SIW, it becomes possible to apply a set of binary controlled reactances to the TAPs, which leads to a tunability. The general concept is shown in Fig. 2. The gate feed resistor *R* is chosen to ensure negligible gate current flows and provides RF isolation between the *Vgs* DC control and the RF signals in the FET. A value of circa 2k ohms is used for *R* in our designs.

To investigate the SIW tunability concept, we have created both a 73 GHz resonator in GaAs using the UMS Ltd PH10 process and also created a 23 GHz Rogers R4003C PCB version using surface mount GaAs transistors from CEL.

B. 73 GHz SIW on GaAs

The layout of the designed MMIC is shown in Fig. 3. The design uses the UMS PH10 MMIC process (70 µm GaAs substrate, 2 x 20 µm pHEMT devices as cold FET switches). In Fig. 3, the six TAPs of the tunable SIW directly abut to the main SIW metal work, with no inset.

All the pHEMTS are arranged with their gate fingers running east-west as required by the manufacturer. The pHEMTs are all controlled externally with simple DC voltage sources, fed through on-chip high value resistors to the gates. To turn on the pHEMTs a control of +0.8 V is used, and to turn them off -0.8 V is used. As a reference, a fixed untuned SIW is also provided on the MMIC, as can be seen on the left of Fig. 3. RF probing will use 150 µm GSG probes. The MMIC is currently being manufactured by UMS Ltd.

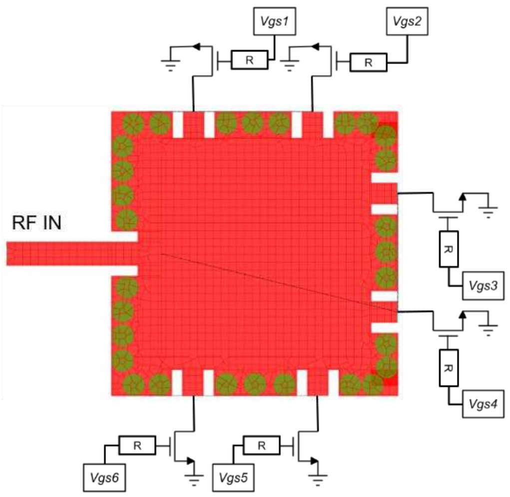


Fig. 2. SIW with vias removed and cold FETs added to TAPs.

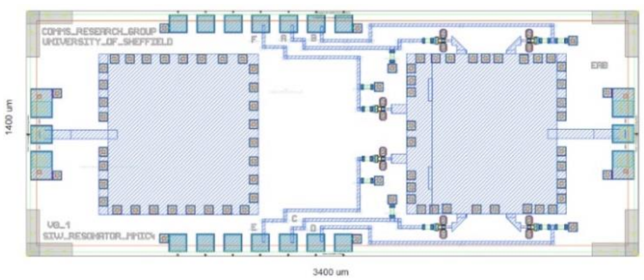


Fig. 3. MMIC layout of proposed 73 GHz SIWs: fixed SIW (left) and switched cold-FET tunable SIW (right).

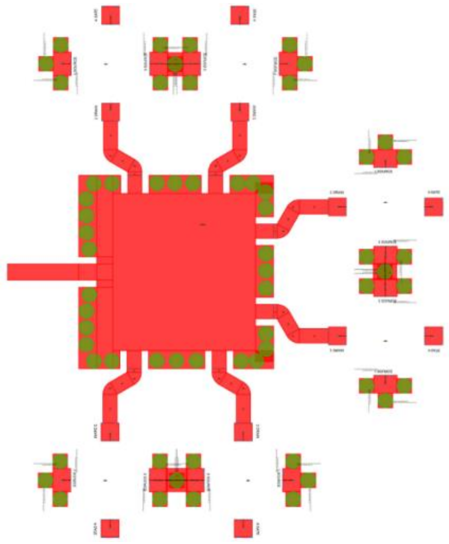


Fig. 4. PCB artwork of 23 GHz cold FET tuned SIW (FETs not shown).

C. 23 GHz SIW on PCB

The cold FET tuned SIW concept has also been investigated at 23 GHz, using Keysight ADS simulations and a manufactured PCB prototype using 0.2 mm thick Rogers R4003C. The design uses CE3520K3 GaAs packaged surface mount FETs from CEL. The on-state *Vgs* was 0 V and the off-state voltage was -2.0 V. A simple fixed SIW was also prepared. Fig. 4 shows the layout of the switched SIW, with six TAP lines to the FET drains emerging from the SIW. For clarity, the transistors and DC gate control circuitry is not shown.

III. Simulated and Lab Measured Results

A Keysight N5245B vector network analyser hosted at [6] was used to perform the RF measurements of return loss (RL). TRL calibration sets on the device under test are used to de-embed the measured results. The unloaded Q (Q_U) can be obtained from the measured loaded Q using the technique in [7].

A. 73 GHz GaAs SIW Simulation Results

In this section we present the Keysight ADS EM co-simulation results of the SIW MMIC at 73 GHz. Fig. 5 shows the de-embedded RL of the simple fixed-frequency SIW (left side of Fig. 3). Fig. 6 shows the RL of the switched resonator design (right side of Fig. 3) for a subset of switch states, ranging from all off to all on.

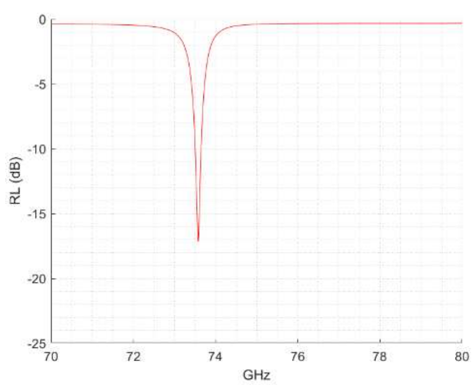


Fig. 5. ADS simulation of RL for simple fixed frequency SIW on GaAs.

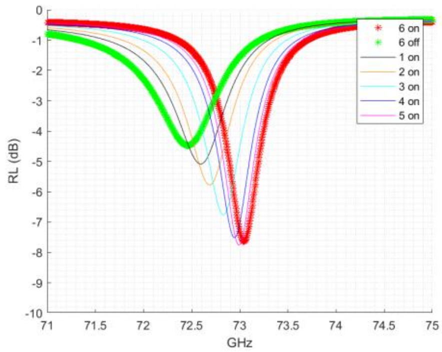


Fig. 6. ADS simulation of RL for cold FET switched SIW on GaAs.

TABLE I. ADS SIMULATION RESULTS OF 73 GHZ GAAS SIWS

SIW type	*Fo (GHz)*	*Qu*
Fixed frequency SIW	73.58	267
FET tuned SIW (all FETs off)	72.46	82
FET tuned SIW (1 FET on)	72.59	96
FET tuned SIW (2 FETs on)	72.69	108
FET tuned SIW (3 FETs on)	72.83	126
FET tuned SIW (4 FETs on)	72.94	139
FET tuned SIW (5 FETs on)	72.99	145
FET tuned SIW (All 6 FETs on)	73.05	152

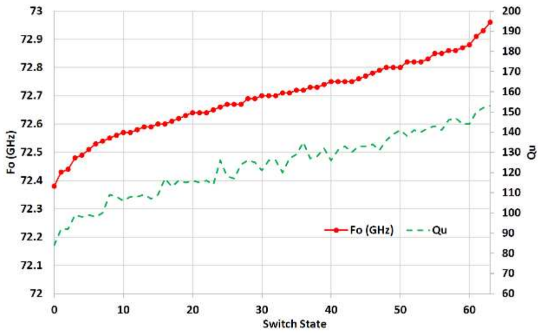
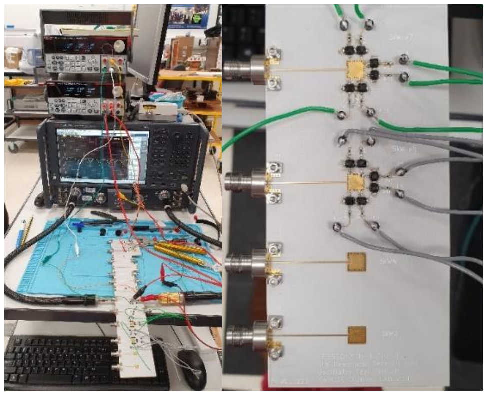


Fig. 7. ADS simulation of cold FET switched SIW on GaAs – tuning steps and *Qu* over all switch states.

The simulated resonant frequency (*Fo*) of the SIW concepts and associated *Qu* are summarised in Table 1. The full swept simulated performance over all switch states (from all off through to all on) of the cold FET switched GaAs SIW is shown in Fig. 7. The simulation results predict a tuning range of 580 MHz and RMS frequency step size of 13.5 MHz.

B. 23 GHz PCB SIW Simulation and Lab Measurements

The lab testing of the SIW 23 GHz PCB version of the concepts are shown in Fig. 8 (a) performed at [6]. The finished PCB concepts (2 of each type) are shown in Fig. 8 (b). De-embedding was performed using TRL standards also on the PCB. In Fig. 9 the comparison between the ADS Momentum co-simulation of the fixed SIW RL and associated PCB measured results are shown. The ADS simulated subset of tuning state RLs are shown in Fig. 10 and the corresponding measured PCB results are shown in Fig. 11. A summary of measured *Fo* and *Qu* for the RO4003C PCB versus simulated performance of the six cold FET tuned SIW is presented in Table 2.



(a) (b)

Fig. 8. SIW testing in lab. a) test setup using Keysight VNA, b) 23 GHz SIW test PCB - fixed SIWs at bottom and cold FET tuned SIWs at top.

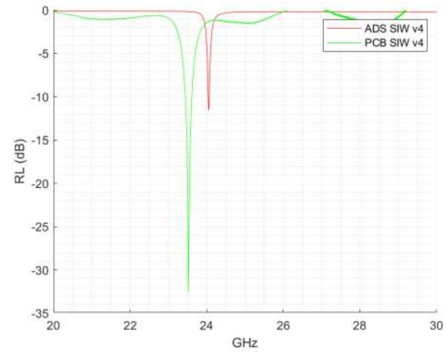


Fig. 9. Comparison of measured (de-embedded) fixed SIW to ADS model.

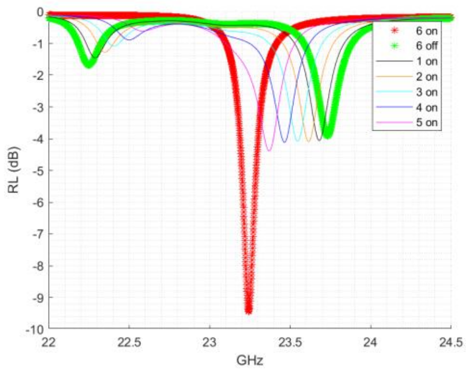


Fig. 10. ADS simulation of the cold FET switched 23 GHz SIW RL as function of selected switch state.

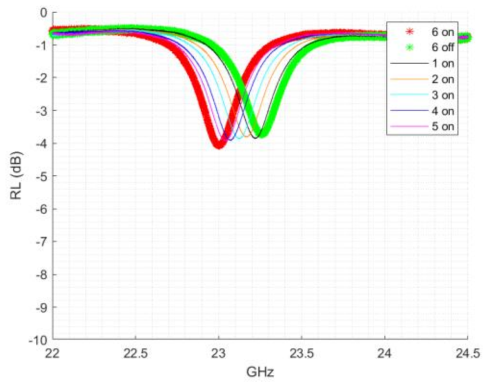


Fig. 11. De-embedded measured 23 GHz PCB six cold FET switched SIW RL as function of switch state.

TABLE II. 23 GHz PCB MEASURED AND SIMULATED SIWS

SIW type	*Fo Measured / Simulated (GHz)*	*Qu Measured / Simulated*
Fixed frequency SIW	23.53 / 24.05	89 / 254
FET tuned SIW (all FETs off)	23.26 / 23.73	71 / 139
FET tuned SIW (1 FET on)	23.22 / 23.68	74 / 140
FET tuned SIW (2 FETs on)	23.17 / 23.61	72 / 138
FET tuned SIW (3 FETs on)	23.12 / 23.55	73 / 134
FET tuned SIW (4 FETs on)	23.07 / 23.46	74 / 129
FET tuned SIW (5 FETs on)	23.04 / 23.37	73 / 116
FET tuned SIW (All 6 FETs on)	23.0 / 23.24	73 / 211

IV. DISCUSSION

The GaAs 73 GHz prototype is currently being manufactured by UMS - good tuning range and *Qu* are seen in simulation. The *Qu* of the fixed frequency SIW is notably good at 267, highlighting the key attraction in using SIWs and suggesting GaAs mmWave resonators are viable. The *Qu* is degraded in the cold FET tuned SIW, but it is interesting to note that the *Qu* tends to improve as more switches are turned on and follows the trend of the resonant frequency. The GaAs MMIC cold FET simulated SIW has an average *Qu* of 121 and a tuning range of 580 MHz (0.82 % tuning range). The RMS frequency step size is 13.5 MHz.

The measured 23 GHz PCB variant shows agreement with the simulated results. The PCB shows better RL on the fixed SIW due to it presenting a better match to 50 ohms, possibly due to tolerancing changes of the substrate loss and ε_r, compared to the model. The measured fixed 23 GHz SIW has a lower measured *Qu* of 89 (254 in simulation). However, the centre frequency of the fixed frequency SIW is within 2.2 % of the expected frequency. The measured cold FET tuned 23 GHz SIW has an average *Qu* of 72.9 (143.8 simulated) and a tuning range of 260 MHz (490 MHz simulated), giving a measured tuning range of 1.1 %. When all FETS are on, the measured cold FET 23 GHz SIW resonant frequency is within 1 % of the ADS simulation.

The variations in measured PCB prototype performance are possibly due to the parasitic effects of the transistor and its production tolerance spread. The transistor circuit models used the manufacturer's S parameters at fixed bias data, rather than our own measurements of actual devices. Further performance degradation could be due to additional substrate loss, dielectric tolerances, and manufacturing tolerancing issues related to via size and copper track and gap tolerancing not included in simulation.

A comparison of our SIW resonator concept to recent published works is made in Table 3, showing that the digital controlled cold FET tuned SIW has competitive performance and, to the authors' knowledge, is the first example of such a tuneable resonator at mmWave frequencies.

TABLE III. COMPARISON OF RECENT PUBLISHED WORKS ON TUNABLE SIW RESONATORS

Reference	*Centre Frequency (GHz) / Tuning Range (MHz)*	*Qu*	*Tuning Method*
[2]	9 / 630	138	Analogue (varactor)
[3]	10.5 / 360	150	Analogue (varactor)
[16]	58.6 / -	135	None (fixed filter)
[14]	1.8 – 2.4	291	Analogue (varactor)
[18]	11.7 / 492	286-299	Analogue (varactor)
This work (73 GHz MMIC)	73 / 580 (simulated)	121 (simulated)	Digital (cold FET)
This work (23 GHz PCB)	23 / 490 (simulated) 23 / 260 (measured)	144 (simulated) 72.9 (measured)	Digital (cold FET) Digital (cold FET)

V. CONCLUSION

In this paper we present a new concept for a digitally tuned SIW resonator using cold FETs. We have designed and simulated the resonator using a commercial MMIC process at 73 GHz. We have also tested and report a 23 GHz version of the design using R4003C PCB and commercial parts. In both designs we have demonstrated that tuning is possible and good *Qu* can be achieved.

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