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Evaluation of a 1200 V Polarization Super Junction GaN Field-Effect Transistor in Cascode Configuration

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Abstract: GaN HEMTs based on polarization super junction (PSJ) technology offer significant improvements in efficiency and power density over conventional silicon (Si) devices due to their excellent material characteristics, which enable fast switching edges and lower specific on-resistance. However, due to the presence of an uninterrupted channel between drain and source at zero gate bias, these devices have normally-on characteristics. In this paper, the performance of a 1200 V GaN FET utilizing PSJ technology in cascode configuration is reported. The device working principle, characteristics, and switching behavior are experimentally demonstrated. The results show that cascoded GaN FETs utilizing the PSJ concept are highly promising for power device applications.

Keywords: cascode; polarization super junction; 1200 V; GaN-FET

1. Introduction

GaN-based power switches have gained significant traction in recent years due to their excellent performance, which enables high efficiency and high-power density power electronic systems. The unique material characteristics of GaN, such as its high critical electric field of 3.3 MV.cm^{-1} and wide bandgap of 3.45 eV, make it possible for the fabrication of high-voltage devices with short drift regions. One of the distinct attributes of GaN is the ability to grow thin, high-quality epitaxial layers on widely available foreign substrates such as Si, SiC, and sapphire. However, the use of Si substrate for high-voltage devices of 1200 V and above presents substantial challenges such as crack formations due to thick GaN layers that compromise reliability, performance, and costs [1]. On the other hand, sapphire offers superior cost performance due to its insulating properties, which allow for the use of thin substrate and buffer layers [1]. Lateral GaN HEMTs utilizing GaN/AlGaN/GaN double heterostructures of appropriate dimensions and material properties can benefit from the polarization properties unique to group III–V materials, which can lead to the formation of the high density and high mobility of electrons (2DEG) and holes (2DHG) at respective heterointerfaces. These unique characteristics enable the design of high-voltage devices with low specific on-state resistance, particularly in the form of polarization super junction (PSJ) technology [2–5]. These PSJ devices can make use of the charge balance principle to achieve low specific on-resistance, ideally beyond the one-dimensional (1D) material limit [6,7]. Meanwhile, conventional GaN devices rely on several field plates to enhance breakdown voltage, which adds to processing and fabrication difficulties [1,8].

Due to the presence of a polarization-based 2DEG channel between drain and source in the absence of gate bias (i.e., V_{GS} = 0 V), conventional GaN HEMTs have normally-on

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characteristics. This behavior necessitates the application of a negative gate voltage to turn off the device, which is not considered desirable from an application viewpoint. Normally-off devices are preferred from a fail-safe point of view in the event of gate drive failure and to avoid shoot-through during circuit power-up sequence. There are various techniques that can shift the threshold voltage into a positive regime to create an enhancement mode (e-mode) of operation. One such popular method is the implementation of a p-GaN or p-AlGaN gate to deplete the 2DEG beneath the gate area to achieve an e-mode device [9]. Another method works by employing a recessed gate structure, where the thickness of the AlGaN layer beneath the gate is sufficiently reduced to interrupt the 2DEG channel [10]. Similarly, a recessed MOS gate structure has been demonstrated [11]. Many of the reported techniques rely on reducing the conductivity of the channel regions, which leads to an increase in on-state resistance. Moreover, these methods do not offer compatibility with standard MOSFET-based gate drivers. Another approach is the implementation of a cascode structure, which combines a high-voltage GaN HEMT with a low-voltage Si MOSFET in series configuration that enables compatibility with MOSFET-based gate drivers. Although several studies have reported 650 V cascode configurations [12–16], characteristics of higher-voltage devices are yet to be addressed in detail. In this paper, a 1200 V cascode GaN FET utilizing the state-of-the-art PSJ GaN HEMT is demonstrated. The device is evaluated through experimental measurements of static and dynamic characteristics to determine power losses.

2. Principle of Operation

The concept of super junction in silicon (Si) devices has paved the way for the development of low-resistance devices with geometrically optimized drift regions that can operate beyond the 1D material limit. This is normally achieved by charge balance through precise control over doping profiles of n-type and p-type regions [17,18]. Meanwhile, PSJ devices benefit from the charge balance arising out of polarization properties, and there is no impurity doping involved. The charge balance is achieved by the simultaneous presence of positive and negative polarization charges confined in respective double heterojunction interfaces [19]. As the device turns off, the 2DEG and the 2DHG are depleted through respective terminals, which leads to an even distribution of the electric field, which enables the device to withstand high voltages without the need for field plates. The p-GaN layer provides an ohmic contact to the 2DHG, which can be connected to the gate [19] or the source [3], depending on the design. Due to the uniform distribution of the electric field, PSJ devices do not suffer from the current collapse phenomenon [2]. A cross-sectional view of the depletion mode PSJ GaN HEMT with the p-GaN connected to the gate is shown in Figure 1.

Overall, PSJ devices offer excellent performance and high-reliability features at a low cost. Competing technologies such as SiC MOSFETs offer the benefits of wide bandgap materials. However, the fabrication costs and environmental impact associated with SiC devices pose major challenges to the widespread acceptance of the technology. A detailed discussion on the benefits of PSJ technology compared to SiC MOSFETs has been reported in [1].

A detailed analysis of the device characteristics and performance of the PSJ GaN HEMT is reported in [2,4]. In this work, as illustrated in Figure 2, a cascode configuration utilizing a high-voltage (HV) PSJ GaN HEMT and a low-voltage (LV) Si MOSFET that are rated for 1200 V and 30 V, respectively, is presented.

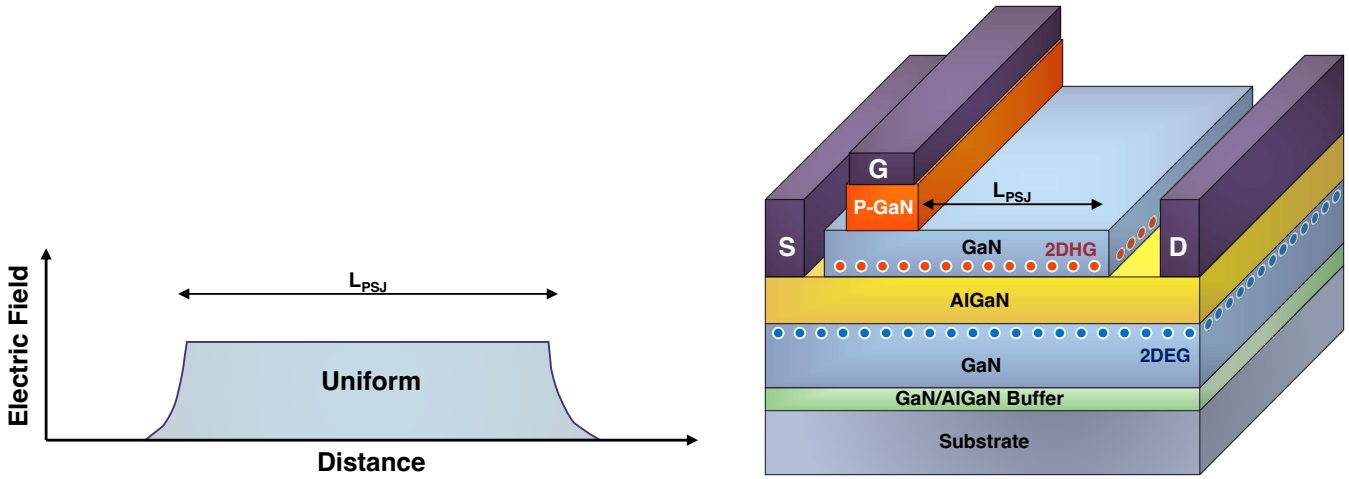


Figure 1. The electric field distribution (**left**) and a cross-sectional view of the PSJ GaN HEMT (**right**).

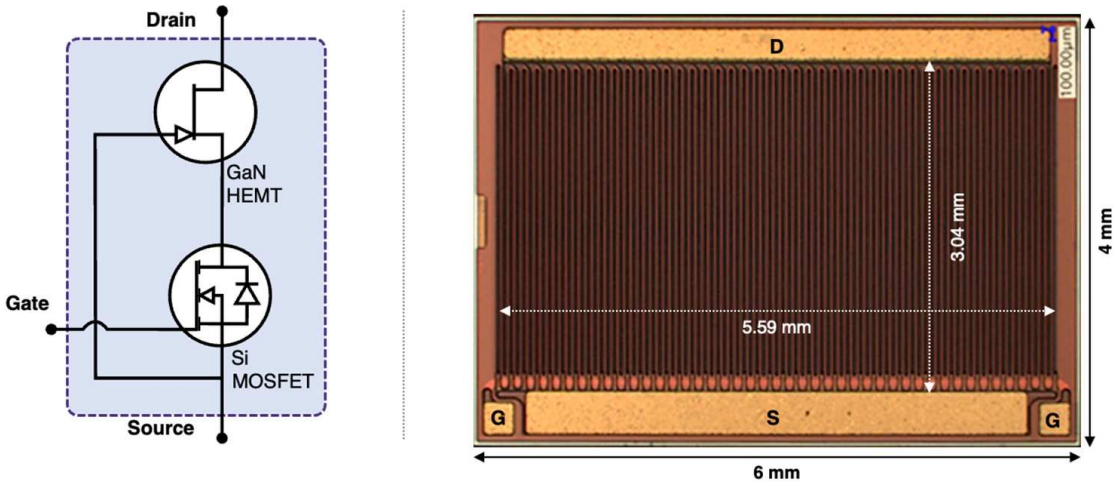


Figure 2. Cascode configuration (**left**) and the top view of a 1.2 kV PSJ GaN HEMT (**right**). Gate, drain, and source are marked as G, D, and S, respectively. The device image is reproduced from [4].

The voltage is effectively supported by the 1200 V PSJ GaN HEMT featuring an active area of 17 mm^2. The device is fabricated on a sapphire substrate. The length of the drift region (L_{PSJ}) is 20 µm, which determines the voltage blocking capability. The actual avalanche breakdown is more than 3.1 kV. The turn-on is initiated by the application of a positive gate bias above the threshold of the LV MOSFET. Once the MOSFET is turned on, the gate of the HEMT is shorted to its source, thereby causing the device to turn on. The turn-off occurs by removing the MOSFET's gate voltage, which leads to the drain potential to increase, which is equivalent to a negative gate voltage being applied to the HEMT. Once the drain voltage surpasses the threshold voltage of the HEMT, both devices are turned off. Under turn-off conditions, the output capacitances of the HEMT and the MOSFET form a capacitive voltage divider. The voltage distribution across these two capacitors can cause avalanche breakdown of the MOSFET. To mitigate this issue, various techniques can be utilized such as placing a parallel capacitor [20] with the MOSFET. However, no such additional circuitry is added in this cascode configuration. Since the gate of the HEMT is controlled through the MOSFET, the effect of the gate driver is expected to be minimal in terms of controlling the switching slew rates. A summary of the devices is presented in Table 1.

Table 1. Summary of key parameters of the cascode and its constituents. T_{amb} = 25 °C.

	PSJ GaN HEMT	Cascode GaN FET	Si MOSFET
Breakdown voltage	1200 V	1200 V	30 V
On-resistance	93 mΩ/120 mΩ *	125 mΩ	5 mΩ
Threshold voltage	−4.75 V	2 V	2 V

* Measured at 3 V and 0 V, respectively.

3. Experimental Methodology

The device is evaluated through a variety of static and dynamic measurements. The measurements were performed at a room temperature of 25 °C unless otherwise specified. A curve tracer/power device analyzer was employed to perform the static characterizations. These tests include pulsed I–V characterization of the output, transfer, and leakage current characteristics at various temperatures. To analyze the switching behavior of the device, a standard double pulse test, as shown in Figure 3, was set up.

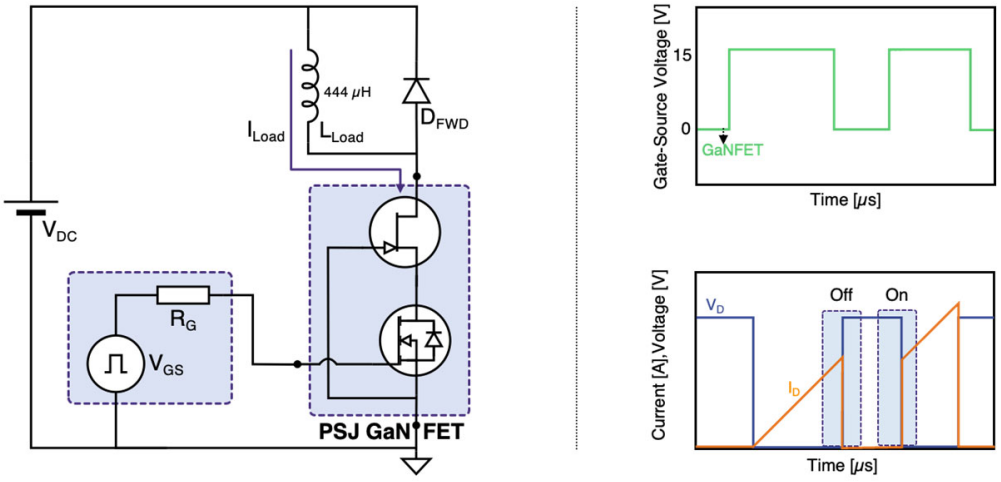


Figure 3. Circuit diagram of the experimental setup (**left**) and typical switching waveforms (**right**).

The circuit employs an inductive load of 444 μH in parallel with a 1200 V SiC Schottky diode. A standard isolated gate driver generates two pulses with an amplitude of 15 V and 0 V for turn-on and turn-off, respectively. The rise time and fall time are measured as the time taken for the drain voltage to switch from 10% to 90% of its final value. The switching energy losses are derived from the integration of the dissipated power over the switching period as given by Equation (1).

$$E_{Total} = E_{On} + E_{Off} = \int V_{Drain}.I_{Drain}dt \quad (1)$$

Additionally, the unclamped inductive switching (UIS) capability of the constituent GaN HEMT is evaluated using the same circuit presented in Figure 3 without the free-wheeling diode. The supply voltage is fixed at 50 V. The device is subject to UIS at different pulse widths until failure.

4. Experimental Results and Discussion

4.1. Static Characteristics

The output I–V characteristics of the device were measured in pulse mode at various gate voltages at 25 °C, as illustrated in Figure 4. Additionally, the normalized on-resistance was extracted from the measurements at different temperatures at a drain current of 5 A.

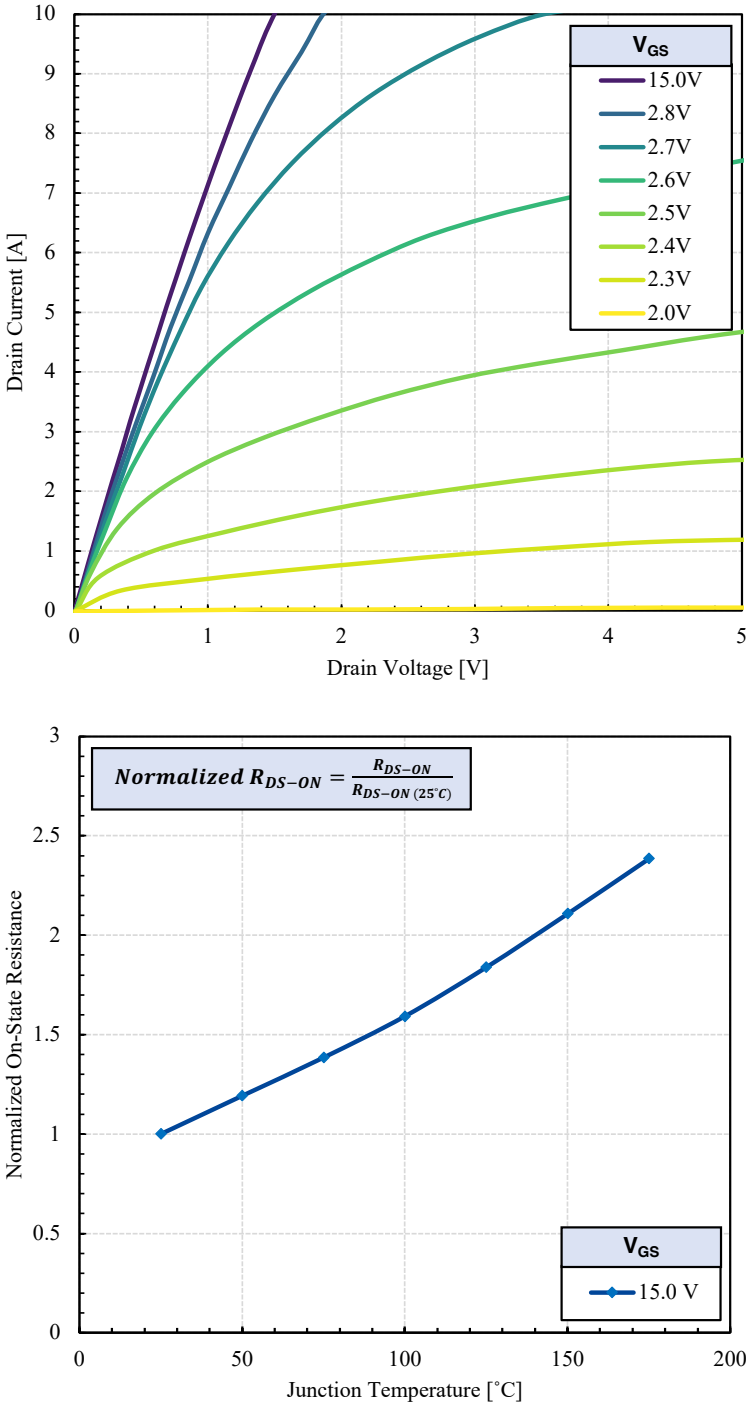


Figure 4. Measured (**a**) output I–V characteristics at RT and (**b**) normalized on-state resistance at different temperatures. The pulse width is 250 μs.

The total on-state resistance corresponds to 125 mΩ at RT and a gate voltage of 15 V. The on-resistance contribution of GaN HEMT is dominant in this case, accounting for approximately 120 mΩ. For this reason, the on-resistance variation (slope) as a function of gate voltage is minimal in cascode devices. The device exhibits a strong positive temperature coefficient of on-resistance due to the unipolar current flow. In the reverse conduction mode, the cascode GaN FET behaves similarly to conventional power MOSFETs. The measured reverse I–V characteristics of the device are illustrated in Figure 5.

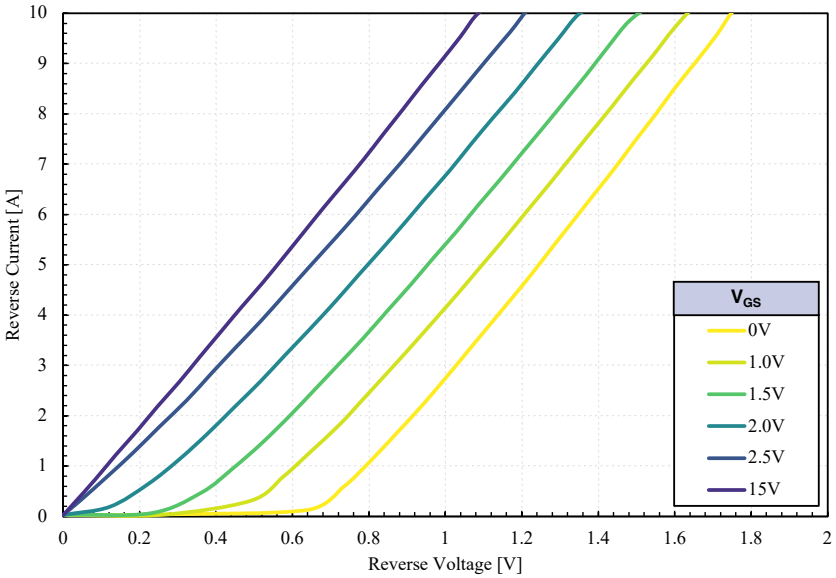


Figure 5. Measured reverse I–V characteristics of the 1.2 kV PSJ cascode GaN FET as a function of different gate voltages at RT. The pulse width is 250 µs.

The body diode of the LV MOSFET provides a path for current flow in the absence of gate bias. Applying a positive gate bias lowers the conduction threshold, and eventually the entire current flows through the channel, bypassing the body diode.

The transfer characteristics of the device were measured as a function of temperature and are shown in Figure 6a. The device exhibits a positive threshold voltage of 2 V at RT, which is governed by the constituent MOSFET. At a higher temperature, the threshold voltage decreases because of the increased amount of charge carriers [21]. However, the drain current is reduced due to the increase in the on-resistance of the GaN HEMT.

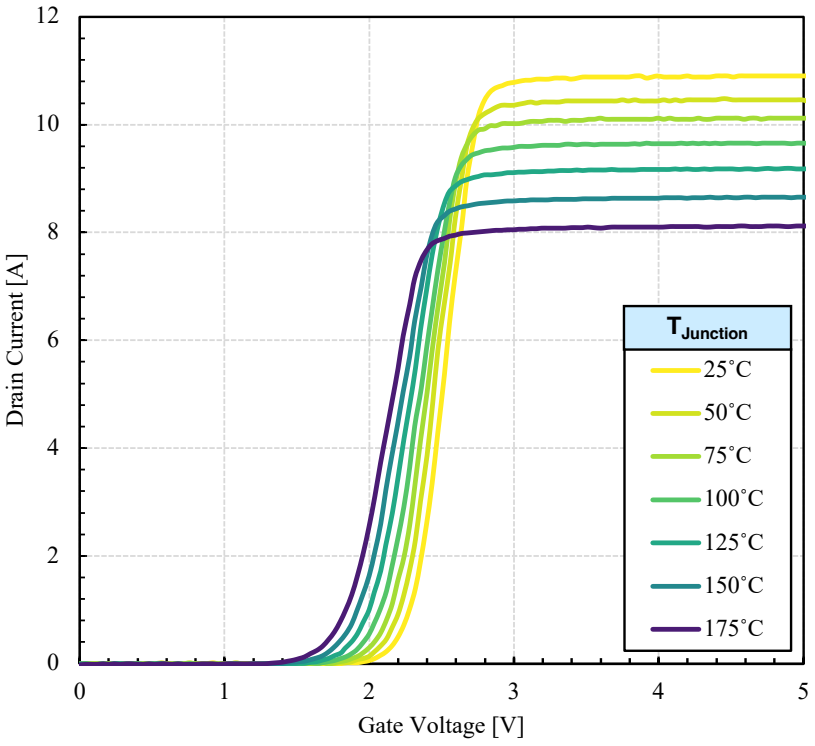


Figure 6. *Cont.*

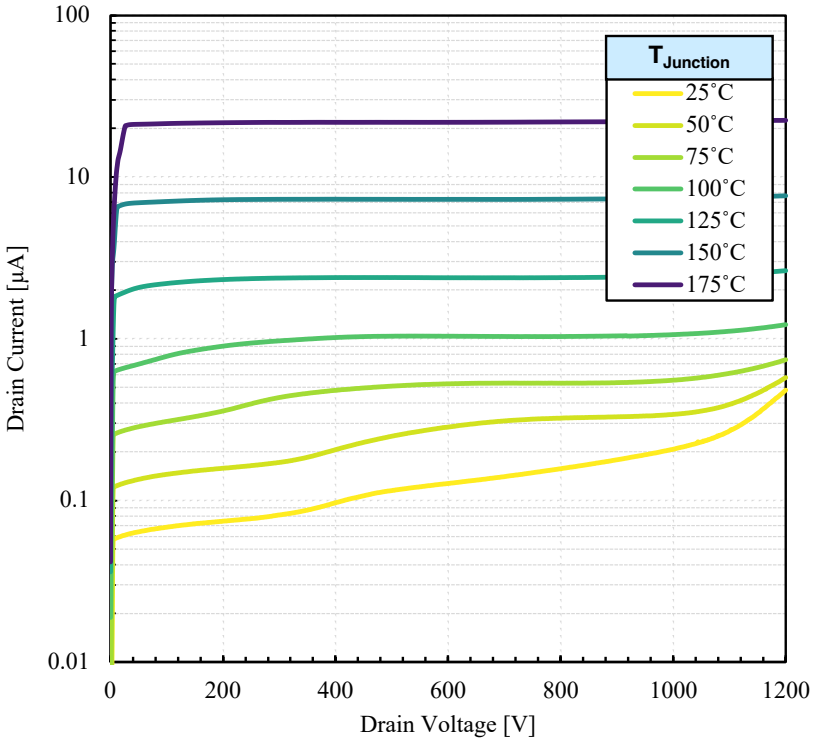


Figure 6. Measured (**a**) transfer I–V characteristics and (**b**) off-state leakage current characteristics at different junction temperatures. V_{GS} = 0 V.

The off-state leakage current was measured as a function of different junction temperatures at a gate-source voltage of 0 V, as illustrated in Figure 6b. The device shows a very small leakage current of less than 0.5 μA at 25 °C, which increases to 20 μA at 175 °C due to the wide bandgap nature of PSJ GaN HEMTs. This feature is considered to be important for the HEMT to have a low-leakage current to prevent premature avalanche breakdown of the LV MOSFET under switching conditions.

4.2. Dynamic Switching Characteristics

4.2.1. Switching Characteristics

The switching characteristics of the device at different load currents, including its on and off states, are illustrated in Figures 7a and 7b respectively.

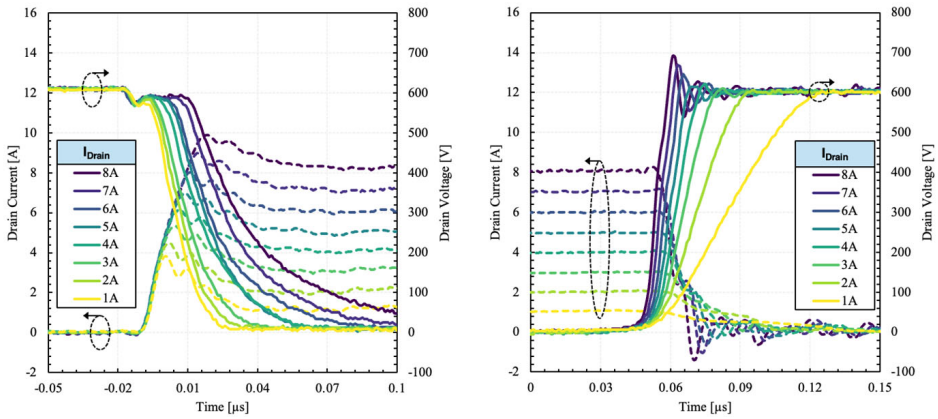


Figure 7. Measured (**a**) turn-on and (**b**) turn-off switching waveforms of the 1.2 kV PSJ cascode GaN FET at different load currents. R_G = 22 Ω, T_{amb} = 25 °C, V_{GS} = 15/0 V.

It can be observed that under low load conditions, the slew rate is lower. This is attributed to the parasitic capacitances of the device and circuit being charged and discharged at a slower rate during the switching transients. Based on the measurements, the switching energy losses were extracted, as shown in Figure 8.

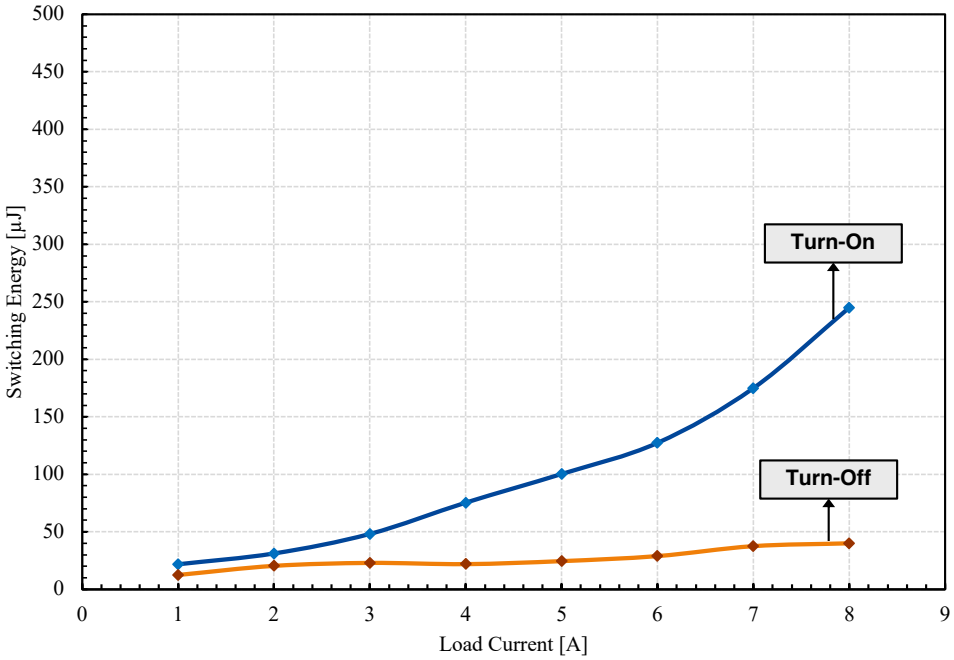


Figure 8. Measured switching energy losses of the 1.2 kV PSJ cascode GaN FET at different load currents. V_{DS} = 600 V, T_{amb} = 25 °C.

The switching losses increase with the load as the overlap of current and voltage becomes larger. The turn-on losses are higher than the turn-off, particularly noticeable at higher-load currents due to the impact of freewheeling diode on switching performance, which in this case is a SiC Schottky diode to minimize this impact.

4.2.2. dV/dt Controllability

GaN HEMTs exhibit high speed switching performance, which is ideal for high-frequency operation. However, the fast-switching edges of GaN can be challenging in certain applications such as motor drives. High dV/dt leads to degradation or failure of motor winding, as well as electromagnetic interference (EMI) [22,23]. This is particularly problematic in turn-off, as the overshoot voltage can exceed the components' rating. Conventionally, these issues can be mitigated via optimizing the gate resistor value to fit the application requirements. In the cascode configuration, the gate of the GaN HEMT is controlled via the LV MOSFET through an indirect control. The turn-off switching waveforms of the cascode GaN FET are shown in Figure 9.

As evident from the graph, the slew rate remains constant regardless of the gate resistance. It is noteworthy that the switching delay increases with the gate resistance. Therefore, to control the slew rate, cascode devices require external circuitry such as a snubber in parallel with the device, which can potentially impact the efficiency and require additional components.

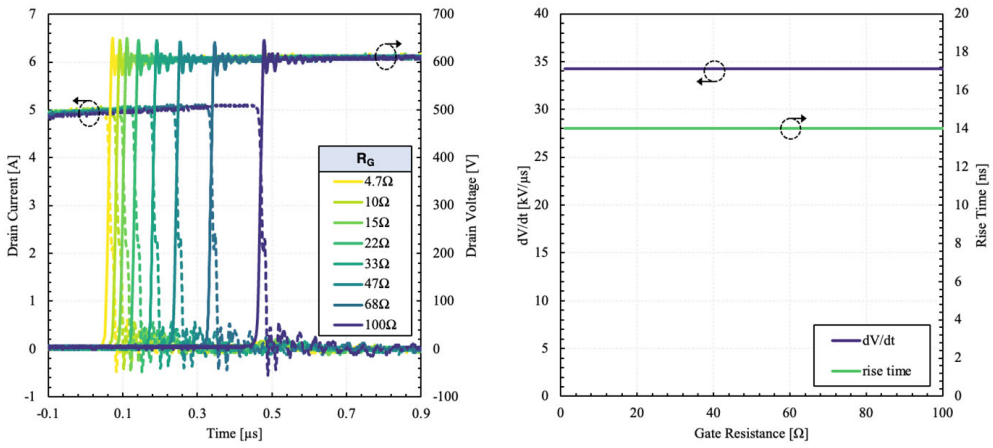


Figure 9. Measured (**a**) turn-off switching waveforms and (**b**) turn-off dV/dt controllability and rise time of the 1.2 kV PSJ cascode GaN FET at different gate resistances. T_{amb} = 25 °C, V_{GS} = 15/0 V.

4.3. Power Loss Analysis

Based on the measured data, the power loss contributions from conduction and switching losses at different frequencies are shown in Figure 10.

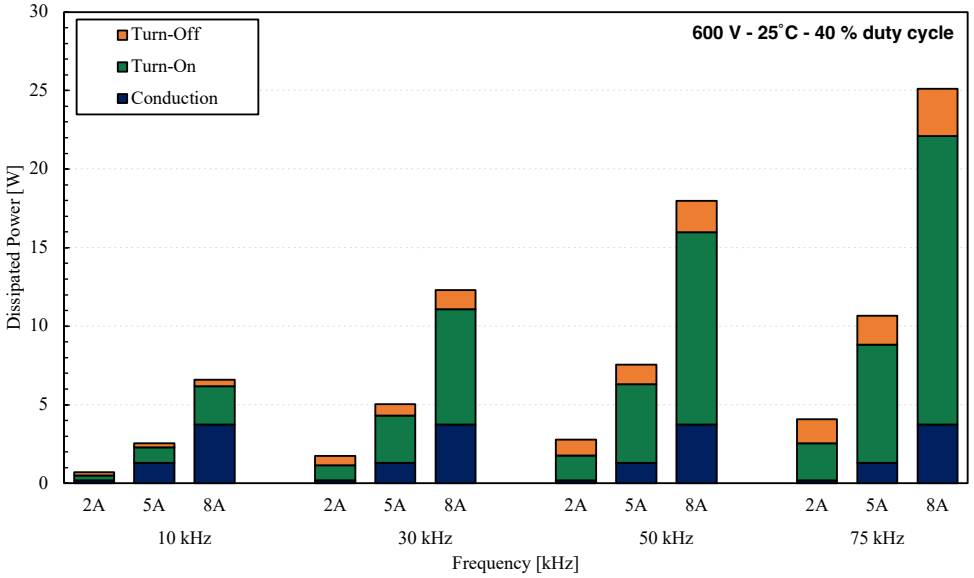
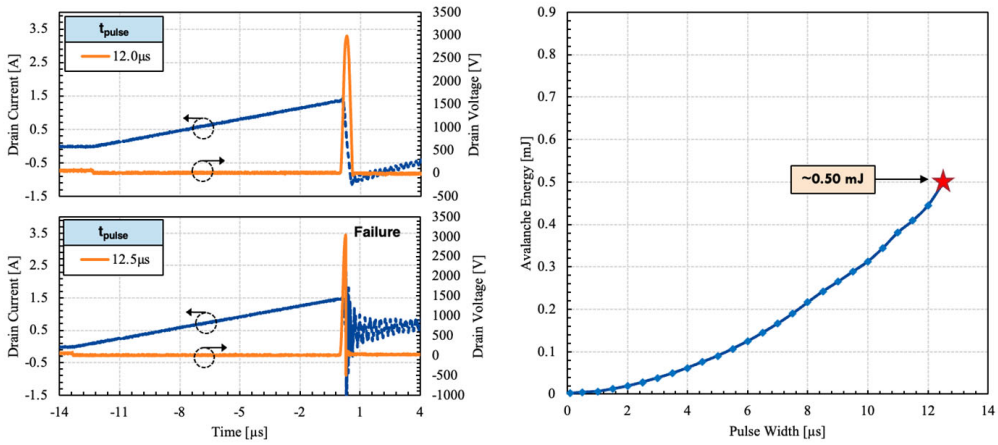


Figure 10. Measured power loss contributions in the 1.2 kV PSJ cascode GaN FET at different load currents and frequencies. R_G = 22 Ω, V_{DC} = 600 V, T_{amb} = 25 °C, V_{GS} = 15/0 V.

The device exhibits low power losses under various load conditions, and these losses are significantly lower than those of its silicon counterparts. At higher operating temperatures, it is expected that the conduction losses will become more significant due to the strong influence of temperature on the on-resistance. However, as reported in [2], the switching losses in PSJ HEMTs do not significantly change at elevated operating temperatures. The low switching loss profile of the PSJ GaN FET is ideal for high-frequency operation, which allows for a reduction in the size of passive components, thereby resulting in lower system costs and increased power density.

4.4. UIS Capability

GaN HEMTs, unlike conventional Si unipolar devices, cannot withstand avalanche transients. Consequently, most of the UIS energy is absorbed by the device parasitic capacitances, leading to a destructive avalanche breakdown [24–26]. In this section, the UIS capability of the constituent PSJ GaN HEMT is presented. The device was subjected to UIS at different pulse widths until failure. The voltage and current waveforms of the device prior to failure and at the moment of failure are shown in Figure 11.



(**a**) (**b**)

Figure 11. Measured (**a**) UIS waveforms and (**b**) avalanche energy of the 1.2 kV PSJ cascode GaN FET at different pulse widths. V_{DC} = 50 V, R_G = 51 Ω, T_{amb} = 25 °C, V_{GS} = 0/−15 V.

The measurements show that the device can withstand over 3.1 kV before the avalanche breakdown. The voltage is not clamped, as the device operates below the onset of avalanche breakdown. The negative current flow which occurs at the end of the applied pulse is due to the capacitive responses of the devices. The discharge of stored charges in parasitic capacitances generates a negative current flow. The absorbed energy before the failure is about 0.5 mJ. This large margin of breakdown voltage guarantees that the device remains protected from sudden surge voltage transients.

5. Conclusions

This work has presented, for the first time, a 1200 V PSJ GaN FET in cascode configuration utilizing unique PSJ technologies. The device characteristics and switching performance have been experimentally demonstrated. The device exhibits very low power losses under various load conditions. In terms of the controllability of dV/dt, the cascode device naturally switches at very high slew rates without any noticeable change, even when the gate resistance changes. External circuitry may be added if slower slew rates are needed. Overall, cascode GaN FET based on PSJ technology offers high performance and is ideal for integration into high-power-density, high-efficiency applications.

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References

1. Kawai, H.; Yagi, S.; Hirata, S.; Nakamura, F.; Saito, T.; Kamiyama, Y.; Yamamoto, M.; Amano, H.; Unni, V.; Narayanan, E.M.S. Low cost high voltage GaN polarization superjunction field effect transistors. *Phys. Status Solidi (a)* **2017**, *214*, 1600834. [CrossRef]
2. Sheikhan, A.; Narayanan, E.M.S.; Kawai, H.; Yagi, S.; Narui, H. Evaluation of a 3 kV Polarization Superjunction GaN HEMT. In Proceedings of the PCIM Europe, Nuremberg, Germany, 11–13 June 2024.
3. Nakajima, A.; Sumida, Y.; Dhyani, M.H.; Kawai, H.; Narayanan, E.M.S. GaN-Based Super Heterojunction Field Effect Transistors Using the Polarization Junction Concept. *IEEE Electron Device Lett.* **2011**, *32*, 542–544. [CrossRef]
4. Sheikhan, A.; Narayanan, E.M.S.; Kawai, H.; Yagi, S.; Narui, H. Evaluation of turn-off dV/dt controllability and switching characteristics of 1.2 kV GaN polarisation superjunction HFETs. *Jpn. J. Appl. Phys.* **2023**, *62*, 014501. [CrossRef]
5. Sheikhan, A.; Narayanankutty, G.; Narayanan, E.M.S.; Kawai, H.; Yagi, S.; Narui, H. Analysis of 1.2 kV GaN polarisation superjunction diode surge current capability. *Jpn. J. Appl. Phys.* **2023**, *62*, 064502. [CrossRef]
6. Nakajima, A.; Adachi, K.; Shimizu, M.; Okumura, H. Improvement of unipolar power device performance using a polarization junction. *Appl. Phys. Lett.* **2006**, *89*, 193501. [CrossRef]
7. Nakajima, A.; Sumida, Y.; Dhyani, M.H.; Kawai, H.; Narayanan, E.M.S. High Density Two-Dimensional Hole Gas Induced by Negative Polarization at GaN/AlGaN Heterointerface. *Appl. Phys. Express* **2010**, *3*, 121004. [CrossRef]
8. Saito, W.; Takada, Y.; Kuraguchi, M.; Tsuda, K.; Omura, I.; Ogura, T.; Ohashi, H. High breakdown voltage AlGaN-GaN power-HEMT design and high current density switching behavior. *IEEE Trans. Electron Devices* **2003**, *50*, 2528–2531. [CrossRef]
9. Uemoto, Y.; Hikita, M.; Ueno, H.; Matsuo, H.; Ishida, H.; Yanagihara, M.; Ueda, T.; Tanaka, T.; Ueda, D. Gate Injection Transistor (GIT)—A Normally-Off AlGaN/GaN Power Transistor Using Conductivity Modulation. *IEEE Trans. Electron Devices* **2007**, *54*, 3393–3399. [CrossRef]
10. Ikeda, N.; Li, J.; Kato, S.; Masuda, M.; Yoshida, S. A Novel GaN Device with Thin AlGaN/GaN Heterostructure for High-power Applications. *Furukawa Rev.* **2006**, *29*, 1–6.
11. Kambayashi, H.; Satoh, Y.; Niiyama, Y.; Kokawa, T.; Iwami, M.; Nomura, T.; Chow, P.T. Enhancement-mode GaN hybrid MOS-HFETs on Si substrates with Over 70 A operation. In Proceedings of the 21st International Symposium on Power Semiconductor Devices & ICs (ISPSD), Barcelona, Spain, 14–18 June 2009.
12. Zhang, W.; Huang, X.; Lee, F.C.; Li, Q. Gate drive design considerations for high voltage cascode GaN HEMT. In Proceedings of the IEEE Applied Power Electronics Conference and Exposition (APEC), Fort Worth, TX, USA, 16–20 March 2014.
13. Sugiyama, T.; Hung, H.; Isobe, Y.; Yoshioka, A.; Yasuzumi, T.; Sato, Y. Stable cascode GaN HEMT operation by direct gate drive. In Proceedings of the 32nd International Symposium on Power Semiconductor Devices and ICs (ISPSD), Vienna, Austria, 13–18 September 2020.
14. Liu, C.; Salih, A.; Padmanabhan, B.; Jeon, W.; Moens, P.; Tack, M.; Backer, E.D. Development of 650V Cascode GaN Technology. In Proceedings of the PCIM Europe, Nuremberg, Germany, 19–20 May 2015.
15. Huang, X.; Liu, Z.; Lee, F.C.; Li, Q. Characterization and Enhancement of High-Voltage Cascode GaN Devices. *IEEE Trans. Electron Devices* **2014**, *62*, 270–277. [CrossRef]
16. Huang, X.; Liu, Z.; Li, Q.; Lee, F.C. Evaluation and application of 600V GaN HEMT in cascode structure. In Proceedings of the IEEE Applied Power Electronics Conference and Exposition (APEC), Long Beach, CA, USA, 17–21 March 2013.
17. Fujihira, T. Theory of semiconductor superjunction devices. *Jpn. J. Appl. Phys.* **1997**, *36*, 6254–6262. [CrossRef]
18. Deboy, G.; Marz, M.; Stengl, J.P.; Strack, H.; Tihanyi, J.; Weber, H. A new generation of high voltage MOSFETs breaks the limit line of silicon. In Proceedings of the International Electron Devices Meeting (IEDM), San Francisco, CA, USA, 6–9 December 1998.
19. Nakajima, A.; Dhyani, M.H.; Narayanan, E.M.S.; Sumida, Y.; Kawai, H. GaN based Super HFETs over 700V using the polarization junction concept. In Proceedings of the International Symposium on Power Semiconductor Devices and ICs (ISPSD), San Diego, CA, USA, 23–26 May 2011.
20. Huang, X.; Du, W.; Lee, F.C.; Li, Q.; Liu, Z. Avoiding Si MOSFET Avalanche and Achieving Zero-Voltage Switching for Cascode GaN Devices. *IEEE Trans. Power Electron.* **2016**, *31*, 593–600. [CrossRef]
21. Toshiba Electronic Devices & Storage Corporation: Application Note: MOSFET Secondary Breakdown. Available online: https://toshiba.semicon-storage.com/info/application_note_en_20180901_AKX00077.pdf?did=63593 (accessed on 25 January 2025).
22. Akagi, H. Influence of high dv/dt switching on a motor drive system: A practical solution to EMI issues. In Proceedings of the 16th International Symposium on Power Semiconductor Devices and ICs (ISPSD), Kitakyushu, Japan, 24–27 May 2004.
23. Persson, E. Transient effects in application of PWM inverters to induction motors. *IEEE Trans. Ind. Appl.* **1992**, *28*, 1095–1101. [CrossRef]
24. Kozak, J.P.; Zhang, R.; Porter, M.; Song, Q.; Liu, J.; Wang, B. Stability, Reliability, and Robustness of GaN Power Devices: A Review. *IEEE Trans. Power Electron.* **2023**, *38*, 8442–8471. [CrossRef]

25. Saito, W.; Suwa, T.; Uchihara, T.; Naka, T.; Kobayashi, T. Breakdown behaviour of high-voltage GaN-HEMTs. *Microelectron. Reliab.* **2015**, *55*, 1682–1686. [CrossRef]
26. Saito, W.; Nishizawa, S.-i. Failure Process of GaN-HEMTs by Repetitive Overvoltage Stress. In Proceedings of the 35th International Symposium on Power Semiconductor Devices and ICs (ISPSD), Hong Kong, China, 28 May–1 June 2023.