



This is a repository copy of *To reset, or not to reset—that is the question.*

White Rose Research Online URL for this paper:

<https://eprints.whiterose.ac.uk/224282/>

Version: Published Version

Article:

Gehér, G.P. orcid.org/0000-0003-1499-3229, Jastrzebski, M. orcid.org/0009-0004-6221-9355, Campbell, E.T. et al. (1 more author) (2025) *To reset, or not to reset—that is the question.* npj Quantum Information, 11 (1). 39. ISSN 2056-6387

<https://doi.org/10.1038/s41534-025-00998-y>

Reuse

This article is distributed under the terms of the Creative Commons Attribution-NonCommercial-NoDerivs (CC BY-NC-ND) licence. This licence only allows you to download this work and share it with others as long as you credit the authors, but you can't change the article in any way or use it commercially. More information and the full terms of the licence here: <https://creativecommons.org/licenses/>

Takedown

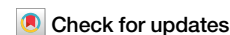
If you consider content in White Rose Research Online to be in breach of UK law, please notify us by emailing eprints@whiterose.ac.uk including the URL of the record and the reason for the withdrawal request.



eprints@whiterose.ac.uk
<https://eprints.whiterose.ac.uk/>



To reset, or not to reset—that is the question



György P. Geher¹ ✉, Marcin Jastrzebski^{1,2}, Earl T. Campbell^{1,3} & Ophelia Crawford¹

Whether to reset qubits, or not, during quantum error correction experiments is a question of both foundational and practical importance for quantum computing. Text-book quantum error correction demands that qubits are reset after measurement. However, fast qubit reset has proven challenging to execute at high fidelity. Consequently, many cutting-edge quantum error correction experiments are opting for the no-reset approach, where physical reset is not performed. It has recently been postulated that no-reset is functionally equivalent to reset procedures, as well as being faster and easier. For memory experiments, we confirm numerically that resetting provides no benefit. On the other hand, we identify a remarkable difference during logical operations. We find that unconditionally resetting qubits can reduce the duration of fault-tolerant logical operation by up to a factor of two as the number of measurement errors that can be tolerated is doubled. We support this with numerical simulations. However, our simulations also reveal that the no-reset performance is superior if the reset duration and infidelity exceed given thresholds. For example, with the noise model we considered, we find the no-reset performance to be superior when the reset duration is greater than approximately 100 ns and the physical error probability is greater than approximately $10^{-2.5} \approx 0.003$. Lastly, we introduce two novel syndrome extraction circuits that can reduce the time overhead of no-reset approaches. Our findings provide guidance on how experimentalists should design future experiments.

Quantum error correction (QEC) is a vital tool for unlocking quantum applications far beyond the capabilities of classical computers. QEC works by periodically measuring a set of multi-qubit Pauli operators, called stabilisers, providing evidence of errors that are then corrected. Measuring a stabiliser commonly involves a so-called syndrome extraction circuit that uses auxiliary qubits to assist with measurements on the data qubits that store the logical information. Many syndrome extraction circuits start by resetting the auxiliary qubits to the $|0\rangle$ state and end with single-qubit readout of the auxiliary qubits in the Z basis, thereby collapsing to either the $|0\rangle$ or $|1\rangle$ state [e.g.,¹, Sec. 4.4]. As these circuits are repeatedly used, the collapsed states on the auxiliary qubits need to be reset back to $|0\rangle$. Resetting can be achieved in various ways that seem, at first appearance, to be equivalent. However, in this paper, we reveal fundamental differences in the fault-tolerant properties of reset schemes previously thought to be similar.

Let us survey the three broad classes of reset strategy. The first class is *unconditional reset*, where a non-unitary operation maps all qubit states into the $|0\rangle$ state. The simplest option to achieve this is to wait until the qubits decay into their ground states². However, this is too slow for mid-circuit reset. By engineering a suitable interaction between a qubit and its environment, energy can be dissipated faster and with higher fidelity^{3,4}.

Unconditional reset is the conventional text-book approach and in the QEC literature is usually just called reset. The second class is *conditional reset*⁵, where a conditional bit-flip gate is applied on the auxiliary qubit if the previous measurement outcome was 1, otherwise no gate is applied. The duration of conditional reset depends on both the bit-flip gate duration and the classical electronics latency, which increase the execution time of the circuit. However, alternatively, we may simply track the effect of the conditional bit-flip in software, which is exactly what is involved in the third class, *no reset*^{6–8}. Recent years⁹ have seen QEC demonstrated with various qubit types^{10–12}. Focusing on superconducting qubits, several QEC experiments used the no-reset scheme^{6,8}, while others implemented unconditional reset^{13,14}, making it timely to investigate the differences between these approaches.

It has been previously claimed [ref. 13, Sec. S2] that choosing the no-reset scheme “has an insignificant impact on code performance”, but this has not been fully investigated. When using no reset or conditional reset, misclassification of measurements has two consequences: the wrong readout outcome is recorded, *and* an erroneous bit-flip (in software or on hardware) is applied to a qubit. This shows that a single failure event effectively causes a correlated pair of errors. The central question is whether this correlated

¹Riverlane, Cambridge, CB2 3BZ, UK. ²Department of Physics and Astronomy, University College London, London, WC1E 6BT, UK. ³School of Mathematical and Physical Sciences, University of Sheffield, Sheffield, S3 7RH, UK. ✉e-mail: george.geher@riverlane.com; gehergyuri@gmail.com

error significantly decreases the number of error events needed for an undetectable logical failure. On the one hand, we will confirm the claim from¹³ that for quantum memory there is no significant impact on QEC performance. On the other hand, we find dramatic consequences when we perform a logical operation. As we scale quantum computers, we enter an era where it becomes possible to demonstrate small examples of fault-tolerant quantum computation (FTQC), for instance, by performing a joint Pauli measurement via lattice surgery^{15–20}. During lattice surgery, classification errors on physical qubits alone can cause an overall misclassification of the logical Pauli measurement. When classical feedback is performed conditionally on this logical Pauli measurement, logical measurement misclassification transforms into a logical qubit error. In this context, we show that in the no-reset (and conditional-reset) schemes, these logical failure mechanisms (not present in quantum memory) may be formed by half as many errors as with unconditional reset. Consequently, to tolerate the same number of errors, no-reset schemes require doubling the duration of lattice surgery; such slow-down is clearly undesirable.

Tolerating half as many errors will impact QEC performance, though the exact effect depends on specific details, including the noise model. We complement our aforementioned analytical insights with numerical results for a range of superconducting-inspired circuit-level Pauli noise models. Our simulations use the stability experiment²¹ (see also Figs. 1 and 2) as a

proxy for lattice surgery and other experiments where similar logical failures occur. Our numerical results are consistent with a $2 \times$ advantage of unconditional resets in the limit of fast, low-error resets. In particular, with a physical error rate of 10^{-3} , which can be expected in the relatively near future, we observe substantial advantage with instantaneous reset, some advantage with fast reset and no advantage with slow reset. However, for nearer-term experimental demonstrations of FTQC, when the physical error rate is higher, we observe the no-reset scheme to be, in general, superior, especially with slow resets. We study this transition in detail, considering performance both in terms of numbers of QEC rounds and logical operation duration.

Finally, we propose and numerically compare two alternative syndrome extraction circuits for the planar code that do not use unconditional resets but substantially decrease the aforementioned incurred time overhead. One of these novel syndrome extraction circuits uses an additional two-qubit gate per measurement round, transforming the classification error into a mixture of two more benign errors. This circuit gets close to recovering the performance of unconditional reset using the no-reset scheme. The other novel syndrome extraction circuit we propose uses two auxiliary qubits per stabiliser, effectively squeezing two measurement rounds into one. As a result, this second circuit's QEC performance is substantially better in the examined noise regime than previous circuits, although it requires $\approx 50\%$ more qubits. Based on these results, we discuss when it is beneficial to use unconditional resets on superconducting hardware and when to use one of our alternative circuits.

The structure of our paper is as follows. The Results section is divided into four subsections. In the first subsection, we describe how the decoding problem changes when we switch from the unconditional-reset to the conditional-reset or no-reset scheme. In the second subsection, we first describe a Pauli noise model, inspired by currently available realistic superconducting hardware, that we use throughout. Then, we present numerical results that verify that the differences between the three reset schemes for quantum memory with the rotated planar code are small. After that, we describe the stability experiment and why it is a useful proxy for estimating the time cost of FTQC. Furthermore, we demonstrate through numerical simulations with the stability experiment that FTQC incurs a substantial time overhead in the no-reset (and conditional-reset) scheme, provided resetting is fast enough and is of high enough fidelity. In the last two subsections of the Results section, we present two alternative syndrome extraction circuits in the no-reset scheme that overcome this time overhead problem. Even though we present circuits only for the planar code, they can also be applied straightforwardly to more general QEC codes. We conclude the paper by discussing the obtained results and possible future research directions.

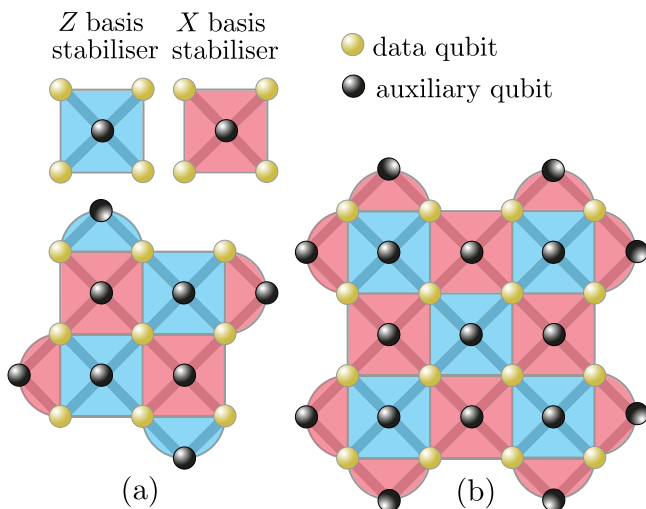


Fig. 1 | Stabilisers for the planar surface code. a Distance-3 quantum memory and **(b)** width-4 stability experiments. A range of distances, widths and numbers of rounds are used in our simulations.

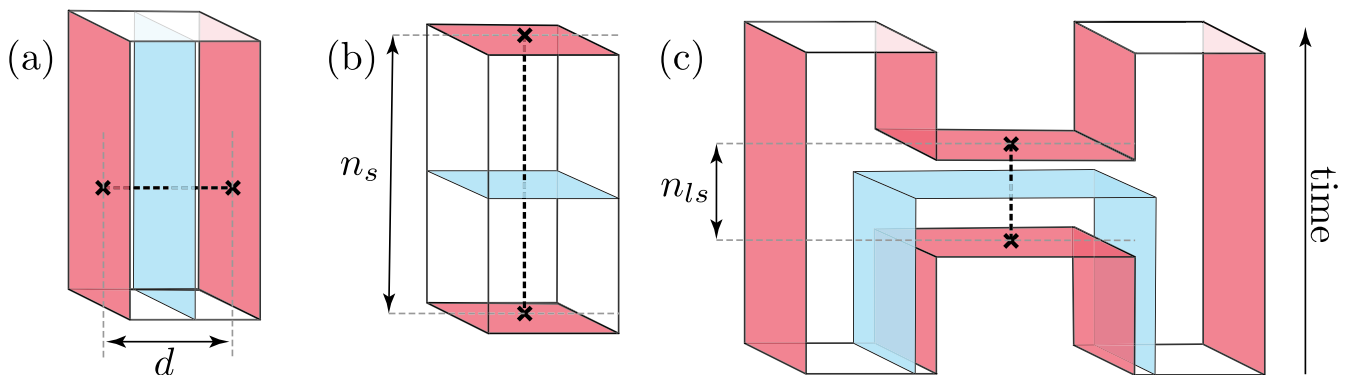


Fig. 2 | Topological space-time perspectives on logical failure mechanisms in QEC experiments. a A quantum memory experiment and a distance d undetectable logical error due to d physical qubit errors. **b** A stability experiment over n_s rounds and an undetectable logical error due to n_s measurement classification errors when using unconditional reset or $\lfloor n_s/2 \rfloor$ measurement classification errors when using

no-reset. **c** A lattice surgery experiment measuring a logical $X \otimes X$ Pauli operator with the logical error shown similar to that observed during stability experiments. In all diagrams, strings of physical qubit errors or measurement classification errors can terminate at pink boundaries. A logical failure occurs whenever these error strings pass through the blue surfaces an odd number of times.

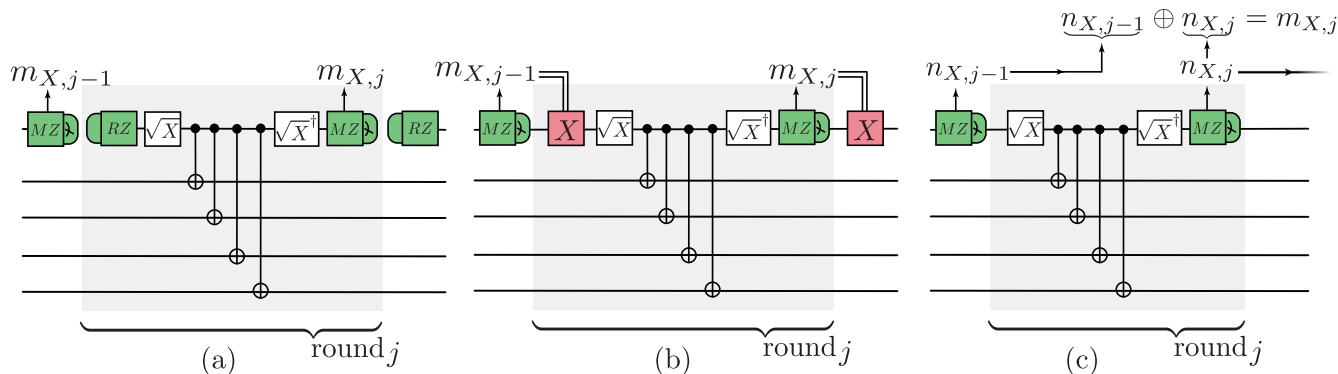


Fig. 3 | Standard syndrome extraction circuits for an XXXX stabiliser in the three reset schemes. The circuits use \sqrt{X} , \sqrt{X}^\dagger one-qubit gates, CX two-qubit gate, and Z-basis reset and measurement. **a** Standard text-book circuit using the unconditional-reset scheme. **b** The conditional-reset version of (a), where the classically-controlled bit-flip gate (pink) is applied immediately after measurement. **c** The no-reset version of (a) where the conditional bit-flip's effect from (b) is tracked in software; cf. Eq. (1). We note that, for our simulations, we compiled all circuits in terms of the native gates specified in Table 1.

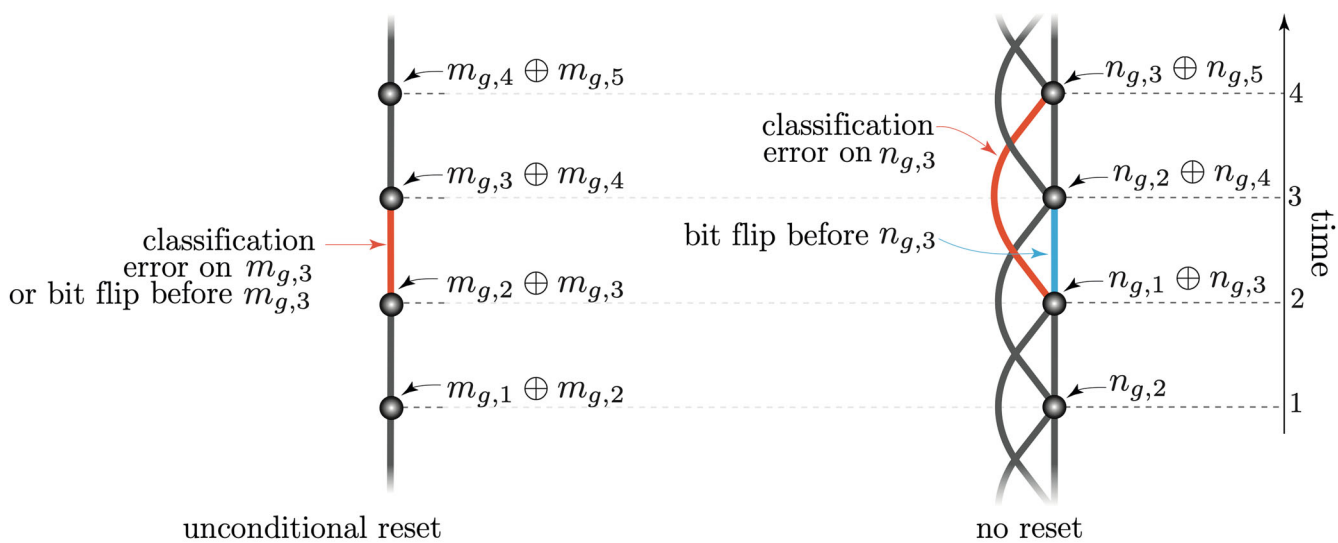


Fig. 4 | Decoding graphs for measurements from a single auxiliary qubit in the unconditional-reset (left) and no-reset (right) cases.

Results

The structure of detectors in the three reset schemes

A simple QEC experiment, like quantum memory or stability, with a Calderbank-Shor-Steane (CSS) code is composed of three steps: initialising the data qubits of a code in either the X or Z basis, measuring a set of stabilisers some number of times, and finally measuring the data qubits in the X or Z basis. More complicated QEC experiments, like lattice surgery, are composed of more steps. The stabilisers may be measured using standard syndrome extraction circuits shown in Fig. 3. With standard circuits, the stabiliser measurements directly correspond to the outcomes of the auxiliary qubits. More complex circuits, such as circuits with flag qubits²² or the circuit we discuss in the last subsection of the Results section, obtain further information.

In order to detect errors, we define detectors²³ that are measurement combinations with deterministic values in the absence of errors. We explain the detector definitions for simple CSS-code QEC experiments, as outlined in the previous paragraph, that use standard syndrome extraction with unconditional resets, like Fig. 3a. We may compose detectors for such experiments in the following way. For each stabiliser g , denote by $m_{g,j}$ the outcome from the j th QEC round, where $j \in \{1, 2, \dots, n\}$, and let (x, y) be the spatial coordinate of the auxiliary qubit of g . Between the first and last rounds of a QEC experiment, we define $m_{g,j} \oplus m_{g,j+1}$ as a detector at coordinate (x, y, j) for all stabilisers g and numbers of rounds $j \in \{1, 2, \dots, n -$

$1\}$. In the first round of QEC, if g is of the same type as the data qubit initialisation, then we assign $m_{g,1}$ as a detector with coordinate $(x, y, 0)$. In the last round of QEC, for stabilisers of the same type as the data qubit measurement, we assign a detector at coordinate (x, y, n) defined as $m_{g,n} \oplus \bigoplus_{q \in \text{supp}(g)} m_q$, where m_q is the measurement outcome of data qubit q . The first two coordinates of detectors are called spatial coordinates, while the last coordinate is called a time coordinate.

Now, we analyse which detectors are triggered (change value from the noise-free case) by different errors. A Pauli error on a data qubit occurring during the initialisation of the auxiliary qubits triggers only detectors with the same time coordinate. We refer to errors with this property as “space-like”. On the other hand, a measurement error (due to either quantum bit flip or classical misclassification) on the auxiliary qubit of g in the j th QEC round triggers at most two detectors, namely at coordinates $(x, y, j - 1)$ and/or (x, y, j) , as shown on the left of Fig. 4. Such an error is described as “time-like”. Some Pauli errors that occur mid-syndrome-extraction-circuit trigger a set of detectors where neither the spatial nor the time coordinates coincide for all the detectors – these are known as hook errors²⁴.

In order to evaluate the errors that have occurred during the experiment, the decoder takes in the triggered detectors along with a model of which errors trigger which detectors. For the planar code, in the case of a circuit-level Pauli noise model such as that described in the next subsection, to a good approximation, this model can be captured in a graph and

therefore graph-based decoders such as minimum-weight perfect matching (MWPM)^{24,25} can be used. We declare success in a run of the experiment if the decoder correctly predicts whether some logical observable has changed due to errors. In the case of W -quantum memory, for $W \in \{X, Z\}$, this logical observable is given by $\bigoplus_{q \in \text{supp}(\widehat{W})} m_q$, where \widehat{W} is the logical W operator of the code.

We now consider the case where we apply a bit-flip gate to each auxiliary qubit after measurement conditioned on the outcome (Fig. 3b, c) instead of applying unconditional resets. We may apply these X gates in hardware, to give the conditional-reset scheme (Fig. 3b), or track their effect in software, to give the no-reset scheme (Fig. 3c). As we will see, in both schemes, one measurement classification error leads to a pair of correlated errors, unlike with unconditional reset—a previously overlooked phenomenon. In the conditional-reset case, we define the detectors as above; in the no-reset case, we determine the detectors as follows.

For the no-reset scheme, we calculate the effect of removing all conditional X gates by pushing them through the subsequent unitary Clifford gates and find that a conditional X can be accounted for by flipping the subsequent measurement²⁶. Therefore, we can determine the stabiliser observable outcomes, $m_{g,j}$ from the no-reset measurement outcomes labelled $n_{g,j}$ as

$$m_{g,j} = n_{g,j-1} \oplus n_{g,j} \quad \text{for } j = 1, 2, \dots, n, \quad (1)$$

where we define $n_{g,0} = 0$; see Fig. 3c. Between the first and last rounds of QEC, the detectors at coordinate (x, y, j) are then

$$m_{g,j} \oplus m_{g,j+1} = n_{g,j-1} \oplus n_{g,j+1} \quad \text{for } j = 1, 2, \dots, n-1, \quad (2)$$

where we have used $n_{g,j} \oplus n_{g,j} = 0$ to simplify the expression. Therefore, instead of comparing outcomes from consecutive rounds, we compare outcomes that are two rounds apart.

Next, we consider the special case of the first and last QEC rounds. In the first QEC round, for each stabiliser g of the same type as the data qubit initialisation, we assign $n_{g,1}$ as a detector with coordinate $(x, y, 0)$. In the last round of QEC, for stabilisers of the same type as the data qubit measurement, we assign a detector at coordinate (x, y, n) for $n_{g,n-1} \oplus n_{g,n} \oplus \bigoplus_{q \in \text{supp}(g)} n_q$.

This structural difference of detectors does not change the triggered detectors corresponding to any mid-circuit quantum Pauli error. However, misclassification of a measurement outcome results in a different combination of triggered detectors to the unconditional-reset case. To see this, let us assume we have a classification error on measurement result $n_{g,j}$, i.e., we read out $n_{g,j} \oplus 1$, even though the qubit collapsed into the $n_{g,j}$ -eigenstate. This triggers two detectors at coordinates $(x, y, j-1)$ and $(x, y, j+1)$ (cf. Eq. (2)), so in the decoding graph it corresponds to a time-like edge with length 2. In contrast, even in the no-reset case, a quantum measurement error corresponds to a time-like edge with length 1. A bit-flip on the auxiliary qubit associated with stabiliser g just before measurement in the k th QEC round flips all measurements $n_{g,j}$ with $j \geq k$. This therefore triggers the detectors at coordinates $(x, y, k-1)$ and (x, y, k) . Both types of error are shown on the right of Fig. 4.

In Fig. 2, we present a topological perspective on how vertical strings of classification errors can lead to an undetectable logical failure in lattice surgery and stability experiments. In a lattice surgery operation, we measure a joint logical Pauli between 2 or more logical qubits, and the result is determined from a (corrected) product of stabiliser measurement outcomes. An uncorrected vertical string of classification errors will flip the value of one of these stabiliser measurements, and therefore flip the outcome of this logical Pauli measurement. The need to suppress such failure modes is why d QEC rounds is the standard recommendation. When lattice surgery is used to perform a non-Clifford gate (e.g. a T gate), we apply a logical Clifford gate conditional on the outcome of the lattice surgery measurement result. In such a situation, a logical measurement error during lattice surgery would be converted into a logical qubit error.

Such lattice surgery circuits are large and complex. Fortunately, we can instead use the smaller and simpler stability experiment, in simulation or on real qubits, to quantify the probability of logical failures due to a vertical string of errors. Stability experiments are therefore an excellent proxy for lattice surgery operations. Considering these vertical failure mechanisms, we see that the no-reset approach will tolerate only half as many classification errors as the unconditional-reset approach, since each error has twice the vertical length in the former scheme. This insight applies equally to lattice surgery and stability experiments. As we will see in the next subsection, this difference significantly impacts the performance of the stability experiment, and hence lattice-surgery-based FTQC. For other types of logical operation such as transversal gates, logical failure modes are less well understood—there is no known proxy in the same spirit as stability—and the required number of QEC rounds is an ongoing topic of debate^{27–29} that we regard as unsettled. For quantum memory, the no-reset approach does not reduce the weight of minimal-weight logical errors, and so in this context we should expect only a minor variation in logical error rates.

In the conditional-reset scheme, a classification error on $m_{g,j}$ further results in erroneously applying an X gate after measurement. As a result, the next measurement outcome $m_{g,j+1}$ is also flipped. Thus, two detectors are triggered at $(x, y, j-1)$ and $(x, y, j+1)$, introducing a time-like edge with length 2, as in the no-reset case.

QEC experiments with standard syndrome extraction circuits

Noise model. This work is motivated by the absence of unconditional resets in recent QEC experiments on superconducting devices^{6,8}. Therefore, the numerical results presented in this paper are from simulating a quantum computer with superconducting-like properties. These properties are the qubit connectivity, the native gates and the noise model.

We assume that the device has fixed and uniform qubit connectivity, with a planar nearest-neighbour architecture connecting each (bulk) qubit to four others. This so-called square-grid connectivity enables implementation of the planar code and is found in several modern superconducting quantum computers [e.g.,^{14,30}]. In the last subsection of the Results section, we will present a circuit that requires slightly different planar connectivity – some qubits need only be connected to three others instead of four.

We construct our simulated circuits³¹ in terms of the controlled- Z two-qubit gate (CZ) and single-qubit X - and Z -basis rotations, a common native gate set for superconducting qubits [e.g.,³⁰]. In particular, we use the $\pi/2$ rotations \sqrt{X} and S , given by

$$\sqrt{X} = \frac{1}{\sqrt{2}}(I - iX), \quad S = \frac{1}{\sqrt{2}}(I - iZ). \quad (3)$$

We also use Z -basis measurement (MZ) and reset (RZ). Each of these operations has an associated duration, given in Table 1. In particular, measurement and reset take an order of magnitude longer than one- and two-qubit gates (see also^{6,7}). The CZ gate takes only twice as long as a one-qubit gate.

We parameterise our noise model with a single parameter, p . The p -dependent probabilities of different error mechanisms are given in Table 1. These probabilities are based on an existing superconducting-inspired noise model³², with a few small differences. Firstly, we split the measurement noise into two – a quantum part, which is bit-flip noise applied to the qubit before the measurement, and a classical part, which is the misclassification of the outcome value, e.g., reading out 0 even though the qubit collapsed into the $|1\rangle$ state. This distinction is not commonly made, as they have the same effect under the unconditional-reset scheme. However, with no reset this distinction becomes important as the two types of measurement noises have different effects. We assign 80% and 20% of the noise respectively to these two mechanisms, inspired by existing hardware properties⁶. Secondly, when a qubit is idling, we apply noise depending on the length of time for which it is idle, t . The noise is obtained by Pauli twirling the amplitude damping and

Table 1 | Properties of our noise model inspired by current superconducting devices

Operation	Duration in ns
\sqrt{X} , S gate	20
CZ gate	40
measurement	600
(unconditional) reset	500
reference T_1	30,000
reference T_2	30,000
Error mechanism	Probability
1Q depolarisation after \sqrt{X} or S	$p/10$
2Q depolarisation after CZ	p
1Q bit-flip after reset	$2p$
1Q bit-flip before measurement	$4p$
classical measurement flip	p

(Top) Native qubit operations with their duration in nanoseconds, and reference T_1 and T_2 times corresponding to physical error rate $p = 0.01$. As p changes, the T_1 and T_2 times are scaled accordingly (see main text). For the stability experiment, we also consider faster resets; the 500 ns value here corresponds to slow reset. (Bottom) The noise channels associated with each operation. Notably, the measurement error has quantum and classical components that have the same effect in the unconditional-reset scheme; however, their effect is different in the no-reset (or conditional-reset) scheme.

dephasing channel to give a Pauli channel with associated probabilities

$$p_X(t) = p_Y(t) = \frac{1}{4} \left(1 - e^{-t/T_1} \right), \tag{4}$$

$$p_Z(t) = \frac{1}{2} \left(1 - e^{-t/T_2} \right) - \frac{1}{4} \left(1 - e^{-t/T_1} \right), \tag{5}$$

where p_W is the probability of a Pauli- W error occurring³³. To parameterise the idle noise by p , we scale the T_1 and T_2 times so that

$$T_1 = \frac{p^{\text{ref}}}{p} T_1^{\text{ref}}, \quad T_2 = \frac{p^{\text{ref}}}{p} T_2^{\text{ref}} \tag{6}$$

where T_1^{ref} and T_2^{ref} are given in Table 1 and $p^{\text{ref}} = 0.01$.

We note that our chosen noise model is not meant to capture the exact behaviour of any specific device. The analysis could be repeated with different device assumptions which may change the quantitative details of the results. However, it captures the key features of superconducting hardware and will be qualitatively representative of other qubit types.

The impact of no-reset on memory. Using the noise model described above, we performed quantum memory simulations for distance- d rotated planar code for d number of QEC rounds. Figure 5 compares the unconditional-reset and no-reset schemes. We constructed circuits using the python library `stim`³⁴ and took samples which were then decoded using the MWPM python library `pymatching`²⁵. The circuits are available here:³¹. The number of samples for each data point was the minimum required to observe 10^4 logical failures or reach 10^8 samples, whichever happened first. This ensures error bars that are too small to be visible in our plots. We calculated the sample logical failure probabilities p_X and p_Z , for X and Z -memory, respectively, and combined them into one quantity as $p_L = p_X + p_Z - p_X p_Z$. Our results (Fig. 5) confirm the statement of¹³, mentioned earlier, that there is only a small difference between the two reset schemes in the context of quantum memory. More precisely, the no-reset scheme’s performance is slightly better, as the threshold is somewhat higher and the logical failure probabilities are slightly lower. One reason for this difference is that the idle noise on the data qubits is lower in the no-reset case.

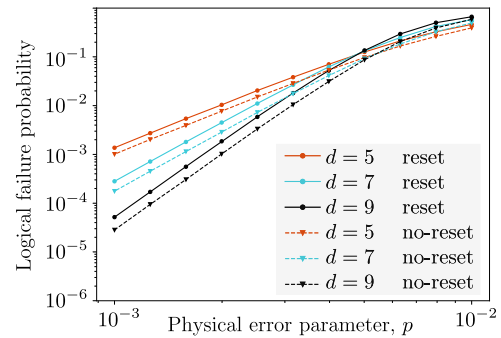


Fig. 5 | Comparison of quantum memory performances in the unconditional-reset (dots and solid lines) and no-reset (triangles and dashed lines) schemes using standard syndrome extraction circuits. For each distance $d = 5, 7, 9$ (corresponding to red, blue, black colours), we performed d QEC rounds. The numbers of samples taken to calculate the data points are sufficiently large for the error bars not to be visible. As can be seen, there is only a small difference between the two schemes, confirming the statement made in [ref. 13, Sec. S2]. Note that the conditional reset scheme is not shown as the simulation is identical to the no-reset simulations except with higher noise levels due to the increased physical qubit idling. As a consequence, the conditional-reset scheme will always perform worse and is therefore not shown here.

Note, however, that, as we will see below, the time-like effective distance (i.e., the number of mid-circuit errors that cause an undetectable time-like logical failure) is halved in the no-reset scheme for the stability experiment. Therefore, in the no-reset scheme, it may be more reasonable to perform $2d - 1$ number of QEC rounds instead of d . Increasing the number of rounds for quantum memory degrades its performance, eroding the slight advantage of the no-reset scheme.

The impact of no-reset on FTQC. During FTQC, there are purely time-like undetectable logical failures that would be affected by the choice of reset scheme. For instance, if we measure a joint logical Pauli product via lattice surgery between some logical qubits that are each encoded into a planar code, then this outcome is given as a joint parity of a set of stabilisers^{15,17,18}, see also Fig. 2(c). To make this fault-tolerant, we measure these stabilisers for n QEC rounds, with n sufficiently large. With the unconditional-reset scheme, the minimum number of errors that causes an undetectable logical failure is n , e.g., when one stabiliser is misclassified in all QEC rounds. However, with the no-reset scheme, this number becomes $\lceil n/2 \rceil$, as now it is enough to misclassify this measurement in the first, third, fifth, etc. QEC rounds.

The stability experiment²¹ captures this type of situation in a simplified proxy and thus can be used to assess the necessary number of QEC rounds during lattice surgery and other operations where time-like logical failures are relevant. We use a planar code patch that does not encode any logical qubits, but, instead, has one type of stabiliser that is over-determined. Figure 1b shows an example 4×4 stability patch where the X -type stabilisers multiply into the identity operator and so are over-determined. This stability experiment is performed as follows: we initialise all data qubits in the $|0\rangle$ state, then measure the stabilisers for n rounds, and finally we measure all data qubits in the Z basis. We assign detectors as described in the previous subsection, and define the logical observable as the product of all X -type stabilisers in the first QEC round. Mirroring lattice surgery, a minimum of n measurement errors amount to an undetectable logical failure in the unconditional-reset scheme, while $\lceil n/2 \rceil$ classification errors are sufficient in the no-reset scheme, cf. Eqs. (1), (2).

Based on this, we would expect the stability performance to be improved by using unconditional resets – assuming fast enough and high-enough fidelity reset gates. We performed simulations to assess this. We considered planar code stability patches of sizes $w \times w$ with $w \in \{4, 6, 8, 10, 12, 14, 16\}$ and physical error rates $p \in \{10^{-2}, 10^{-2.5}, 10^{-3}\}$. For each, we prepared `stim` circuits³¹, sampled, and decoded until we reached either 10^9

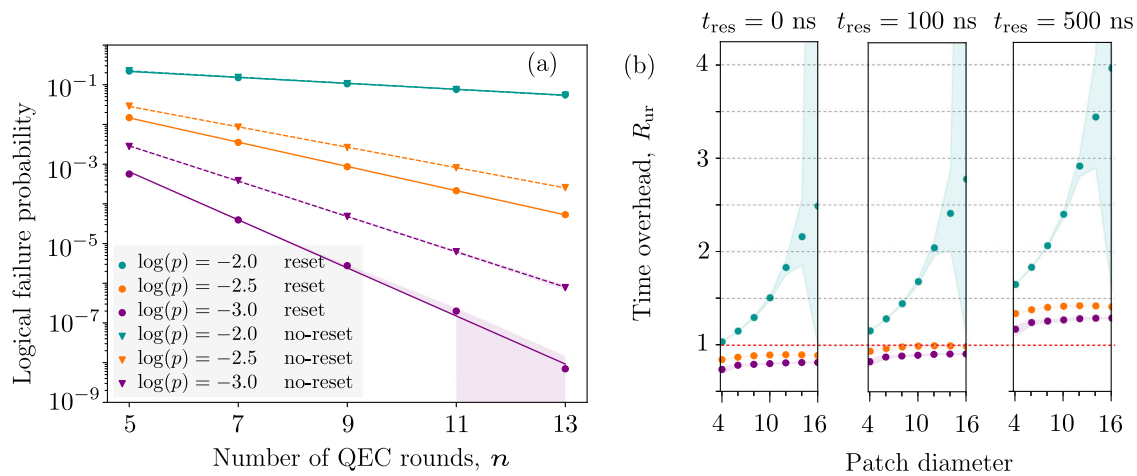


Fig. 6 | Comparison of the stability experiment performances in the two reset schemes using standard syndrome extraction circuits. Colours indicate different physical error probabilities: $p = 10^{-2}$ (blue), $p = 10^{-2.5}$ (orange), $p = 10^{-3}$ (purple). **a** Logical failure probabilities of the stability experiment for the 4×4 patch shown in Fig. 1b plotted against the number of QEC rounds. Error bars corresponding to $3 \times$ the standard error of the mean are also shown as shaded areas. Note that for the $p = 10^{-2}$ case the plots overlap. The unconditional reset is plotted with dots, the no-reset with triangles. Best log-line fits are also shown with solid and dashed lines, respectively. **b** The time overhead R_{ur} that the unconditional-reset scheme requires when compared to the no-reset scheme given $t_{res} = 0$ (instantaneous), 100 (fast) and

500 ns (slow) resets, respectively. In particular, the first column of dots in the first plot corresponds to (a), since instantaneous reset implies equal execution time in the two reset schemes. The shaded areas correspond to 90% confidence intervals. The pink dashed line shows the break-even point, i.e. when $R_{ur} = 1$, below which the unconditional reset has better FTQC performance. Note that the conditional reset scheme is not shown as the simulation is identical to the no-reset simulation except with higher noise levels due to the increased physical qubit idling. As a consequence, the conditional reset scheme will always perform worse and is therefore not shown here.

total shots or 10^6 logical failures, whichever happened first. The obtained logical failure probabilities plotted against the number of QEC rounds, $n = 5, 7, 9, 11, 13$, are shown in Fig. 6a for the $w = 4$ case. They clearly show that implementing unconditional reset improves the performance for $p = 10^{-2.5}, 10^{-3}$. Furthermore, this improvement increases as p decreases.

We now quantify this improvement. In the stability experiment, we expect the logical failure probability p_L to satisfy

$$\log(p_L) = \log(a) - \gamma n, \tag{7}$$

where a and γ both depend on the width of the patch w [ref. 21, Section “Discussion”]. The γ parameter quantifies the strength of the exponential error suppression with the number of rounds in the stability experiment. Note that one QEC round takes $t_{nr} = 840$ ns with the no-reset scheme and, if the reset duration is t_{res} ns, one QEC round takes $t_{ur} = (840 + t_{res})$ ns with the unconditional-reset scheme. These two times are equal only with instantaneous reset, i.e., $t_{res} = 0$ ns. Therefore, as a fairer comparison, Equation (7) may be expressed in terms of the time t the experiment requires, instead of the number of QEC rounds, so that

$$\log(p_{nr,L}) = \log(a_{nr}) - \gamma_{nr} t \tag{8}$$

$$\log(p_{ur,L}) = \log(a_{ur}) - \gamma_{ur} t, \tag{9}$$

where subscripts nr and ur indicate the no- and unconditional-reset schemes, respectively. We define the time overhead of implementing unconditional resets as $R_{ur} = \gamma_{nr}/\gamma_{ur}$ [ref. 35, Sec. 5.2]. This can be interpreted as follows: if we perform a stability experiment for t_{nr} ns without unconditional resets then, in order to match this performance using unconditional resets, we need to spend approximately $t_{ur} = R_{ur} t_{nr}$ ns. If $R_{ur} < 1$, then implementing unconditional resets decreases the time cost of FTQC, and hence is worth implementing; otherwise not. The time overhead is plotted in Fig. 6b, assuming instantaneous reset $t_{res} = 0$ ns, fast reset $t_{res} = 100$ ns, and slow reset $t_{res} = 500$ ns. The plotted error bars correspond to 90% confidence intervals. More precisely, for each data point, we sampled 1000 times from a normal distribution with mean given by the sampled logical error probability, and standard deviation given by the standard error

of the mean. Then, we took the best log-line fits for each of the 1000 cases, calculated the corresponding time overheads, and removed the 50 smallest and the 50 largest values hence obtained. The minimum and maximum of the remaining values are the bottom and top error bars, respectively. We call p_{br} the break-even point, where $R_{ur} = 1$. Clearly, as t_{res} increases, p_{br} decreases. Furthermore, it can be seen in Fig. 6(b) that, as p decreases, the time overhead decreases too, indicating that when p is small enough, implementing unconditional reset improves FTQC performance. In all cases of instantaneous and fast reset, the break-even point satisfies $10^{-2.5} < p_{br} < 10^{-2}$. With slow reset, the break-even point is not visible in our plot, and we expect it to be at very low p . This indicates that, unless the reset gate error rate and duration are below certain values, implementing unconditional reset may not be beneficial for FTQC. However, if the break-even point is reached, either with decreased reset duration or higher-fidelity reset gates, the unconditional-reset scheme substantially improves FTQC performance.

Recovering time-like distance by spreading classification errors

We have seen that the absence of unconditional resets halves the time-like effective distance of FTQC protocols when using standard syndrome extraction circuits. In this section, we present an alternative syndrome extraction circuit that recovers the full time-like effective distance without the need for unconditional resets, and which also keeps the space-like effective distance as d . This circuit uses one additional two-qubit gate per QEC round and an additional $O(d)$ qubits.

The idea is to spread the auxiliary qubit measurement classification errors to the data qubits, thereby triggering additional detectors and thus requiring more errors for an undetectable time-like logical failure. We achieve this by applying two conditional Pauli gates immediately after measuring the auxiliary qubit – one conditioned on the measurement outcome and the other conditioned on the auxiliary qubit state itself; see Fig. 7 for an X -stabiliser circuit. Note that the controlled gates are of Z -(X -)type for X -(Z -)type stabilisers, and that the classically-controlled gates do not have to be applied on the device—instead, their effect can be tracked in software. In the absence of a measurement classification error, the two conditional gates cancel so there is no overall effect on the data qubits. However, if there is a classification error, exactly one of the gates will have an effect, resulting in a Pauli gate being applied to the data qubit which then

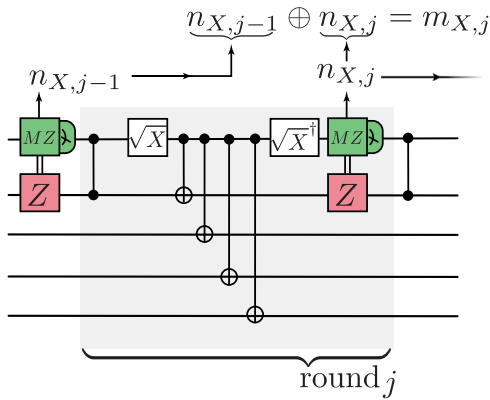


Fig. 7 | Syndrome extraction circuit for an XXXX stabiliser that spreads the classification error to a data qubit. Immediately after measurement, we apply a classically-controlled phase-flip and a CZ quantum gate. There is no overall effect, unless there was a classification error on $n_{X,j-1}$, in which case a Z error is transferred to a data qubit.

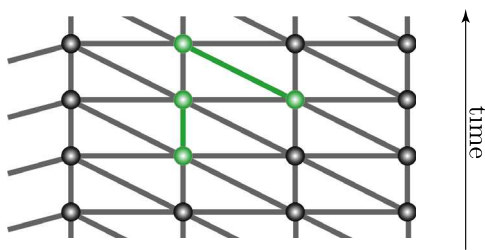


Fig. 8 | A cross-section of the decoding graph for the error-spreading circuit. In the bulk, it is the same as for standard unconditional-reset circuits. A classification error triggers four detectors (green nodes). This error can be decomposed into a quantum measurement error and a hook error (green edges).

behaves like a Pauli error on the qubit. Therefore, misclassification of measurement $n_{g,j}$ will now trigger four detectors—the two which directly result from the measurement classification error, at coordinates $(x, y, j - 1)$ and $(x, y, j + 1)$, and the two which arise from the resulting data qubit error, at coordinates (x, y, j) and (x', y', j) . This pattern is shown in Fig. 8, together with its decomposition into two graph-like errors. Reference³¹ contains an example decoding graph for a 4×4 stability experiment using the error-spreading circuit that we generated with `stim`. In Fig. 9, we show a 4×4 planar code stability patch and the qubit pairs which take part in error-spreading events. In the bulk of the code, we require no additional qubits. However, on the boundary, we require $O(w)$ additional qubits for a $w \times w$ patch to ensure each auxiliary qubit has a qubit to which to spread its classification error; cf. Fig. 1b.

It is easy to see that an undetectable logical error will no longer occur if there are classification errors in only every other round because of the additional detectors now triggered by a classification error. Furthermore, by searching exhaustively with `stim`, we find that, at least for small examples, n errors are required for an undetectable logical failure in an n -round stability experiment. For quantum memory, it is straightforward to see that we need at least d errors for an undetectable logical failure, as each classification error only triggers detectors whose spatial coordinates are adjacent, as in the standard circuit case.

We simulated the error-spreading circuits in order to compare the performance to standard syndrome extraction circuits with no reset. We applied the same principles for the number of shots as in the previous subsection. We present the quantum memory results in Fig. 10 and see that the performance is somewhat (although not significantly) diminished from the standard no-reset case. We attribute this to the error-spreading feature and the slightly higher depth of the error-spreading circuits. However, as we

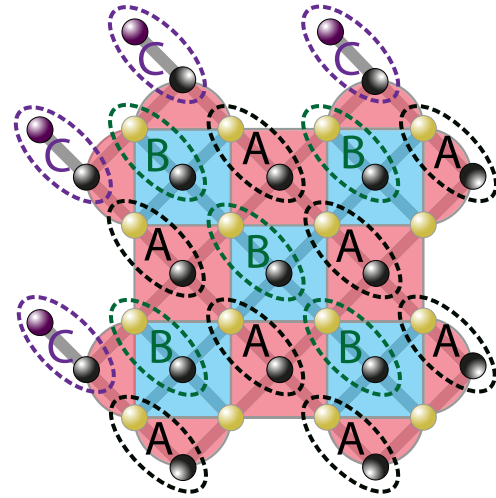


Fig. 9 | A 4×4 stability patch with additional qubits (purple) that are needed for the error-spreading circuit. Pairs of qubits that take part in each error-spreading event are circled. Type A (black) and B (green) are auxiliary and data qubit pairs for X- and Z-type stabilisers, respectively, that do not require additional qubits. Type C (purple) are auxiliary and additional qubit pairs for the top and left boundary X-type stabilisers. For these, we measure a weight-three stabiliser and, at the end of the QEC round, we measure out the additional qubits simultaneously with the auxiliary qubits.

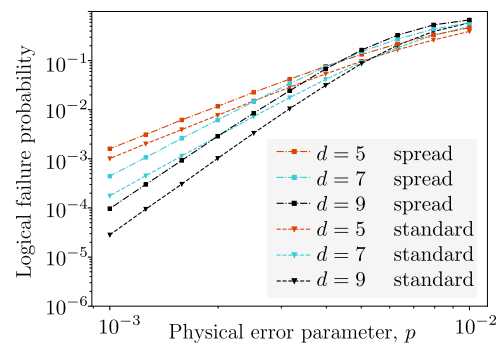


Fig. 10 | Quantum memory performance of rotated planar codes in the no-reset scheme using standard (triangles and dashed lines) and error-spreading (squares and dash-dotted lines) circuits. For each distance $d = 5, 7, 9$ (corresponding to red, blue, black colours), we performed d QEC rounds.

see from the stability time overhead plots Fig. 11b, we need fewer QEC rounds for the error-spreading circuit to avoid undetectable time-like logical failures and so we need fewer QEC rounds for quantum memory as well, making the gap in Fig. 10 smaller. For instance, in case of the 4×4 patch for $p = 0.001$, we have $R_{spr} \approx 0.85$, meaning we have to spend only 85% of the time on stabiliser measurements as with the standard no-reset circuits. Taking into account the differing execution times, we see that we need only $\approx 80\%$ of the number of QEC rounds with the error-spreading circuit. Based on this, we can conclude that the error-spreading circuit improves the QEC performance over the standard no-reset circuits.

From comparing Figs. 11b and 6b, we can further conclude that the error-spreading circuit is a good alternative to unconditional reset if the reset duration exceeds 100 ns for the error regimes we considered. However, if the reset duration is decreased further, then unconditional reset outperforms the error-spreading circuit.

Recovering time-like distance by squeezing two QEC rounds into one

In this section, we show that QEC performance can be improved without using unconditional resets by effectively squeezing two QEC rounds into one. This method, however, requires $\approx 50\%$ additional qubits. We appoint

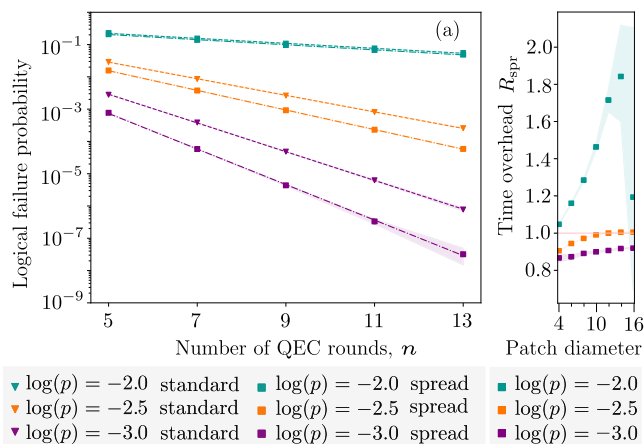


Fig. 11 | Comparison of stability experiment performances in the no-reset scheme using standard (triangles and dashed lines) and error-spreading (squares and dash-dotted lines) circuits. Colours indicate different physical error probabilities: $p = 10^{-2}$ (blue), $p = 10^{-2.5}$ (orange), $p = 10^{-3}$ (purple). **a** Comparison of logical failure probabilities for the 4×4 stability patch. Error bars as in Fig. 6(a) are also shown as shaded areas. Note that for the $p = 10^{-2}$ case, the two lines overlap. **b** The time overhead R_{spr} , that the error-spreading circuit requires when compared to the no-reset standard circuit. The shaded areas correspond to 90% confidence intervals. The conditional reset scheme is not shown as the simulation is identical to the no-reset except with higher noise levels due to the increased physical qubit idling. As a consequence, the conditional reset scheme will always perform worse and is therefore not shown here.

two auxiliary qubits for each stabiliser, as shown in Fig. 12a. Note that the auxiliary qubits of the X-/Z-type stabilisers are arranged horizontally/vertically so that we avoid so-called “bad hook” errors. Therefore, the hardware needs the Cairo pentagonal connectivity³⁶. The main idea is that while we measure the auxiliary qubits of one stabiliser type, we can execute unitary gates on the qubits of the other type and also have plenty of time to obtain two independent measurement outcomes for each stabiliser. Figure 12b, c illustrates this. For instance, the unitary parts of this circuit for a Z-type stabiliser are as follows. We use Roman numerals for qubit labels and numerical labels for protocol steps. First, apply two layers of CZ gates: step (1) $CZ_{i,iii}$ and $CZ_{ii,iv}$; then step (2) $CZ_{i,v}$ and $CZ_{ii,vi}$. Then, swap the auxiliary qubits, so step (3) $SWAP_{i,ii}$. Finally, repeat the two layers of CZ gates: step (5) $CZ_{i,iii}$ and $CZ_{ii,iv}$; then step (6) $CZ_{i,v}$ and $CZ_{ii,vi}$. In this way, we entangle the two auxiliary qubits with the data qubits independently and so measuring each provides independent stabiliser measurements. Since executing these unitary gates takes only 400 ns in total (when compiled to the gates of Table 1), one QEC round with this circuit takes 1000 ns. This is only 160 ns longer than for the standard no-reset syndrome extraction; however, we obtain each stabiliser outcome twice.

We now show how this new circuit recovers the effective time-like distance. First, we define the detectors. For each stabiliser g , let (x^1, y^1) and (x^2, y^2) be the spatial coordinates of its two auxiliary qubits. For the sake of simplicity, we will consider outcomes in the conditional-reset scheme, which is equivalent to the no-reset scheme. Denote by $m_{g,j}^k$ the outcome in the j th QEC round obtained on the auxiliary qubit at (x^k, y^k) ($k = 1, 2$). We set $m_{g,j}^1 \oplus m_{g,j}^2$ as a detector for all j and assign the coordinates (x^1, y^1, j) to it. Furthermore, in the bulk of the experiment, we define $m_{g,j}^1 \oplus m_{g,j+1}^1$ as a detector if j is even, and $m_{g,j}^2 \oplus m_{g,j+1}^2$ when j is odd, and assign the coordinates $(x^2, y^2, j + \frac{1}{2})$ to it. The full decoding graph of a stability experiment on a 4×4 patch with 5 rounds is available in³¹. Figure 13 depicts the part of the decoding graph where only nodes (detectors) corresponding to one X-type stabiliser are shown. This restricted graph has edges of two types: diagonal and vertical edges. If $m_{g,j}^k$ ($k \in \{1, 2\}$) is flipped due to a quantum bit-flip measurement error, then at most two detectors are triggered, namely

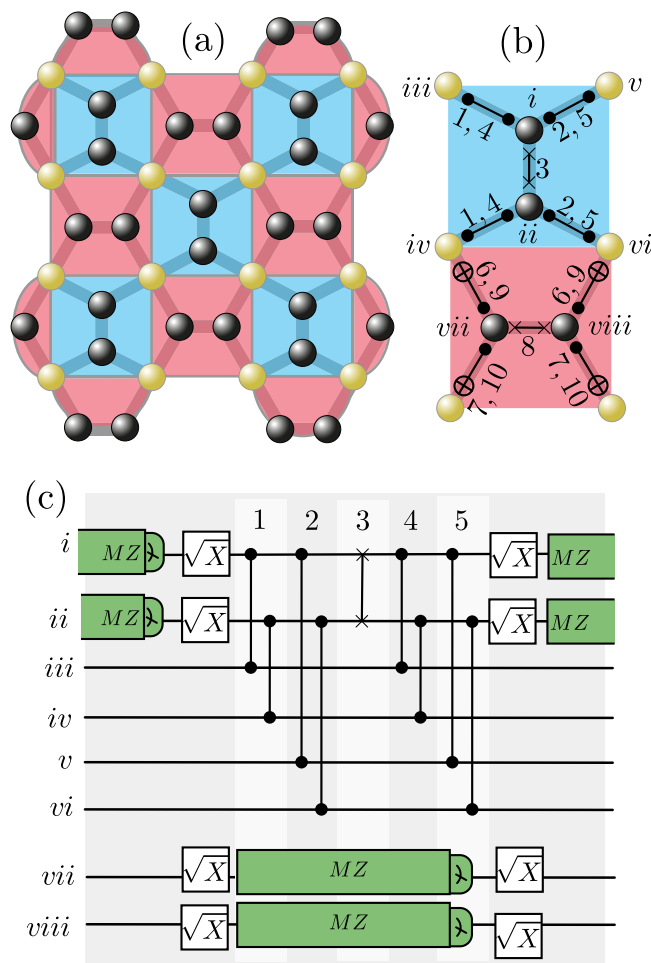


Fig. 12 | Round-squeezing circuit. **a** 4×4 stability patch (cf. Fig. 1b) for the round-squeezing circuit implementation laid out on the Cairo pentagonal connectivity that avoids “bad hooks”. Each stabiliser has two auxiliary qubits as shown. **b** Graphical representation of the round-squeezing circuit for two adjacent stabilisers. In steps 1–5, we apply CZ and SWAP two-qubit gates for the Z-type stabiliser as shown, during which we measure the auxiliary qubits of the X-stabiliser. Then, in steps 6–10, we apply CX and SWAP two-qubit gates for the X-type stabiliser and, at the same time, measure the auxiliary qubits of the Z-type stabiliser. In the bulk of the experiment, we repeat this. In this way, the execution time of the round-squeezing circuit for the same number of QEC rounds is only slightly increased compared to the standard circuit’s execution time with no reset, and is shorter than the execution time of standard circuits with unconditional reset, provided the reset duration is >160 ns. **c** Circuit diagram of steps 1–5.

at coordinates (x^1, y^1, j) and $(x^2, y^2, j \pm \frac{1}{2})$, corresponding to a diagonal edge. If $m_{g,j}^k$ ($k \in \{1, 2\}$) is flipped due to misclassification, the most dangerous error for FTQC, then that will also flip $m_{g,j+1}^{3-k}$, hence triggers at most four detectors. However this can be decomposed into two parallel diagonal edges. To account for the vertical edges, consider an XX -error occurring after the SWAP gate in Fig. 12b. This error flips both outcomes of the j th QEC round, hence triggers at most two detectors at coordinates $(x^2, y^2, j - \frac{1}{2})$ and $(x^2, y^2, j + \frac{1}{2})$ – a vertical edge. We verified using `stim`’s functionality that the effective distance of stability experiments is recovered to be n . Furthermore, the effective distance for quantum memory remains the same as with standard syndrome extraction circuits: d .

We simulated these circuits in order to compare the performance to the previously discussed syndrome extraction circuits. We applied the same principles for the number of shots as in the previous two subsections. We present the quantum memory results in Fig. 14 and see that again the

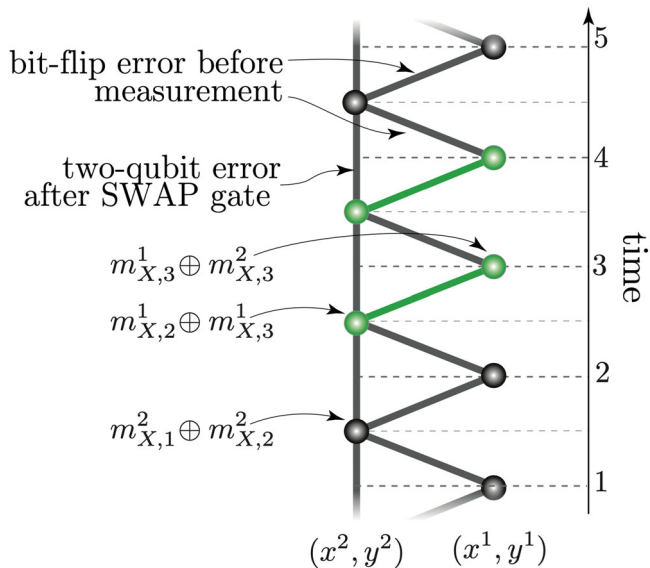


Fig. 13 | Part of the decoding graph for a stability experiment with the round-squeezing circuit that only contains nodes associated with one X-type stabiliser. A quantum bit-flip error before measurement corresponds to a diagonal edge, while an XX -error on the auxiliary qubits after the SWAP gate corresponds to a vertical edge. The measurement classification error triggers four detectors (green nodes) and can be decomposed into two diagonal edges (green edges).

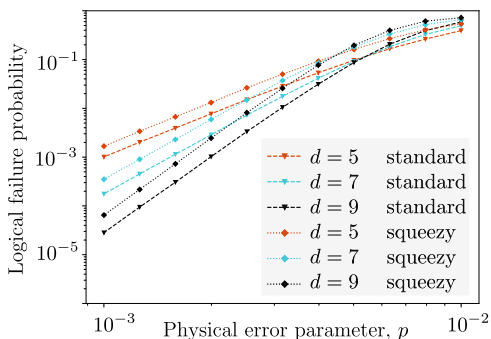


Fig. 14 | Comparison of quantum memory performances in the no-reset scheme using standard (triangles and dashed lines) and round-squeezing (diamonds and dotted lines) circuits. For each distance $d = 5, 7, 9$ (corresponding to red, blue, black colours), we performed d QEC rounds.

performance is slightly diminished from the standard no-reset case, though not as much as with the error-spreading circuits. We attribute this to the increased number of two-qubit gates used in these syndrome extraction circuits. However, as we see from the stability time overhead plots in Fig. 15b, we need fewer QEC rounds for the round-squeezing circuit to avoid undetectable time-like logical failures and so we need fewer QEC rounds for quantum memory as well, making the gap in Fig. 14 smaller. For instance, with $p = 0.001$ we have $R_{sqz} \approx 0.65$. Since execution times per QEC round differ, we need only $\approx 55\%$ of the number of QEC rounds with the round-squeezing circuit—slightly more than half as many as for the standard no-reset case. Based on this, we can conclude that this circuit improves on the QEC performance of both the standard and error-spreading no-reset circuits, though with the use of additional physical qubits.

From comparing Figs. 15b and 6b, we can further conclude that this circuit is a good alternative to implementing unconditional resets, even with instantaneous reset, at least for the range of physical error parameters we consider. We expect that, with much lower physical error probability, this would no longer be the case.

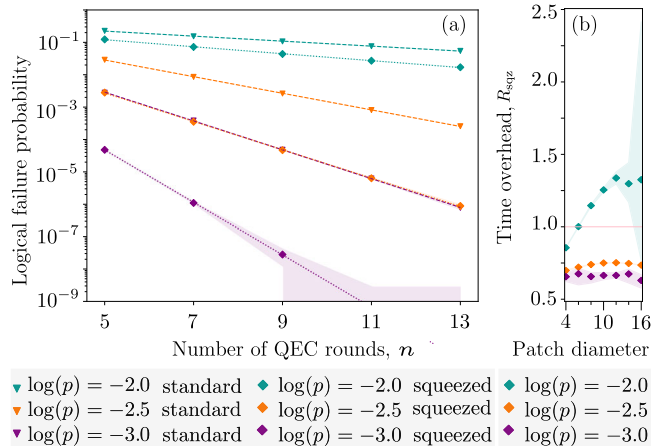


Fig. 15 | Comparison of stability experiment performances in the no-reset scheme using standard (triangles and dashed lines) and round-squeezing (diamonds and dotted lines) circuits. Colours indicate different physical error probabilities: $p = 10^{-2}$ (blue), $p = 10^{-2.5}$ (orange), $p = 10^{-3}$ (purple). **a** Comparison of logical failure probabilities for a 4×4 stability patch. Error bars as in Fig. 6a are also shown as shaded areas. Note that the standard $p = 10^{-3}$ and round-squeezing $p = 10^{-2.5}$ plots overlap. **b** The time overhead R_{sqz} that the round-squeezing circuit requires when compared to the no-reset standard circuit. The shaded areas correspond to 90% confidence intervals.

Whilst no device with the connectivity shown in Fig. 12a currently exists, it has lower connectivity than many current devices suggesting it should be easier to build. However, we point out that using an additional SWAP layer on one stabiliser type, it is possible to align the auxiliary qubits in a parallel direction without introducing “bad hooks”³⁷. In this case, the required connectivity is a sub-graph of the popular square-grid connectivity.

Discussion

We investigated the QEC consequences of performing mid-circuit reset, or not, during QEC experiments using standard syndrome extraction circuits. Our main conclusion is that unconditionally resetting qubits, for instance by driving interactions with a dissipative environment, fundamentally improves the fault-tolerance properties of logical operations offering up-to $2 \times$ speedup of fault-tolerant quantum computers. Access to fast, high-fidelity unconditional resets would make this approach a clear winner.

Nevertheless, with current best-in-class devices operating close to the QEC threshold and focused more on memory experiments, our simulations indicated that not resetting qubits can result in better performance. This justifies the approach taken in recent proof-of-principle experiments^{6,8} and offers encouragement for near-term experiments to continue this practice. For those keen to avoid developing unconditional-reset technology, we presented two alternative syndrome extraction circuits that provide additional protection against measurement errors. These alternative circuits are interesting near-term experiments and potential long-term solutions. Whether our alternative circuits are genuine contenders for the best approach to FTQC will depend on additional effects, such as leakage errors, not considered in this paper. Such investigation would be interesting future work.

Furthermore, we emphasise again that our results are based on a particular noise model which assumes, for example, the measurement classification and qubit bit-flip error rates are 20% and 80% of the total measurement error rate, respectively. A direction for future work could be to repeat the analysis with different noise models or obtain results from real quantum computers. In particular, varying the measurement time on a particular device could affect results, not just by changing the amount of idling error on other qubits, but also by altering the total measurement error and the above split into classification and qubit bit-flip error.

Table 2 | Summary of the best-performing scheme(s) in different regimes based on our circuit-level noise simulations

Physical error probability	Reset speed	Suggested scheme to use
High	Fast	No reset
	Slow or not available	No reset
Medium	Fast	Unconditional reset, error-spreading or round-squeezing
	Slow or not available	Error-spreading or round-squeezing
Low	Fast	Unconditional reset
	Slow or not available	Error-spreading or round-squeezing

This can be used to help decide which scheme to use for FTQC. For the 'Physical error probability' column, 'high' corresponds to $p \approx 10^{-2}$, 'medium' to $p \approx 10^{-2.5}$ and 'low' to $p \lesssim 10^{-3}$. In the 'Reset speed' column, 'fast' corresponds to ≈ 100 ns and 'slow' to ≈ 500 ns.

As for the third class of reset strategy, conditional reset, our analysis shows that it will never compete with other strategies, and so should not be used in any of the QEC experiments considered here. This observation debunks folklore claims that control systems for QEC require fast conditional reset.

A summary of our results can be found in Table 2, where we present the best-performing scheme in different regimes based on our circuit-level noise simulations. This table can be used to help decide which scheme to use for FTQC.

Data availability

Data generated in the course of this work can be made available upon reasonable request.

Code availability

Circuits that were used for simulations are available in³¹.

Received: 5 September 2024; Accepted: 21 February 2025;

Published online: 07 March 2025

References

- Nielsen, M. A. & Chuang, I. L. *Quantum Computation and Quantum Information: 10th Anniversary Edition* (Cambridge University Press, 2010).
- DiVincenzo, D. P. The physical implementation of quantum computation. *Progr. Phys. Fortschr. Phys.* **48**, 771–783 (2000).
- Magnard, P. et al. Fast and unconditional all-microwave reset of a superconducting qubit. *Phys. Rev. Lett.* **121**, 060502 (2018).
- Zhou, Y. et al. Rapid and unconditional parametric reset protocol for tunable superconducting qubits. *Nat. Commun.* **12**, 5924 (2021).
- Córcoles, A. D. et al. Exploiting dynamic quantum circuits in a quantum algorithm with superconducting qubits. *Phys. Rev. Lett.* **127**, 100501 (2021).
- Ali, H. et al. Reducing the error rate of a superconducting logical qubit using analog readout information. *Phys. Rev. Appl.* **22**, 044031 (2024).
- Marques, J. F. et al. Logical-qubit operations in an error-detecting surface code. *Nat. Phys.* **18**, 80–86 (2022).
- Krinner, S. et al. Realizing repeated quantum error correction in a distance-three surface code. *Nature* **605**, 669–674 (2022).
- Campbell, E. A series of fast-paced advances in quantum error correction. *Nat. Rev. Phys.* **6**, 160–161 (2024).
- Bluvstein, D. et al. Logical quantum processor based on reconfigurable atom arrays. *Nature* **626**, 58–65 (2024).
- Ryan-Anderson, C. et al. Implementing fault-tolerant entangling gates on the five-qubit code and the color code. *arXiv* <https://arxiv.org/abs/2208.01863> (2022).
- Menendez, D., Ray, A. & Vasmer, M. Implementing fault-tolerant non-clifford gates using the $[[8,3,2]]$ color code. *arXiv* <https://arxiv.org/abs/2309.08663> (2023).
- Miao, K. C. et al. Overcoming leakage in scalable quantum error correction. *Nat. Phys.* **19**, 1780–1786 (2023).
- Acharya, R. et al. Suppressing quantum errors by scaling a surface code logical qubit. *Nature* **614**, 676–681 (2023).
- Horsman, D., Fowler, A. G., Devitt, S. & Van Meter, R. Surface code quantum computing by lattice surgery. *N. J. Phys.* **14**, 123011 (2012).
- Litinski, D. A game of surface codes: Large-scale quantum computing with lattice surgery. *Quantum* **3**, 128 (2019).
- Chamberland, C. & Campbell, E. T. Universal quantum computing with twist-free and temporally encoded lattice surgery. *PRX Quantum* **3**, 010331 (2022).
- Chamberland, C. & Campbell, E. T. Circuit-level protocol and analysis for twist-based lattice surgery. *Phys. Rev. Res.* **4**, 023090 (2022).
- Bombin, H. et al. Logical blocks for fault-tolerant topological quantum computation. *PRX Quantum* **4**, 020303 (2023).
- Gehér, G. P. et al. Error-corrected Hadamard gate simulated at the circuit level. *Quantum* **8**, 1394 (2024).
- Gidney, C. Stability experiments: The overlooked dual of memory experiments. *Quantum* **6**, 786 (2022).
- Chao, R. & Reichardt, B. W. Flag fault-tolerant error correction for any stabilizer code. *PRX Quantum* **1**, 010302 (2020).
- McEwen, M., Bacon, D. & Gidney, C. Relaxing hardware requirements for surface code circuits using time-dynamics. *Quantum* **7**, 1172 (2023).
- Dennis, E., Kitaev, A., Landahl, A. & Preskill, J. Topological quantum memory. *J. Math. Phys.* **43**, 4452–4505 (2002).
- Higgott, O. & Gidney, C. Sparse blossom: correcting a million errors per core second with minimum-weight matching. *arXiv:2303.15933* (2023).
- Varbanov, B. M. et al. Leakage detection for a transmon-based surface code. *npj Quantum Inf.* **6**, 102 (2020).
- Sahay, K., Lin, Y., Huang, S., Brown, K. R. & Puri, S. Error correction of transversal cnot gates for scalable surface code computation. *arXiv preprint arXiv:2408.01393* (2024).
- Wan, K. H., Webber, M., Fowler, A. G. & Hensinger, W. K. An iterative transversal cnot decoder. *arXiv preprint arXiv:2407.20976* (2024).
- Zhou, H. et al. Algorithmic fault tolerance for fast quantum computing. *arXiv preprint arXiv:2406.17653* (2024).
- Rigetti Systems. <https://qcs.rigetti.com/qpus> (2023). Accessed: 01/07/2023.
- Gehér, G. P., Jastrzebski, M., Campbell, E. T. & Crawford, O. Stim circuits for "To reset, or not to reset – that is the question" manuscript (2024).
- Gidney, C., Newman, M., Fowler, A. & Broughton, M. A fault-tolerant honeycomb memory. *Quantum* **5**, 605 (2021).
- Sarvepalli, P. K., Klappenecker, A. & Rötteler, M. Asymmetric quantum codes: Constructions, bounds and performance. *Proc. R. Soc. A: Math., Phys. Eng. Sci.* **465**, 1645–1672 (2009).
- Gidney, C. Stim: a fast stabilizer circuit simulator. *Quantum* **5**, 497 (2021).
- Gehér, G. P., Crawford, O. & Campbell, E. T. Tangling schedules eases hardware connectivity requirements for quantum error correction. *PRX Quantum* **5**, 010348 (2024).

36. Gidney, C. A pair measurement surface code on pentagons. *Quantum* **7**, 1156 (2023).
37. Hetényi, B. & Wootton, J. R. Tailoring quantum error correction to spin qubits. *Phys. Rev. A* **109**, 032433 (2024).

Author contributions

O.C. and G.P.G. identified the distance-halving effect of the no-reset and conditional-reset schemes for logical computation. G.P.G., O.C. and E.T.C. contributed to novel syndrome extraction circuit design. G.P.G., O.C., and M.J. implemented the circuits; G.P.G. and M.J. performed simulations. G.P.G. lead the project. O.C. and E.T.C. provided input on the project direction. G.P.G. lead the writing process with all four authors contributing.

Competing interests

The authors declare no competing interests.

Additional information

Correspondence and requests for materials should be addressed to György P. Gehér.

Reprints and permissions information is available at <http://www.nature.com/reprints>

Publisher's note Springer Nature remains neutral with regard to jurisdictional claims in published maps and institutional affiliations.

Open Access This article is licensed under a Creative Commons Attribution-NonCommercial-NoDerivatives 4.0 International License, which permits any non-commercial use, sharing, distribution and reproduction in any medium or format, as long as you give appropriate credit to the original author(s) and the source, provide a link to the Creative Commons licence, and indicate if you modified the licensed material. You do not have permission under this licence to share adapted material derived from this article or parts of it. The images or other third party material in this article are included in the article's Creative Commons licence, unless indicated otherwise in a credit line to the material. If material is not included in the article's Creative Commons licence and your intended use is not permitted by statutory regulation or exceeds the permitted use, you will need to obtain permission directly from the copyright holder. To view a copy of this licence, visit <http://creativecommons.org/licenses/by-nc-nd/4.0/>.

© The Author(s) 2025