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Evaluation of a 3 kV Polarization Superjunction GaN HEMT

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Abstract

Gallium Nitride (GaN) offers unique material properties making it more suitable for high frequency, high voltage, power dense applications. Our GaN devices benefit from high density polarization charges of 2DEG and 2DHG, which coexist in respective heterojunctions of a double heterostructure to form a charge balanced, polarization based super junction (PSJ). This capability enables design of area efficient, scalable, high performance transistors and diodes. This paper demonstrates a large area, 3 kV PSJ GaN high electron mobility transistor (HEMT) fabricated on sapphire. The device characteristics, working principle and switching performance are experimentally investigated. The device shows a low on-state resistance of 210 mΩ at 25˚C. At elevated operating temperatures, it can be observed that the turn-off switching losses are not affected while the turn-on losses show a small increase. Also, a wide range of dV/dt controllability can be achieved through intelligent control of gate without significant increase in losses to meet various application requirements.

1 Introduction

In recent years, GaN based devices have gained significant popularity and market acceptance due to their superior material characteristics compared to conventional silicon (Si). GaN offers a wide bandgap of 3.4 eV, a high critical electric field of 3.3 MV cm^{-1} and high electron mobility which facilitates construction of high voltage, low resistance diodes and transistors capable of operating at high frequencies and temperatures [1,2]. Such properties are ideal for power dense efficient power electronics of the future [3,4]. The high frequency characteristic of GaN HEMTs is key to achieve high power density power conversions as the size of passive components shrink at high frequency.[1][5-7]. GaN has already established its commercial success in lighting, power supplies and radio frequency applications. However, the development of high voltage devices has been hindered by a few factors [1]; One of the key challenges in fabrication of high voltage GaN power transistors and diodes is the management of electric fields under off-state conditions. Conventional lateral GaN HEMTs utilize several field plates and sophisticated processing to manage field crowding, which adds to manufacturing overheads [1][8,9]. Furthermore, these devices use cheaply available Si as substrate material for epitaxial growth of GaN layers, which limits the performances. Moreover, thick GaN transition and buffer layers are required for high voltage devices to account for lattice mismatch and prevent vertical breakdown [1]. Sapphire substrates, on the other hand, offer insulating and cost-effective thin GaN layer solutions to achieve high voltage capability, particularly in the form of PSJ technology [2]. PSJ devices work on a similar manner to conventional superjunction (SJ) which is based on the precise control of charges through impurity doping methods. However, in the PSJ concept, the charge balance is achieved due to the coexistence of positive and negative polarization charges in a double heterojunction formed by GaN/AlGaN/GaN layers [8]. Therefore, a uniform distribution of electric field is realized in PSJ devices with minimum drift region length in such a way that these devices can offer performance beyond the one-dimensional material limits [10]. GaN HEMTs often show very high dV/dt switching transitions which is beneficial in reducing switching losses [3]. However, they typically offer limited controllability which can limit their use in applications such as motor drives where dV/dt needs to be limited to prevent damage and adhere to EMI requirements [11-15]. Also, the sharp switching edges of GaN can result in unavoidable oscillatory behavior due to presence of stray inductances in circuit layout and packing [7]. Therefore, a comprehensive understanding of their switching behavior is essential to fully take advantage of their performance. In this paper, a large area, 3 kV GaN PSJ HEMT fabricated on sapphire is

demonstrated for the first time. The device characteristics, working principle and switching behavior are experimentally investigated and the results are discussed in detail. The effect of temperature on switching characteristics and power losses are also analyzed.

2 Operating Physics and Characteristics

2.1 Polarization Superjunction

SJ in Si was the key to realize high voltage, low resistance devices which works on the basis of charge balance within the drift region to minimize its width. PSJ devices work on a similar principle to conventional SJ [16]. The main difference is that the charge balance is originated from polarization based charges in the two dimensional electron gas (2DEG) and two dimensional hole gas (2DHG) which are formed at their respective interface within a double heterojunction (GaN/AlGaN/GaN) [5,17].

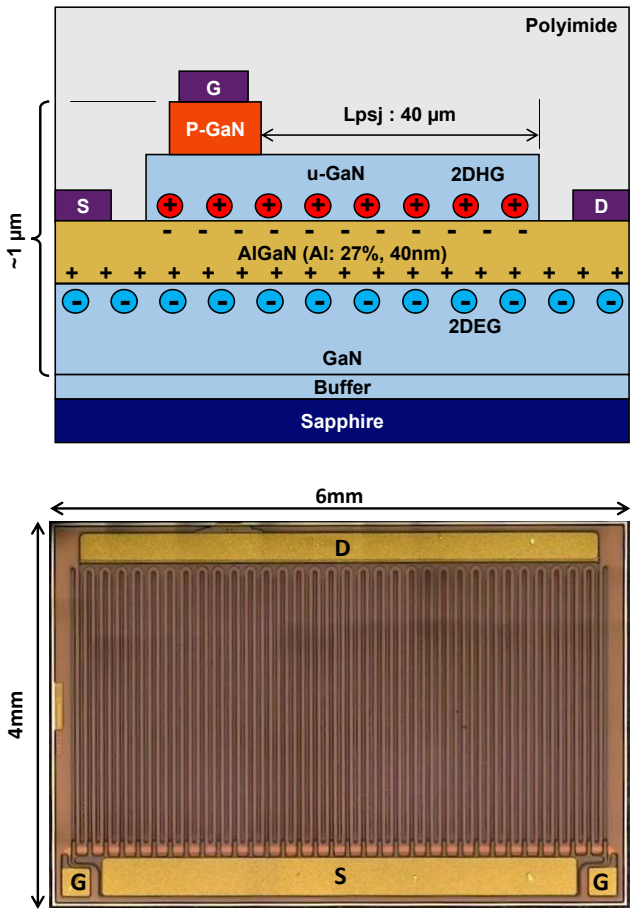

Fig. 1 Cross-sectional view of the device and top view of a 3 kV GaN PSJ HEMT chip. Gate, drain, and source are marked as G, D and S respectively.

In previous works, it has been demonstrated that breakdown voltage can be enhanced with a small increase in on-state resistance by extending the gate-drain distance (L_{PSJ}) [1]. Figure 1 illustrates a typical cross-sectional diagram of a depletion mode (d-mode) 3 kV GaN PSJ HEMT along with a top view of a chip.

The number of fingers connected to the drain, and source terminals are 33 and 34 respectively. The presence of the 2DEG provides a channel for current flow in the absence of gate bias (V_{GS} = 0 V) resulting in a normally on d-mode operation. The threshold voltage depends upon the thickness of the AlGaN layer. Once a negative gate bias larger than the threshold voltage of -4.9 V is applied, the device enters its blocking state. The p-GaN gate provides an ohmic contact to the 2DHG which facilitates injection or extraction of holes for collapse free operation. A positive gate bias can be applied to reduce the on-state resistance by attracting additional electrons beneath the 2DHG. Application of positive gate bias is restricted by two p-n junction diodes that are formed between (1) gate-drain (D_{GD}) and (2) gate-source (D_{GS}) which limits the positive gate drive voltage to around ~3.5 V. Exceeding this limit leads to excessive gate current injection that can lead to degradation.

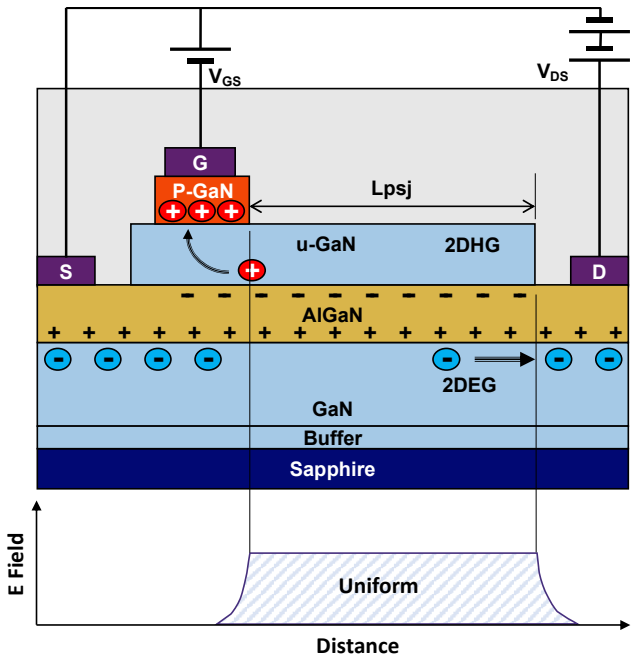

Fig. 2 Cross-sectional view of the GaN PSJ HEMT under off-state condition.

In the off state, the 2DHG and 2DEG are depleted through the gate and drain terminals respectively as depicted in Fig. 2. Consequently, a charge balance state is achieved which results in a uniform distribution of electric field over the drift

region length (L_{PSJ}). This mechanism has enabled the design of high voltage GaN devices with a prospective of up to 10 kV blocking capability [18]. The device does not have a body diode and the reverse conduction can be facilitated through the 2DEG or an external GaN diode [4].

2.2 Current Voltage Characteristics

The measured output I-V characteristics of the 3 kV GaN PSJ HEMT at 25˚C are presented in Fig. 3. The measurements were carried out under pulse mode to avoid self-heating.

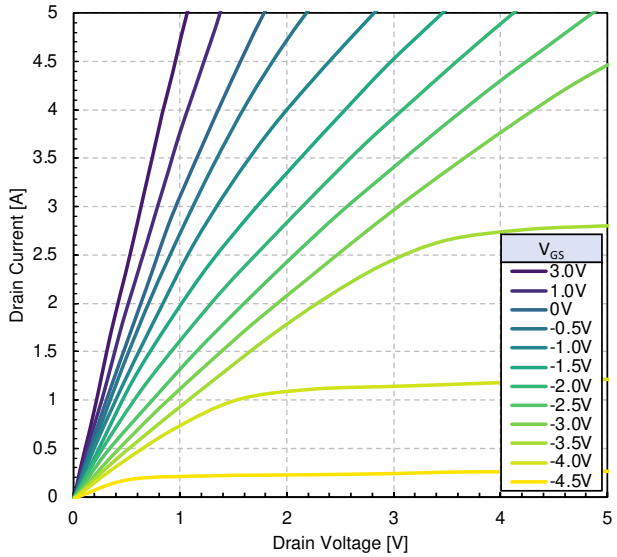

Fig. 3 Measured output characteristics of the 3 kV GaN PSJ HEMT at 25˚C and pulse width of 250 µs.

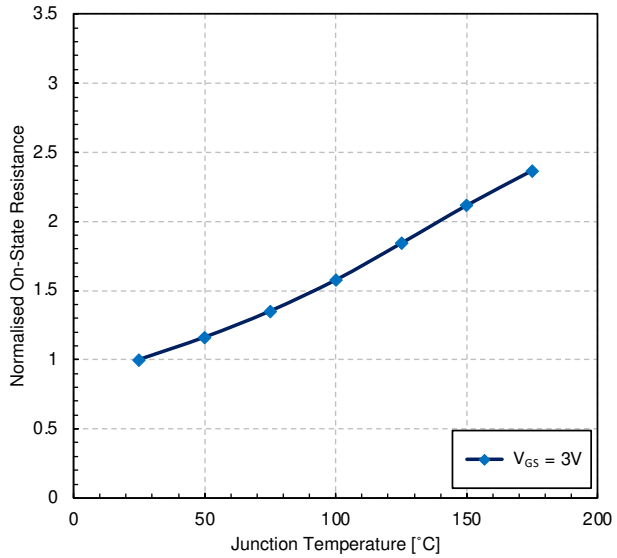

Fig. 4 Normalized on-state resistance versus temperature.

The on-state resistance of the device at room temperature corresponds to 210 mΩ and 305 mΩ at the gate voltage of 3 V and 0 V respectively. The on-state resistance of the device was extracted from the measured I-V characteristics at different junction temperatures as shown Fig. 4.

The device exhibits a positive temperature coefficient of on-state resistance which facilitates even distribution of current sharing between paralleled devices without the risk of thermal runaway. The transfer characteristics were measured at drain voltage of 10 V and at different temperatures as shown in Fig. 5.

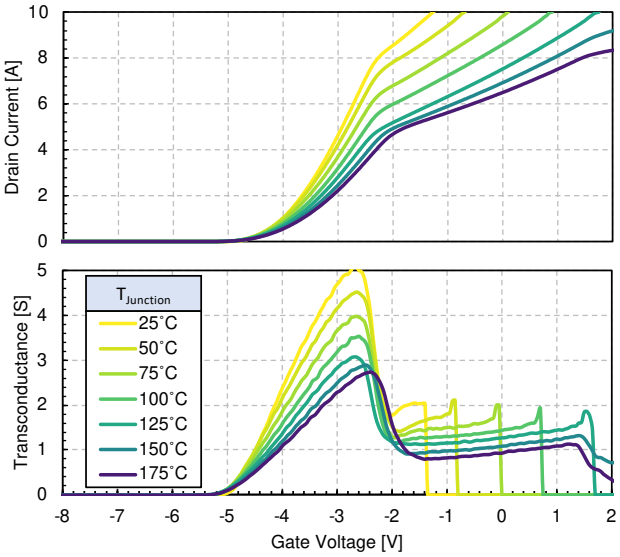

Fig. 5 Measured transfer characteristics of the 3 kV GaN PSJ HEMT at 25˚C. The drain voltage is at 10 V, and the compliance current is set at 10 A.

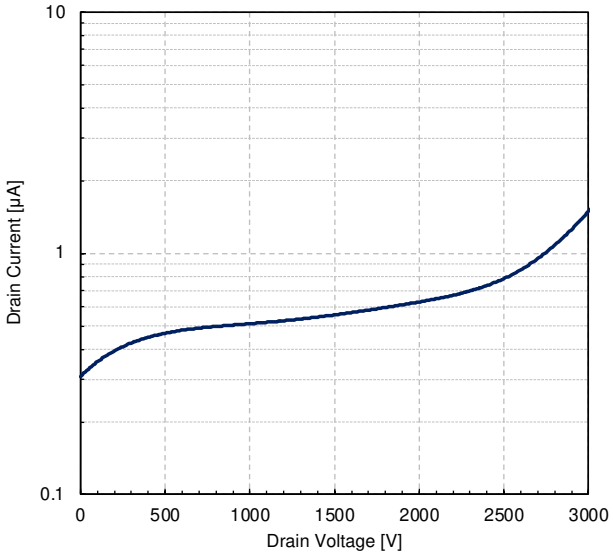

Fig. 6 Measured off-state I-V characteristics. The gate voltage is -10 V. The maximum drain voltage is limited by the instrument.

The slope of the transfer curves indicates the transconductance g_m which can be seen to decrease at higher temperatures. A threshold voltage of -4.9 V was extracted at drain voltage of 1 V and current of 1mA at room temperature. The threshold voltage rises by only ~6 % at 175˚C which indicates high switching stability.
The off-state leakage current was measured at RT as illustrated in Fig. 6. The drift region to support 3 kV is 40 µm as shown previously in Fig. 1. The leakage current is 1 µA at 3 kV at 25˚C. This is particularly important in high voltage devices to have low leakage current.

2.3 Dynamic On-State Resistance

One of the challenges in the development of power GaN devices, is the presence of dynamic on-state resistance (dynamic R_{dson}) which occurs due to current collapse phenomena [6]. The increase in resistance is attributed to electrons that are trapped near the channel which deplete the 2DEG causing its resistance to increase [6]. This is particularly problematic if high electric field peaks are present [19]. In GaN PSJ devices, current collapse is suppressed by the effective use of the p-GaN to inject or extract holes into the 2DHG which results in a uniform distribution of electric field. Figure 7 illustrates variation in the dynamic resistance as a function of applied voltage.

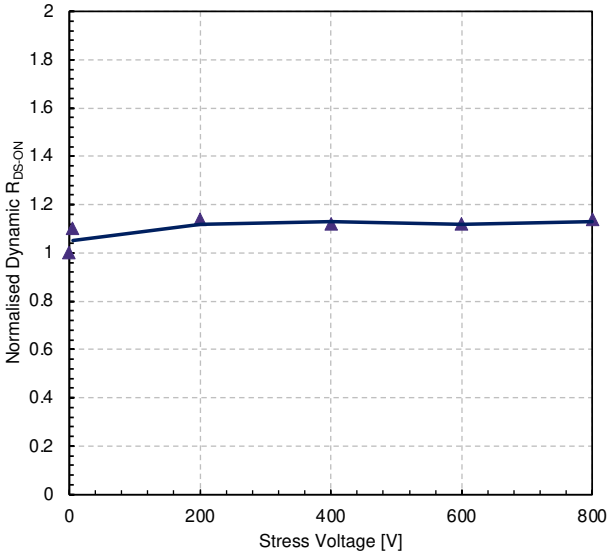

Fig. 7 Typical dynamic on-state resistance as function of applied stress voltage. The stress period is 10 s.

It can be observed that the on-state resistance does not change significantly with the applied voltage. This is because the electric field spreads evenly across the drift region.

2.4 Capacitance Characteristics

The input (C_{ISS}), output (C_{OSS}) and reverse transfer (C_{RSS}) capacitances of the device were measured using an Agilent B1505 power device analyzer at 1 MHz as shown in Fig. 8.

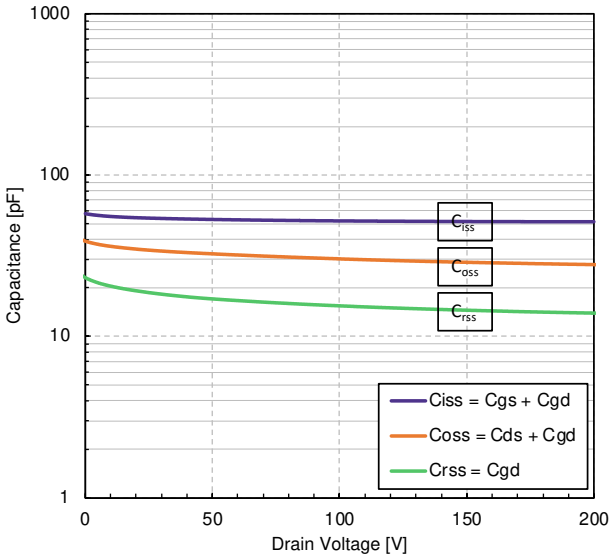

Fig. 8 Measured capacitance versus drain voltage measured at 1 MHz. The gate voltage is -20 V.

Amongst these capacitances, the gate-drain capacitance (C_{GD} = C_{RSS}) determines the switching speed as given by Eq. (1)

$$\frac{dV_{DS}}{dt} = \frac{I_G}{C_{GD}} = \frac{V_{GS}}{R_G.C_{GD}} \qquad (1)$$

In GaN PSJ HEMTs, C_{GD} originates from the overlap of the 2DEG and 2DHG which is optimized for dV/dt controllability [3].

3 Experiment

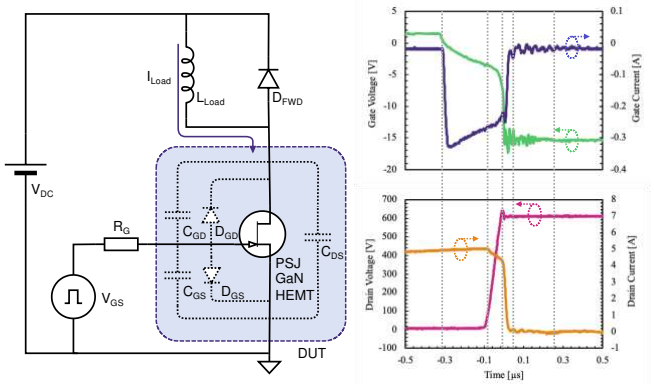

Fig. 9 Experimental setup and typical turn-off switching waveforms [3].

The switching performance was evaluated by a clamped inductive switching test (commonly referred to as double pulse test) set up as shown in Fig. 9. The switching voltage is limited by the measurement setup and safety considerations.

A 1.18 mH inductor is used as the load with a freewheeling SiC Schottky diode (D_{FWD}). The turn-off sequence can be described as follows; Initially, the gate-source capacitance (C_{GS}) is charged via the external gate resistor (R_G) by the gate driver (V_{GS}). In this period, the device is still on and carrying the full load current (I_D). The gate voltage is then maintained to keep the drain current flowing while the gate-drain capacitance (C_{GD}) begins to charge by the gate current (I_G). During this period, the drain voltage (V_{DS}) begins to climb to its final value set by the supply (V_{DC}) depleting the 2DEG and 2DHG. The slew rate is governed by the V_{GS} and R_G as given by Eq. (1). It should be noted that the C_{GD} decreases as the depletion expands. Once the V_{DS} is at supply voltage, the current starts to decrease and diverts to the D_{FWD}. Meanwhile, the V_{GS} continues to ascend to its final value set by the gate driver. An overshoot voltage occurs due to stray inductances as given by Eq. (2).

$$V_{Overshoot} = L_{Stray} \cdot \frac{dI_{Drain}}{dt} \qquad (2)$$

It is critical to reduce stray inductances to minimise the surge voltage. The turn-on sequence is essentially the same as the turn-off in backward sequence. During the switching period, energy is dissipated in the form of heat due to overlap of current and voltage as given by Eq. (3).

$$E_{SWT} = E_{On} + E_{Off} = \int V_{Drain} . I_{Drain}\, dt \qquad (3)$$

The integration is performed over the turn-on and turn-off transitions.

4 Switching Characteristics

4.1 Turn-Off dV/dt Controllability

The turn-off dV/dt is evaluated by analyzing the effect of gate drive parameters on switching slew rate as shown in Fig. 10. In this experiment, the switching voltage and current are set at 600 V and 5 A respectively. The rise time and dV/dt were extracted from the measured waveforms as shown in Fig. 11.

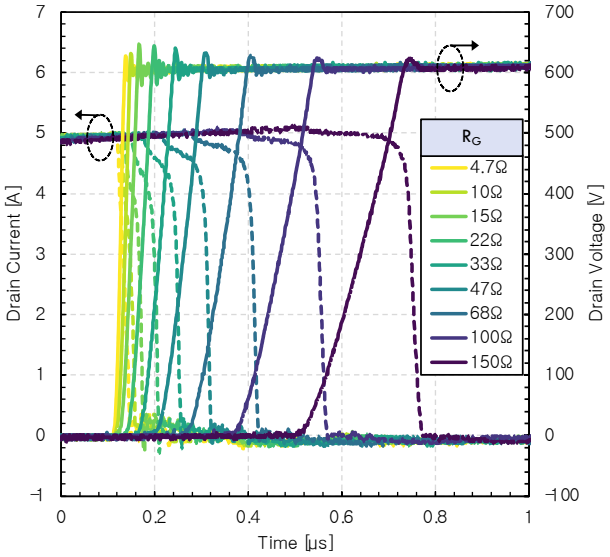

Fig. 10 Measured turn-off switching waveforms at different gate resistances and at 25˚C.

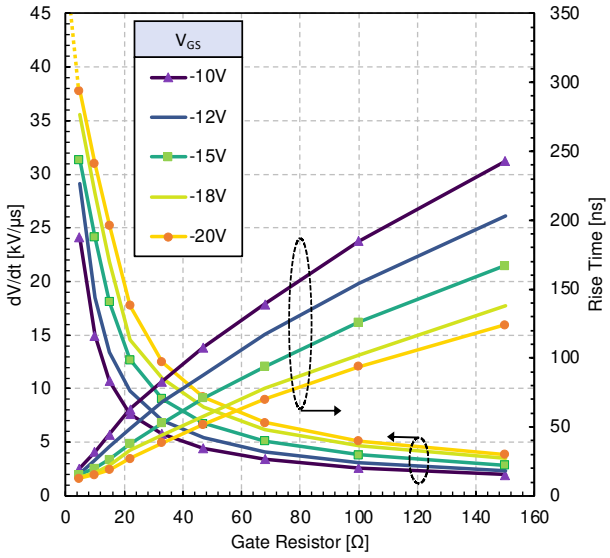

Fig. 11 Measured turn-off dV/dt and rise time at different gate resistances and gate voltages and at 25˚C.

It can be observed that the device can operate at a wide range of dV/dt values which can be adjusted by the gate voltage and gate resistance based on the application requirement. The turn-off switching energy losses were calculated as shown in Fig. 12.

The dissipated energy increases at higher gate resistances and lower gate voltages due to the lower slew rates and longer switching time. It should be noted that the dissipated energy is at least an order of magnitude lower than Si IGBTs counterparts.

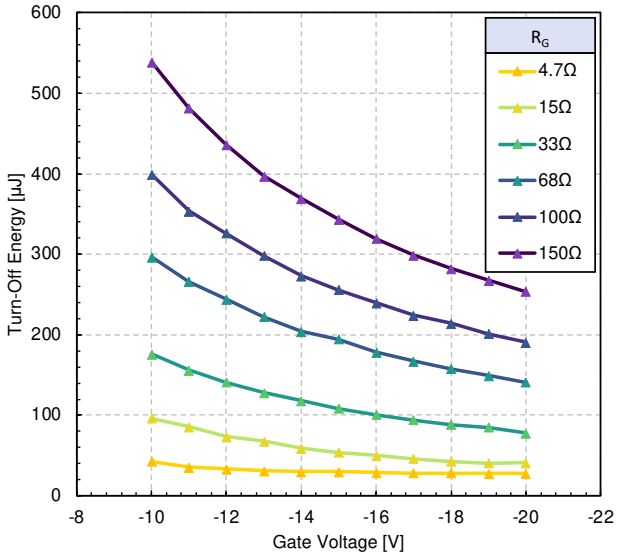

Fig. 12 Measured turn-off energy at different gate resistances and gate voltages and at 25˚C.

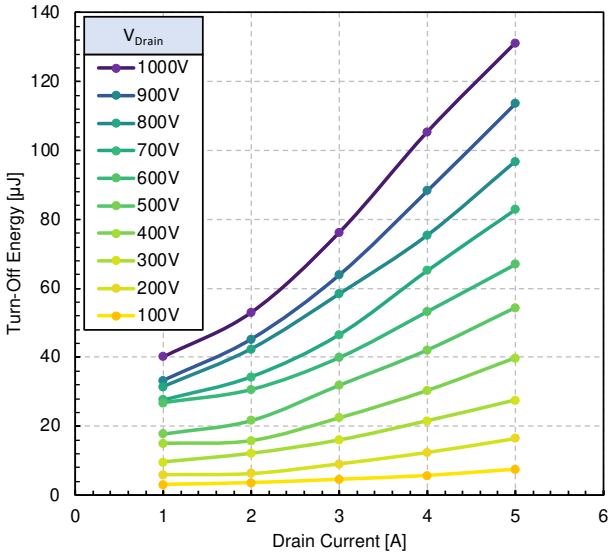

Fig. 14 Measured turn-off dissipated energy at various load currents and voltages and at 25˚C. R_G = 15 Ω and V_G = +2 V/-15 V.

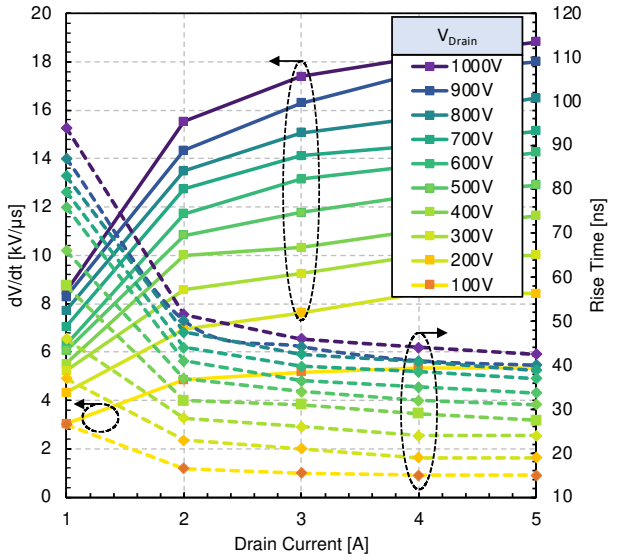

Fig. 13 Measured dV/dt and rise time as function of load current and voltage and at 25˚C. R_G = 15 Ω and V_G = +2 V/-15 V.

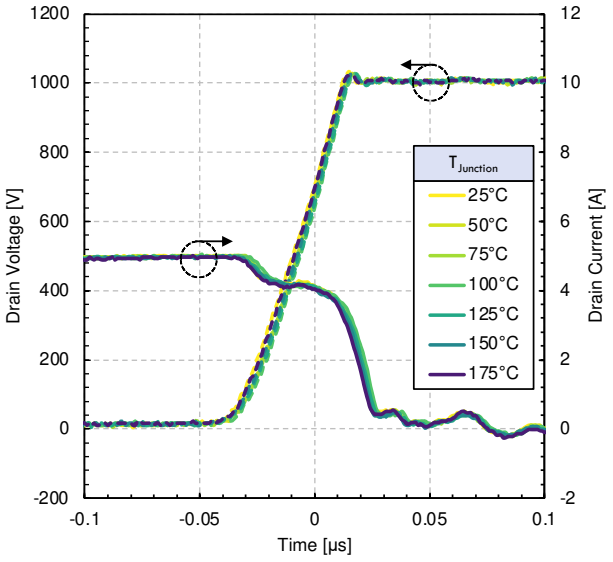

Fig. 15 Measured turn-off switching waveforms at different junction temperatures. R_G = 15 Ω and V_G = +2 V/-15 V.

4.2 Influence of Load current and Voltage on Turn-Off dV/dt

Figure 13 shows the influence of switching voltage and load current on dV/dt and rise time. The gate resistance is 15 Ω. While the switching voltage has a direct impact on switching speed, the incremental increase in dV/dt gets smaller at high voltage.

The corresponding energy losses at different voltages and currents are shown in Fig. 14.

4.3 Influence of Temperature and Load Current

Power semiconductor devices often are required to operate at elevated ambient temperatures. In this section, the influence of temperature on switching characteristics is evaluated. The turn-off and turn-on switching waveforms at different temperatures are presented in Fig. 15 and Fig. 16 respectively.

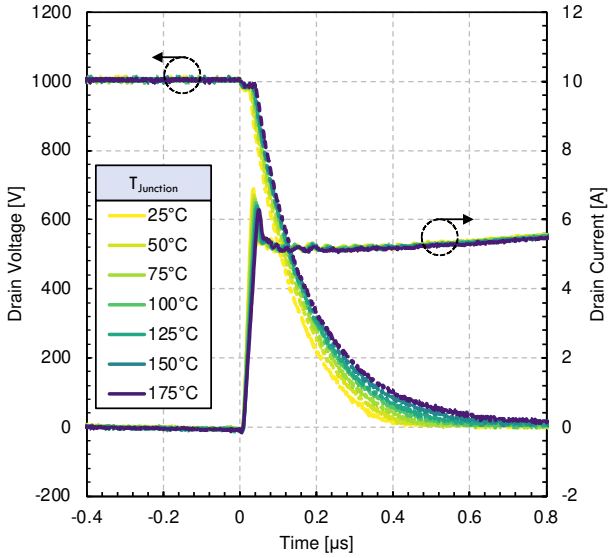

Fig. 16 Measured turn-on switching waveforms at different junction temperatures. R_G = 15 Ω and V_G = +2 V/-15 V.

It can be observed that the temperature has no significant effect on the turn-off switching performance. The turn-on, however, is affected by the temperature due to the changes in the transconductance which decreases at elevated temperatures as previously illustrated in Fig. 5. Figure 17 illustrates the voltage rise and fall time for turn-off and turn-on transients respectively at various temperatures. The corresponding switching energy losses were calculated separately for turn-on and turn-off as shown in Fig. 18.

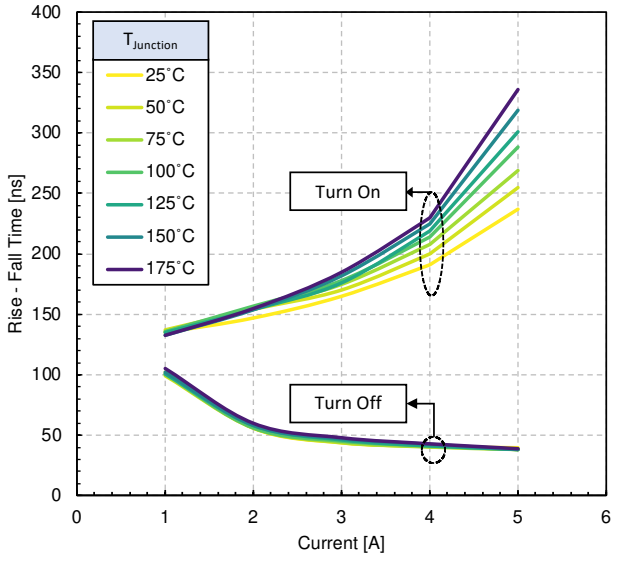

Fig. 17 Measured voltage rise (turn-off) and fall (turn-on) time at different current levels and junction temperatures.

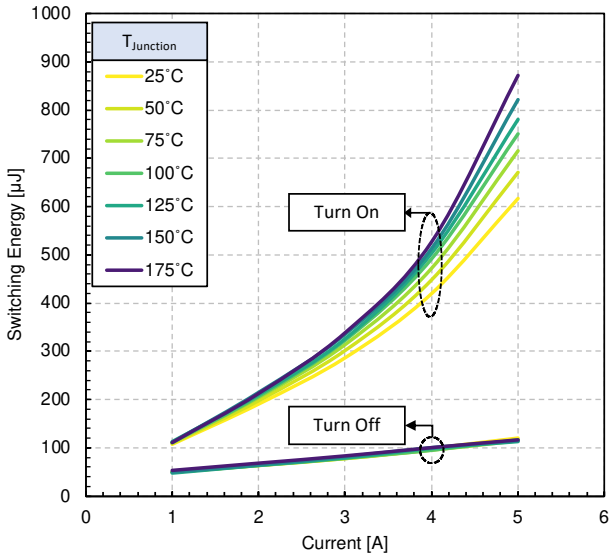

Fig. 18 Measured switching energy as a function of load current at different junction temperatures.

Due to slower transition of fall time at higher junction temperatures, the turn-on energy losses increase. The turn-off switching energy is almost constant regardless of the operating temperature. Overall, the results show potential benefits of GaN for high temperature applications.

5 Conclusion

In this paper, a large area, 3 kV PSJ GaN HEMT is demonstrated for the first time. The device characteristics, working mechanism and switching performance were investigated in detail. The device demonstrates a wide range of slew rates which can be adjusted through intelligent control of the gate resistance and gate voltage to fit various application requirements while maintaining a low power loss profile. The high temperature switching performance shows that the turn-off is effectively unaffected at elevated temperatures. The turn-on shows an increase in switching losses at higher operating temperature. Nevertheless, the losses are much lower than Si counterparts. The results are highly promising for the application of PSJ GaN technology in high voltage power electronic applications.

References

[1] H. Kawai, S. Yagi, S. Hirata, F. Nakamura, T. Saito, Y. Kamiyama, M. Yamamoto, H. Amano, V. Unni and E. M. S. Narayanan, “Low cost high voltage GaN polarization superjunction field effect transistors,”

Physica Status Solidi (a), vol. 214, no. 8, p. 1600834, 2017.

[2] "The 2018 GaN power electronics roadmap," *Journal of Physics D: Applied Physics,* vol. 51, no. 16, p. 163001, 2018.

[3] A. Sheikhan, E. M. S. Narayanan, H. Kawai, S. Yagi and H. Narui, "Evaluation of turn-off dV/dt controllability and switching characteristics of 1.2 kV GaN polarisation superjunction heterostructure field-effect transistors," *Japanese Journal of Applied Physics,* vol. 62, p. 064502, 2023.

[4] A. Sheikhan, G. Narayanankutty, E. M. S. Narayanan, H. Kawai, S. Yagi and H. Narui, "Analysis of 1.2 kV GaN polarisation superjunction diode surge current capability," *Japanese Journal of Applied Physics,* vol. 62, no. 1, p. 014501, 2023.

[5] A. Nakajima, Y. Sumida, M. H. Dhyani, H. Kawai and E. M. S. Narayanan, "High Density Two-Dimensional Hole Gas Induced by Negative Polarization at GaN/AlGaN Heterointerface," *Applied Physics Express,* vol. 3, no. 12, p. 121004, 2010.

[6] W. Saito, T. Nitta, Y. Kakiuchi, Y. Saito, K. Tsuda, I. Omura and M. Yamaguchi, "Suppression of Dynamic On-Resistance Increase and Gate Charge Measurements in High-Voltage GaN-HEMTs With Optimized Field-Plate Structure," *IEEE Transactions on Electron Devices,* vol. 54, no. 8, pp. 1825-1830, 2007.

[7] E. A. Jones, F. F. Wang and D. Costinett, "Review of Commercial GaN Power Devices and GaN-Based Converter Design Challenges," *IEEE Journal of Emerging and Selected Topics in Power Electronics,* vol. 4, no. 3, pp. 707 - 719, 2016.

[8] A. Nakajima, V. Unni, K. G. Menon, M. H. Dhyani, E. M. S. Narayanan, Y. Sumida and H. Kawai, "GaN-based Bidirectional Super HFETs Using Polarization Junction Concept on Insulator Substrate," in *International Symposium on Power Semiconductor Devices and ICs*, Bruges, 2012.

[9] V. Unni, H. Y. Long, H. Yan, A. Nakajima, H. Kawai and E. M. S. Narayanan, "Analysis of drain current saturation behaviour in GaN polarisation super junction HFETs," *IET Power Electronics,* vol. 11, no. 14, pp. 2198-2203, 2018.

[10] C. Hu, "Optimum doping profile for minimum ohmic resistance and high-breakdown voltage," *IEEE Transactions on Electron Devices ,* vol. 26, no. 3, pp. 243-244, 1979.

[11] H. Akagi, "Influence of high dv/dt switching on a motor drive system: a practical solution to EMI issues," in *International Symposium on Power Semiconductor Devices and ICs*, Kitakyushu, 2004.

[12] A. V. Jouanne and P. N. Enjeti, "Design Considerations for an Inverter Output Filter to Mitigate the Effects of Long Motor Leads in ASD Applications," in *Applied Power Electronics Conference*, San Jose, 1996.

[13] E. Persson, "Transient effects in application of PWM inverters to induction motors," *IEEE Transactions on Industry Applications,* vol. 28, no. 5, pp. 1095-1101, 1992.

[14] A. V. Jouanne and P. N. Enjeti, "Design considerations for an inverter output filter to mitigate the effects of long motor leads in ASD applications," *IEEE Transactions on Industry Applications,* vol. 33, no. 5, pp. 1138-1145, 1997.

[15] A. V. Jouanne, P. N. Enjeti and W. Gray, "Application issues for PWM adjustable speed AC motor drives," *IEEE Industry Applications Magazine,* vol. 2, no. 5, pp. 10-18, 1996.

[16] A. Nakajima, M. H. Dhyani, E. M. S. Narayanan, Y. Sumida and H. Kawai, "GaN based Super HFETs over 700V using the polarization junction concept," in *23rd International Symposium on Power Semiconductor Devices and ICs*, San Diego, 2011.

[17] A. Nakajima, K. Adachi, M. Shimizu and H. Okumura, "Improvement of unipolar power device performance using a polarization junction," *Applied Physics Letters,* vol. 89, no. 19, p. 193501, 2006.

[18] Powdec K.K., [Online]. Available: www.powdec.co.jp. [Accessed 1 May 2024].

[19] W. Saito, M. Kuraguchi, Y. Takada, K. Tsuda, T. Domon, I. Omura and M. Yamaguchi, "380v/1.9A GaN power-HEMT: current collapse phenomena under high applied voltage and demonstration of 27.1 MHz class-E amplifier," in *IEEE International Electron Devices Meeting*, Washington, 2005.