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A Methodology to Characterize the Virtual Gate Effect in a Power Amplifier

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***Abstract*— An experimental method to characterize the virtual gate effect in radio-frequency (RF) power amplifiers (PAs) based on high-electron-mobility transistors (HEMTs) is presented. The experimental setup ensures that the GaN device in an amplifier is at the same temperature and trap state every time the experiment is repeated. An algorithm is proposed to estimate multiple trapping time constants simultaneously from measured DC drain current transients of the PA in response to pulsed RF excitation. We observe that the time constants of the device recovery time remain constant over a range of power levels and are related to the shape of the load cycle of the device.**

Keywords— GaN Power Amplifier characterization, Trapping effect, Virtual Gate Effect

I. INTRODUCTION

To meet stringent requirements of linearity of fifth and future-generation mobile networks, a pre-distorter often precedes amplifiers to compensate for their non-linearities. A portion of the distortion is due to memory effects, where the output is dependent on the present and previous inputs to the amplifier. Memory effects can originate from the termination at the baseband and second harmonic frequencies, excitation of traps in the active devices used in the amplifier, the variation in the temperature due to heat dissipation, as well as the layout of the amplifier. The impact of the baseband impedance, the second harmonic impedance, and the layout of the amplifier can be minimized by appropriate design of matching networks. In GaN-based High-Electron-Mobility Transistors (HEMTs), the time constant of the capture mechanism ie., electron trapping, is typically in the order of pico to microseconds whereas emission ie., de-trapping, occurs in micro to milliseconds [1]–[3]. Hence, the application of an RF signal even for a microsecond, results in trapping/de-trapping of charge. The time constant, especially for de-trapping is comparable to the slowly varying envelope of signals used in modern mobile communication systems [4].

However, to offset the impact of traps, there is an immediate need for techniques to characterize the impact of traps on the amplifier. This is important because the widespread adoption of GaN HEMTs is still impeded by trapping which results in current collapse, knee walkout, and DC-RF dispersion, even though these demonstrate high power density and efficiency at high frequency. Characterization of the impact of traps on the amplifier will enable to device compensation mechanism. The trapped charges result in an additional electric field leading to, typically, a reduction in the drain current consumed by the amplifier, thereby impacting the gain. This additional electric field is typically modelled as a fictional voltage source that offsets the gate voltage, often referred to as the virtual gate effect.

Under RF signals, the excited trap centres are related to the maximum drain voltage and the minimum gate voltage of the RF load-line [5], which results in the peak electric field in the device. To characterize the impact of traps under actual large-signal RF stimulus, an RF pulse can be applied to a device in a load pull setup [6]. In this case, the time constants of traps are extracted from the relaxation of the drain current (drain lag) upon the application of the RF pulse [7]. The trap characterization method requires a costly load-pull setup but is now widespread for characterising RF devices.

To better assess the impact of traps on a PA performance, the trap and thermal state of the PA were controlled by a pre-RF pulse, before measuring the dynamic gain in [8]. Apart from an RF input, the impact of a large negative DC gate voltage stressing pulse on the dynamic gain of a GaN-HEMT PA was investigated in [1]. The recovery of the dynamic gain of the PA post-stress was observed to be similar to that from the transient emission of traps in drain-lag measurements of transistors. However, these approaches do not estimate the virtual gate voltage. In [9][10], a technique was introduced to estimate the virtual gate voltage from a two-tone stimulus applied to a PA. In this approach, the cumulative virtual gate voltage originating from the excited trap centres is estimated from the dynamic gain of the amplifier upon the application of the two-tone signal.

In this paper, rather than relying on measured gain as in [9][10], we propose a methodology to identify multiple trap centres excited under large signal RF excitation by segregating the contribution of individual traps to the virtual gate. The experimental setup requires a signal generator and spectrum analyzer which are readily available in an RF lab. We relate the conditions of excitation with the stress caused by the respective load cycle conditions as a function of power level. Measuring the impact of traps on the amplifier is important to design the compensation network such as a lineariser.

II. MEASUREMENT SETUP

The setup used in this work to measure drain current is shown in Fig. 1. The setup is obtained by adding additional circuitry for pulsing the gate voltage of the PA on top of a conventional setup to measure intermodulation distortion. The aim is to identify traps excited under a large signal RF signal ($v_{in,RF}$) whilst keeping the impact of $V_{gs(Q)}$ fixed. A DC switch toggles the gate voltage of the amplifier between V_{off} (less than threshold voltage) and $V_{gs(Q)}$ upon the application of the Pulse_Vg. The timing diagram of the various signals used in the setup is plotted in the Fig. 1 (b). We measure the drain current under two conditions and, in both cases,between event 4 and event 5 highlighed in Fig 1 (b).

1. First, we measure the drain current by turning on the device by pulsing the gate from below threshold, referred to as V_{off}, to $V_{gs(Q)}$ whilst V_{ds} is fixed to V_{dsq}. The rise time of the gate voltage (Vgate) to reach the quiescent voltage ($V_{gs(Q)}$) is dependent on the bypass capacitors; Bypass capacitors are required to ensure that baseband impedances are near short to avoid memory effect due to

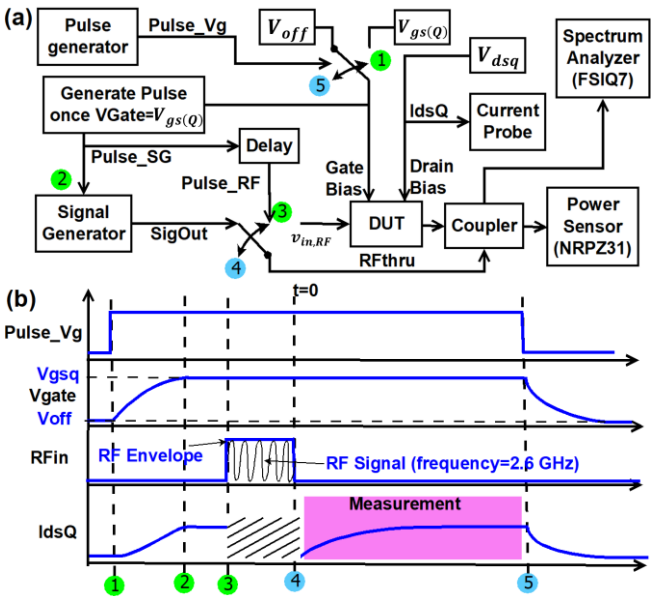

Fig. 1. (a) Block diagram of the pulsed RF setup used. (b) Timing diagram of the measurement setup.

the mixing of the second harmonic with baseband frequencies.

2. The transients of the drain current are measured after the application of the RF pulse. Since the delay between the application of gate voltage (event 1) and the application of RF pulse (event 3) is constant, the temperature and trap state of the device remain the same every time the experiment is repeated.

This methodology is illustrated in detail for a 10W single-stage harmonic tuned amplifier designed using a CGH40010F for 2.6 GHz. The amplifier is biased at V_{dsq} =28 V and I_{dsq} =143 mA. The PAE, output power, and Gain of the amplifier under CW conditions are plotted in Fig. 2. It operates with a small signal gain of 20 dB, delivering 42.1 dBm saturated output power. The peak PAE is ~75 %.

A. Impact of the gate voltage pulse

V_{off} is set to -4.71 V, V_{dsq} to 28 V, and the gate pulse (T_{DC}) is applied for 4 s. Because of large bypass capacitors (330 μF) at the gate bias network which present a short at baseband frequencies, the gate terminal reaches $V_{gs(Q)}$ approximately 3 ms after the application of the gate pulse. Because of this slow-rising gate voltage, traps with time constants lower than this value trap/de-trap by the time V_{gs} reaches $V_{gs(Q)}$. Even though these traps can be extracted by device-level measurement, as illustrated in [11], we assume a fully trapped state when $V_{gs} = V_{gs(Q)}$ (event 3 in Fig. 1 (b)) as the initial condition.

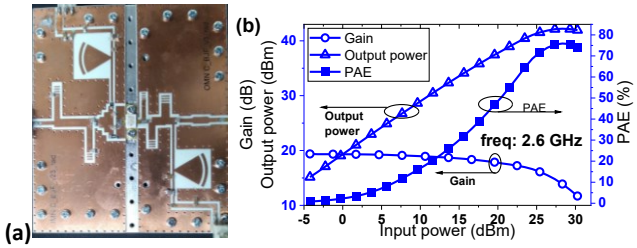

Fig. 2. (a) photograph of the amplifier under test. (b) Measured CW performance of the amplifier.

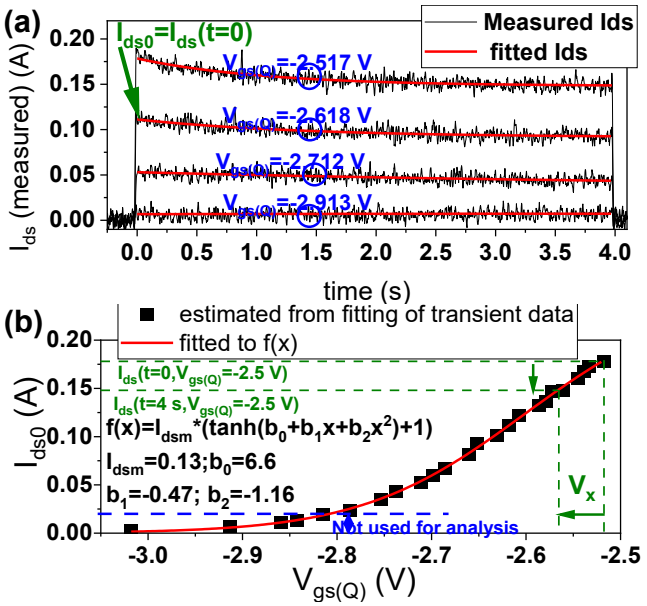

Fig. 3. (a) Measured drain current (I_{ds}) when gate voltage is pulsed from V_{off} (-4.7 V) to $V_{gs(Q)}$. Drain voltage is fixed to V_{dsq} (28 V). The measured drain current is fitted to an exponential function to obtain the drain current when there are no traps (referred to as I_{ds0}). (b) The estimated I_{ds0} from the exponential fitting of the measured I_{ds} as $V_{gs(Q)}$ varied from -3 V to -2.5 V.

The measured drain current (I_{ds}) when $V_{gs(Q)}$ is varied from -2.9 V to -2.5 V is plotted in Fig. 3 (a). The variation of current is minimal with time, at t=4 s, indicating that a steady state has been reached. I_{ds} is fitted to an exponential function given by:

$$I_{ds}(t, V_{gs(Q)}) = I_{ds0} - \Delta I(1 - e^{-\omega t}) \quad (1)$$

The fit is used to identify the initial drain current at t=0, I_{ds0}, and the estimated I_{ds0} from Ids versus $V_{gs(Q)}$ from -3 V to -2.5 V is plotted in Fig. 3 (b). The I_{ds0} is expressed as a function of $V_{gs(Q)}$ ie., $I_{ds0} = f(V_{gs(Q)})$. In this case, we have assumed f(.) to be a hyperbolic tangent function whose coefficients are obtained using a curve fitting tool in MATLAB.

$$f(V_{gs(Q)}) = I_{dsm}(1 + \tanh(b_0 + b_1 V_{gs(Q)} + b_2 V_{gs(Q)}^2)) \quad (2)$$

We assume that $f(.)$ is quasi-static so that the formation of the virtual gate will not change $f(.)$. Under this assumption, $I_{ds}(t)$ can be represented as $f(V_{gs(Q)} + V_x(t))$, where $V_x(t)$ is the voltage of the virtual gate. We first estimate $V_x(t) + V_{gs(Q)}$ as $f^{-1}(I_{ds}(t))$, where $f^{-1}(.)$ is the inverse function of $f(.)$. For example, the voltage of the virtual gate corresponding to I_{ds} at t=4s when $V_{gs(Q)}$=-2.5 V is calculated as $f^{-1}(I_{ds}(t = 4\ s))$+2.5 V, as illustrated in Fig. 3 (b).

B. Characterization of traps excited due to RF signal

The amplifier is characterized by a 60 μs RF pulse and its power level (P_0) is swept from -20 dBm to 30 dBm and the corresponding measured drain current is plotted in Fig. 4 (a). Since the RF pulse width is 2000 times smaller than the time constant of the $V_{gs(Q)}$ pulse, as can be seen from Fig. 3 (a), the interaction of this trap centre with the applied RF signal is minimal.We observe the onset of the virtual gate on the drain current for P_0>10 dBm. The virtual gate voltage V_x due to an RF input pulse corresponding to the current in Fig. 4 (b) is

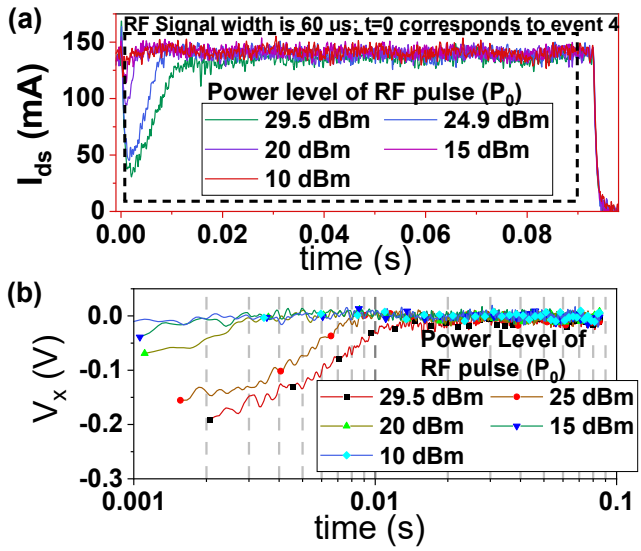

Fig. 4. (a) The measured drain current of the amplifier. The amplifier is biased at Vgsq=-2.5 V and Vdsq=28 V. (b) The virtual gate voltage (V_x) estimated from the measured drain current of the amplifier.

calculated using I_{ds0} from the methodology described in Fig. 3 (b).

III. Results and Discussion

Only a portion of the measured current, as highlighted by the dashed line in Fig. 3 (a), is considered for analysis. $V_x(t)$ is fitted to an exponential by minimizing the following equation.

$$\min \left\| V_x(t) - \sum_{i=1}^{N_\tau} dv_i * exp(-e_{ni} * t) \right\|_2^2 + \sum_{i=1}^{N_\tau} \|dv_i\|_2^2 \qquad (3)$$

Where, N_τ denotes the number of traps, e_{ni} corresponds to the emission rate of the i^{th} trap centre and dv_i is the amplitude of the i^{th} trap center. We use the algorithm outlined in Fig. 5 to estimate N_τ, dv_i and en_i. This algorithm begins with the assumption that there is only one trap ($N_\tau = 1$) and increases N_τ iteratively. For each value of N_τ, we optimize dv_i and en_i to minimize equation (11). The algorithm stops when an increase in N_τ does not result in any additional unique value of en_i ie., a new trap is not identified, and no further reduction of error between the measured $V_x(t)$ and the fit calculated using dv_i and en_i is observed.

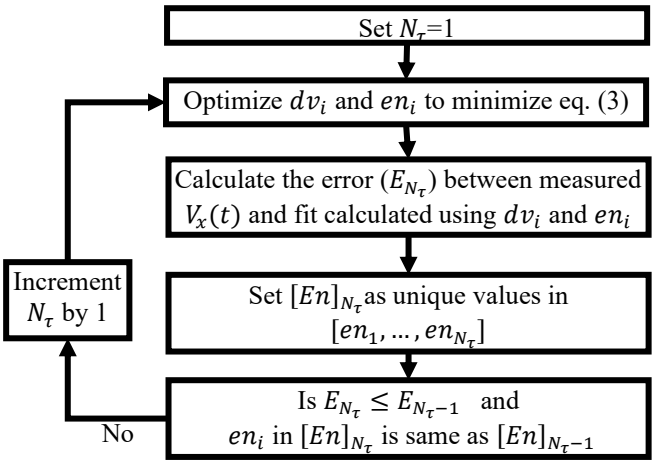

Fig. 5. Algorithm illustrating the identifying dv_i and en_i from $V_x(t)$

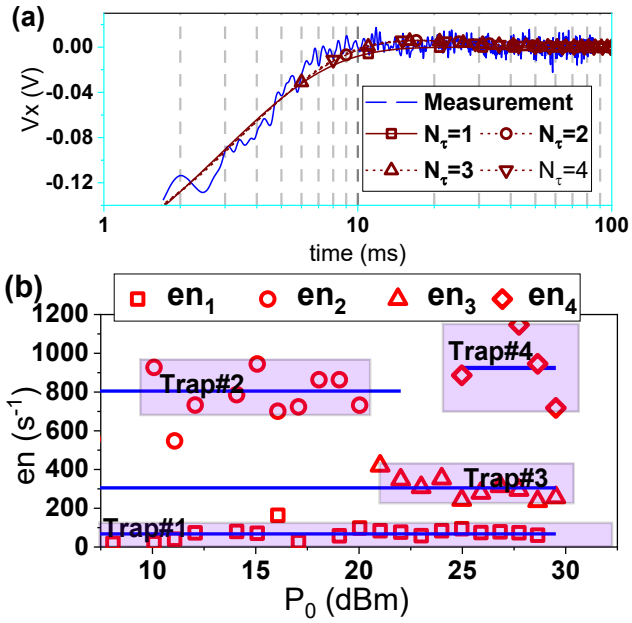

Fig. 6. (a) The comparison of the measured and model fit of the drain current for P_0=27.7 dBm. (b) Emission time constants of traps for power levels from 5-30 dBm.

This algorithm is illustrated for a power level (P_0) of 27.7 dBm. Values of en_i and dv_i obtained as N_τ , increased from 1 to 4 are given in Table I which indicates the existence of three traps. Further increase in N_τ from 3 to 4, results in the same unique en_i values with a repetition of en_i=243 s^{-1} and the corresponding value of dv_i is half of that obtained for N_τ=3. The voltage of the virtual gate estimated based on the en_i and dv_i given in Table I is compared with the v_x estimated from measurement in Fig. 6 (a). We observe good agreement for $N_\tau > 2$.

TABLE I. The obtained values of en_i and dv_i for P_0=-7 dBm when N_τ is set to 1,2,3, and 4.

		Trap#1	Trap#2	Trap#2	Trap#3
N_τ=1	$en_i(s^{-1})$		345.6		
	dv_i(V)		-0.2554		
N_τ=2	$en_i(s^{-1})$	59.9	288.3		
	dv_i(V)	0.0217	-0.261		
N_τ=3	$en_i(s^{-1})$	73.2	286.8		1317.3
	dv_i(V)	0.0266	-0.2693		0.0231
N_τ=4	$en_i(s^{-1})$	73.6	294.4	294.4	1146.7
	dv_i(V)	0.0279	-0.1411	-0.1411	0.0423

The values of en_i extracted from the measured drain current after the application of RF pulses whose magnitude is increased from 5 dBm to 30 dBm are plotted in Fig. 6 (b). We observe four traps with e_n values of 75 s^{-1}, 300 s^{-1}, 800 s^{-1}, and 940 s^{-1}. The corresponding trap voltages (dv_i) for these three traps are plotted in Fig. 7. We observe that trap#2 and trap#3 are de-trapping whereas, trap#1 and trap#4 are trapping, upon application of the RF pulse.

The simulated load lines for power levels from 10 dBm to 18 dBm, which are sufficient to excite Trap #2 are plotted in Fig. 8 (a). These load lines were obtained by performing large signal power sweeps of the vendor model and the measured S-parameters of the input and output matching network. We observe that the minimum of the drain current is just above 0 A at 10 dBm and the drain current clips as this power level

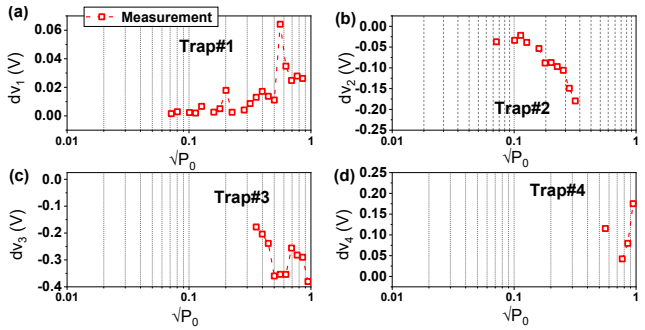

Fig. 7. Virtual gate extracted as a function of power levels from 5 - 30 dBm

increases, indicating that the gate voltage goes below the threshold voltage of the device. Simultaneously, the drain voltage increases, resulting in an increase in the electric field/stress on the gate dielectric.

The onset of traps#3 and traps#4 occurs for power levels 20 dBm and 25 dBm respectively and the corresponding load lines are plotted in Fig. 8 (b). It is observed that trap#3 originates from a similar reason as trap#2 ie., an increase in the magnitude of peak gate and drain voltage. However, trap#4 could be attributed to the fact that the electric stress in the device is minimal as both gate and drain voltages approach 0 V for the duration of the load line in the circled region (Trap#4). This duration increases with power level, as can be observed by comparing the load lines at 25 dBm and 26 dBm. Additionally, we observe that $en_2 \approx en_4$, indicating partial de-trapping of trap#2 for the duration highlighted by the circle for trap#4. Hence, the trap voltage (dv_4) is positive indicating that trapping occurs upon the removal of the RF signal unlike for traps #2 and #3. The origin of trap#1 is not clear. Additionally, further investigations are required for a better understanding of the location of trap centers.

IV. Conclusion

We demonstrate a method for the characterization and modelling of trap centers excited upon application of pulsed RF stimulus in a 10 W radio-frequency (RF) power amplifier (PA) based on a GaN CGH40010 part. The proposed method

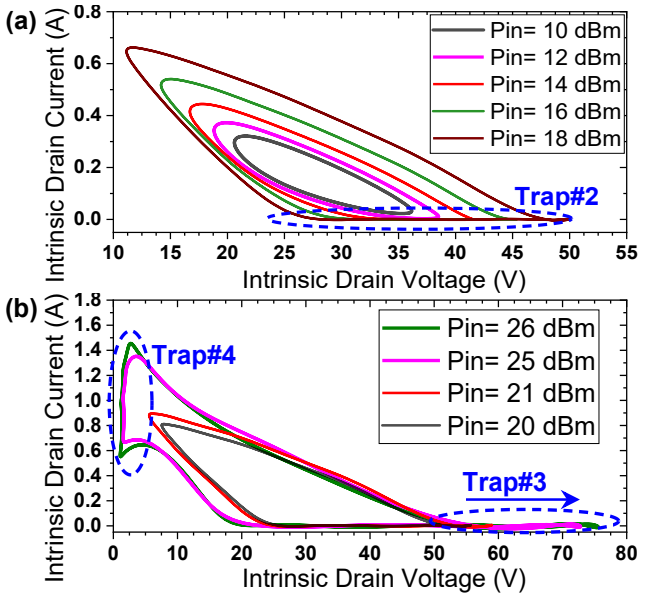

Fig. 8. Simulated load line response of a second harmonic-tuned amplifier for multiple input power levels. (a) 10 dBm – 18 dBm. (b) 20 dBm – 26 dBm

consists of measuring the DC drain current of the PA in response to pulsed RF excitations and estimating the time constants of the traps from the estimated virtual gate voltage. To the best of our knowledge, this is the first time the trapping time constants excited under large signal RF stimulus of a PA, is demonstrated. We observe that trap centers trap#2 and trap#3 result in trapping due to an increase in the gate and drain voltages. On the other hand, when the amplifier operates in saturation ie., when the load line is in the knee region, de-trapping of the electrons occurs (identified as trap#4).

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