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Alimi, Y. [orcid.org/0000-0002-5198-6557](https://orcid.org/0000-0002-5198-6557), Guilhabert, B. [orcid.org/0000-0002-3986-8566](https://orcid.org/0000-0002-3986-8566), Jevtics, D. [orcid.org/0000-0002-6678-8334](https://orcid.org/0000-0002-6678-8334) et al. (4 more authors) (2025) Micro-transfer printing of InGaAs/InP avalanche photodiode on Si substrate. *Semiconductor Science and Technology*, 40 (1). 015023. ISSN 0268-1242

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## Micro-transfer printing of InGaAs/InP avalanche photodiode on Si substrate

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# Micro-transfer printing of InGaAs/InP avalanche photodiode on Si substrate

Yasaman Alimi<sup>1,\*</sup> , Benoit Guilhabert<sup>2</sup> , Dimitars Jevtics<sup>2</sup> , Elisa M Sala<sup>1,3</sup> , Michael J Strain<sup>2</sup>, Kristian M Groom<sup>1</sup> and Jon Heffernan<sup>1,3</sup>

<sup>1</sup> Department of Electronic and Electrical Engineering, University of Sheffield, Sheffield S1 3JD, United Kingdom

<sup>2</sup> Institute of Photonics, Department of Physics, University of Strathclyde, Glasgow G1 1RD, United Kingdom

<sup>3</sup> EPSRC National Epitaxy Facility, University of Sheffield, Sheffield S1 3JD, United Kingdom

E-mail: [y.alimi@sheffield.ac.uk](mailto:y.alimi@sheffield.ac.uk)

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## Abstract

We report on the fabrication and micro-transfer printing ( $\mu$ -TP) of InGaAs/InP avalanche photodiodes (APDs) onto silicon substrates. A process flow was developed to suspend the devices using semiconductor tethers. The developed process reduces the number of fabrication steps required compared to methods based on the use of photoresist tethers. Furthermore, our process is compatible with devices that may be susceptible to damage induced by the photoresist removal process. APDs were characterised in linear mode operation both before suspension and after printing. Despite the additional fabrication steps required to suspend the APD membranes and the physical nature of the  $\mu$ -TP process, the electrical characteristics of the devices were preserved. No degradation in the optical performance of the devices was measured. Our work represents the first demonstration of  $\mu$ -TP of InGaAs/InP APDs onto silicon substrates. The results highlight the viability of  $\mu$ -TP for effective heterogeneous integration of InGaAs/InP APDs with silicon photonic integrated circuits for optical and quantum communication and other light detection applications.

Keywords: III–V-on-Si integration, micro-transfer printing, avalanche photodiodes, InGaAs/InP APDs, heterogeneous integration

## 1. Introduction

Silicon Photonics is an important material platform for the development of complex photonic integrated circuits (PICs) for a wide range of applications including telecom [1] and quantum communications [2]. Despite recent advances, the platform inherently lacks various optical functionalities which

impede its potential for the next generation of PICs. These functionalities are typically realised in III–V devices such as high-speed and low-power consumption modulators, single-photon detectors operating beyond 1600 nm and single-photon sources for quantum applications. It is becoming increasingly evident that the key to developing fast, energy-efficient, ultra-compact PICs is the heterogeneous integration of III–V active devices with Si-based circuits. Amongst the approaches currently used, flip-chip [3] and die bonding [4] are the most mature techniques. However, they face challenges in terms of the cost-effectiveness of scaling up to achieve high throughput and high-density integration or effective use of materials. Monolithic integration [5] is also used as an alternative to heterogeneous integration. This technology is currently in the research and development stage and faces significant

\* Author to whom any correspondence should be addressed.



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challenges in terms of material compatibility and fabrication complexity when the integration of more than one additional material system onto Si PICs is required. Micro-transfer printing ( $\mu$ -TP), on the other hand, is an innovative and versatile approach that has recently gained considerable interest due to its advantages over more established methods [6].  $\mu$ -TP is a pick-and-place integration method, where devices from one material system are picked from their native substrate and placed on a host substrate using a Polydimethylsiloxane (PDMS) stamp. To do so, thin membranes ( $100 \text{ nm}^{-1} \mu\text{m}$ ) are released from their native substrate and suspended by creating tethers. The integration of different III–V devices onto Si-based platforms using  $\mu$ -TP has been demonstrated. Recent reports include the  $\mu$ -TP of GaAs-based quantum dot lasers, single photon sources [7–11] and GaAs photodetectors [12, 13] as well as C-band InP-based sources [14–18] and photodiodes [19]. To the best of our knowledge, despite recent advances,  $\mu$ -TP of III–V avalanche photodiodes (APDs) and single-photon avalanche diodes (SPADs) have not yet been demonstrated. APDs offer fast response times and high detection sensitivity due to the multiplication of photogenerated carriers through internal gain. Moreover, APDs can be operated in Geiger mode for single photon detection, making them indispensable components in advanced PICs for quantum communication.

Currently, Germanium-on-Silicon (Ge-on-Si) APDs and SPADs demonstrate low noise and high gain bandwidth due to the low impact ionization coefficient ratio in silicon [20]. However, they often exhibit relatively high dark current due to lattice mismatch between Si and Ge resulting in a high density of dislocations. Moreover, the absorption coefficient of Ge falls rapidly with increasing wavelength beyond  $1.55 \mu\text{m}$  [21]. Separate absorber, charge, grading and multiplication (SACGM) APDs based on  $\text{In}_{0.53}\text{Ga}_{0.47}\text{As}$  absorbing material are promising candidates for low noise and high sensitivity detection in the C-band wavelength range [22]. InGaAs/InP SACGM APDs and SPADs have been widely commercialised [23] and can achieve a very low dark count rate of a few kilo-counts per second and photon detection efficiency higher than 20% at  $1.55 \mu\text{m}$  [24].  $\mu$ -TP of InGaAs/InP SPADs onto Si-based PICs can pave the way for cost-effective and high-throughput development of integrated next-generation classical and quantum communication circuits. Given the sensitive nature of the detection process in APDs, any change in the physical and structural integrity of the devices during the transfer printing process could impact their performance. Consequently, it is not immediately evident that  $\mu$ -TP would not degrade the performance of APDs.

In recent studies on  $\mu$ -TP of III–V devices, transfer-printed membranes were primarily suspended using photoresist [12, 13] or dielectric [19] tethers. These methods involve additional steps, such as patterning and etching additional mesa on release layers to create encapsulation and tether structures. After transfer printing, the encapsulation layer must be removed, which can present challenges, especially when the host materials are sensitive to removal techniques such as dry etch or  $\text{O}_2$  plasma ashing. As an alternative, membranes can be suspended by fabricating semiconductor tethers from the

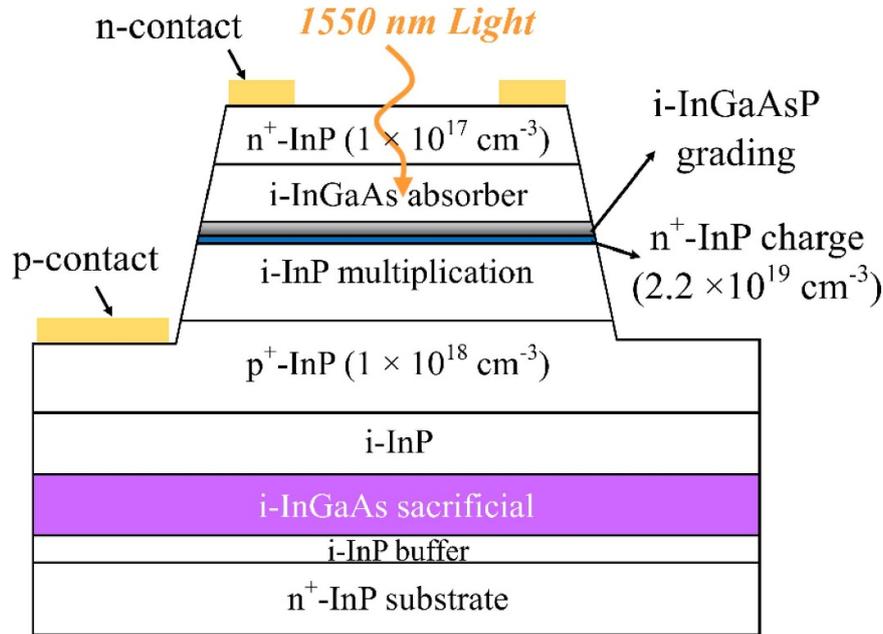
native epitaxial material. In this work, we present the fabrication and  $\mu$ -TP of InGaAs/InP SACGM APDs onto Si wafers, where the devices were suspended using semiconductor tethers. We also present a preliminary investigation into the effect of  $\mu$ -TP on the dark current and electrical characteristics of the APDs.

## 2. Device structure

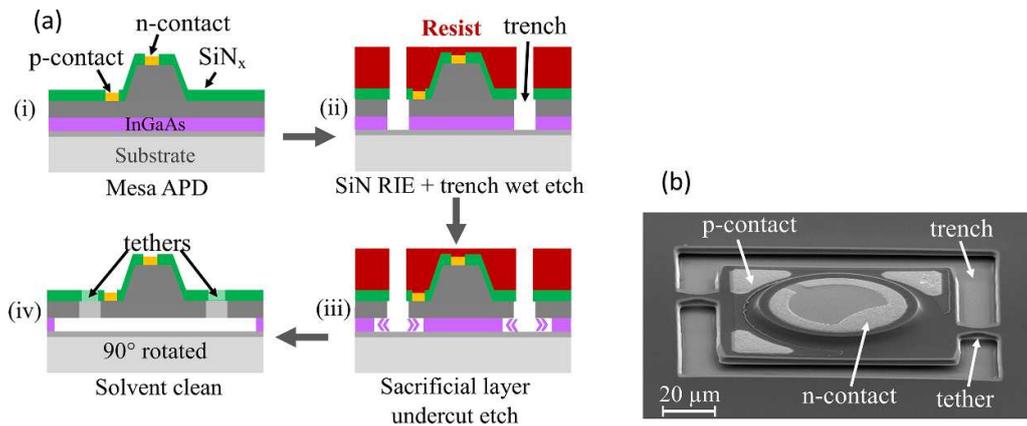
To implement  $\mu$ -TP of any devices, it is essential to release them from their growth substrate. This is achieved by growing the epitaxial structure upon a ‘sacrificial layer’. The sacrificial layer is composed of a material that can be anisotropically etched using an appropriate etchant that provides adequate etch selectivity between the sacrificial layer and the remaining layers. In this study, an InGaAs/InP SACGM APD structure was grown on a lattice-matched  $\text{In}_{0.53}\text{Ga}_{0.47}\text{As}$  sacrificial layer [25]. The device structure is designed for Geiger mode operation. However, in this study, we carried out a preliminary study of the effect of transfer printing on the electrical and optical characteristics of the APDs whilst operated in linear mode. The epitaxial layers were grown in a close-coupled shower-head metal–organic vapour phase epitaxy Aixtron reactor. The detailed layer structure is shown in figure 1. Growth commenced with a 300 nm undoped InP buffer on a (100)  $\text{n}^+$ -InP substrate, followed by a  $1 \mu\text{m}$  thick  $\text{In}_{0.53}\text{Ga}_{0.47}\text{As}$  sacrificial layer, a  $1 \mu\text{m}$  thick undoped InP layer, and the sequential growth of the SACGM APD layers. The APD layers consist of a  $2 \mu\text{m}$   $\text{P}^+$ -InP layer, a  $1 \mu\text{m}$  undoped  $\text{In}_{0.53}\text{Ga}_{0.47}\text{As}$  layer for efficient absorption of photons at a wavelength of 1550 nm, an 85 nm  $\text{n}^+$ -InP charge layer for controlling the electric field distribution in the absorber and multiplication layers, lattice-matched InGaAsP grading layers, a  $1.5 \mu\text{m}$  undoped InP multiplication layer, and a  $1 \mu\text{m}$   $\text{n}^+$ -InP layer. The gradings consist of three layers of InGaAsP with varying indium and arsenic content, from 90.8% to 67.2% and 20.2% to 70.8%, respectively. This composition gradient was used to smooth the valence band discontinuity and prevent hole accumulation at the InGaAs/InP heterointerface.

## 3. Device fabrication

Top illuminated mesa APDs with diameters of 35, 50 and  $70 \mu\text{m}$  were fabricated on  $100 \times 100 \mu\text{m}$  tethered membranes for  $\mu$ -TP. The fabrication process started with the formation of the top n-contacts by photolithography and thermal evaporation of InGe/Au (20 nm/200 nm). The contacts were then annealed by rapid thermal annealing (RTA) at  $420 \text{ }^\circ\text{C}$  for 3 s. Subsequently, circular mesas were defined and etched by an isotropic wet etching to the p-contact layer, using a  $\text{CH}_3\text{COOH}:\text{HBr}:\text{K}_2\text{Cr}_2\text{O}_7$  (1:1:1) solution. The bottom p-contacts were then defined by depositing Au/Zn/Au (5 nm/10 nm/200 nm), and RTA at  $360 \text{ }^\circ\text{C}$  for 30 s. Afterwards, a 250 nm thick  $\text{SiN}_x$  passivation layer was deposited by plasma enhanced chemical vapor deposition at  $300 \text{ }^\circ\text{C}$ . The mesa side walls were subjected to treatment in diluted HCl and  $\text{NH}_4\text{OH}$  solutions before  $\text{SiN}_x$  deposition to reduce the surface current



**Figure 1.** Cross-sectional schematic diagram of the InGaAs/InP SACGM APD structure grown on an InGaAs sacrificial layer.



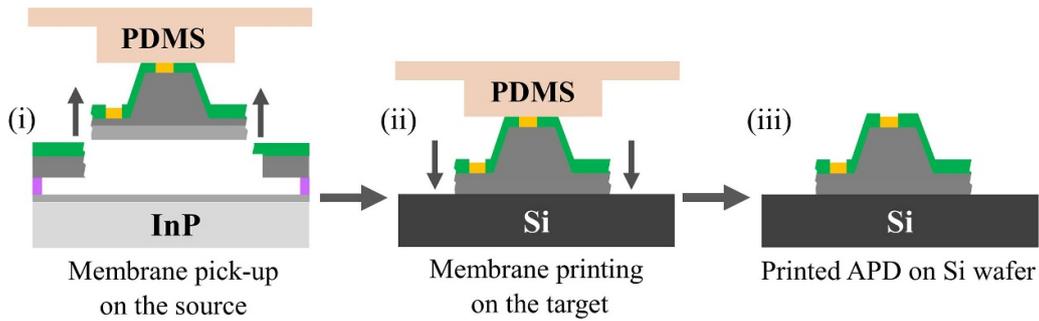
**Figure 2.** (a) Illustration of the process flow for definition and undercut etching the APD membranes ((i): mesa APD with  $\text{SiN}_x$  passivation, (ii): defining  $100 \times 100 \mu\text{m}$  membranes, (iii): undercut etching the sacrificial layer, (iv): a suspended APD membrane, tethered to the substrate, (b) SEM image of a suspended  $70 \mu\text{m}$  APD with two semiconductor tethers.

leakage. The  $\text{SiN}_x$  was then patterned and etched using a reactive ion etch (RIE) tool to open up the optical window as well as the  $n$  and  $p$  contacts. A cross-sectional schematic diagram of a fabricated mesa APD is shown in figure 2(a-i). The following process steps were carried out to create  $100 \times 100 \mu\text{m}$  membranes with semiconductor tethers and release the membranes from the InP substrate.  $100 \times 100 \mu\text{m}$  membranes with either two or four asymmetrically positioned tethers around each APD were defined by photolithography and patterning  $15 \mu\text{m}$  wide trenches with bow-tie-shaped tethers. The trench width was designed to provide sufficient space for the undercut etchant to access the sacrificial layer while offering an appropriate tether length to prevent the membrane from collapsing. The bow-tie design creates breaking points away from the membrane edge and prevents forming cracks and damaging the membranes during the pick-up process. Firstly, the  $\text{SiN}_x$  was removed from the trenches using RIE etching. The

trenches were then etched down to the InGaAs sacrificial layer in a  $\text{CH}_3\text{COOH}:\text{HBr}:\text{K}_2\text{Cr}_2\text{O}_7$  (2:2:1) solution. To release the membranes, the InGaAs sacrificial layer was subsequently etched and removed from underneath the membranes and tethers in an  $\text{H}_2\text{SO}_4:\text{H}_2\text{O}_2:\text{H}_2\text{O}$  solution, which provided a very high etch selectivity to InP. Finally, the photoresist was removed by solvent cleaning. An SEM image of a suspended  $70 \mu\text{m}$  APD is shown in figure 2(b).

#### 4. $\mu$ -TP

$\mu$ -TP of the APDs was performed using a custom high-resolution, computer-controlled tool comprised of a stack of stages with 6 degrees of freedom [26]. The tool provides 200 mm of lateral and 10 mm of vertical travel with a minimum incremental step size of 5 nm, along with roll, pitch and



**Figure 3.** Schematic illustration of  $\mu$ -TP of APDs onto a Si substrate using a PDMS stamp.

yaw angular steps of  $\pm 3^\circ$  and a yaw angle of  $\pm 10^\circ$ . Its precise stage control and alignment techniques enable the accurate placement of printed devices, achieving an average absolute positioning accuracy of  $100 \pm 70$  nm [27]. The tool is equipped with a microscope to facilitate imaging of the devices while manipulating them using a PDMS pick-up head (hereafter referred to as the ‘stamp’), which is supported by a transparent glass plate. The transfer-printing process was fully controlled through a custom graphical user interface.

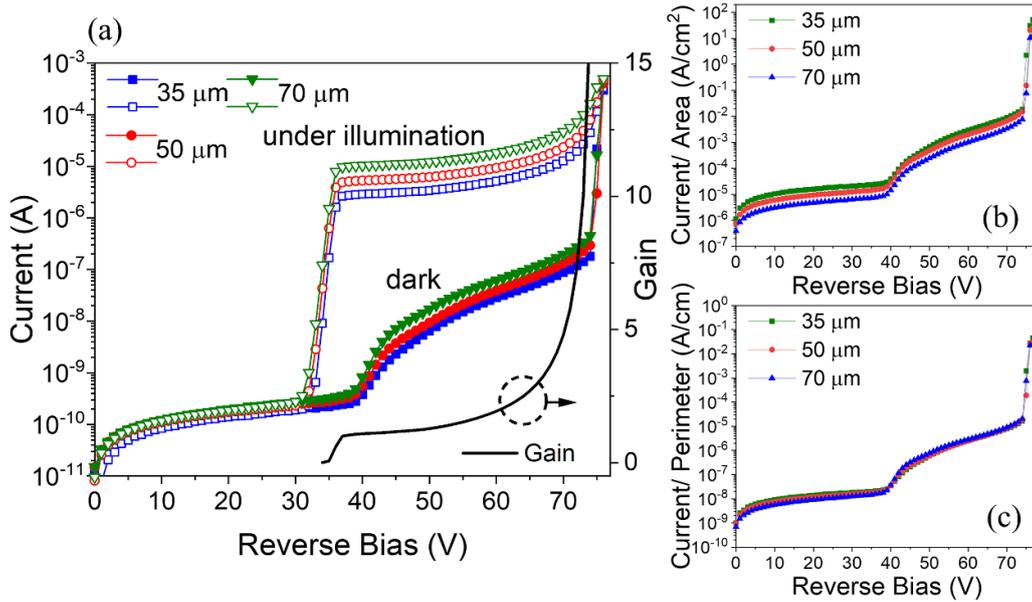
The  $\mu$ -TP process was conducted using a  $100 \times 100 \mu\text{m}$  PDMS stamp. A schematic illustration of the  $\mu$ -TP is shown in figure 3(i–iii), employing reversible adhesion as reported before [28]. PDMS is an elastomer that, rather than applying a force to a membrane device, conforms to the features of the device, creating an interfacial adhesion whose strength depends on the shape of the stamp and its contact area to the device, mediated by Van der Waal’s forces. In addition, this adhesion is kinematically controlled due to the visco-elastic property of PDMS. During the pick-up process, the stamp was brought into contact with the APD membrane to conform to the APD features, followed by a rapid pulling motion at a velocity of  $5 \times 10^3 \mu\text{m s}^{-1}$  to break the tethers and pick up the membrane. At this stage, the membrane adhered to the stamp. The membrane was then transferred and printed onto a bare Si wafer using solely a vertical motion at a velocity of  $1 \mu\text{m s}^{-1}$ . The Si wafer was unpatterned without any features, and its surface was cleaned to a micro-fabrication standard using an oxygen ashing process at  $200^\circ\text{C}$ . No other material was used for adhesion of the membrane devices onto the silicon surface. Through slow retraction of the stamp, the adhesion between the stamp and the membrane is decreased and becomes less than the non-covalent adhesion of the latter to the receiving surface. The non-covalent adhesion of the membrane to the silicon receiver can be estimated using a generalised Van der Waal’s adhesion force calculation. This approach uses the contacts between two flat surfaces and the Van der Waal’s adhesion force is directly proportional to the contact area by their Hamaker constant and inversely proportional to the cube of the separation distance. The Hamaker constant reflects the attraction force between two bodies via their surface energy. For InP onto Si, the Hamaker constant has a typical value in the order of  $10 \times 10^{-19}$  J, resulting in an adhesion force at a distance of 1 nm of  $10 \times 10^{-1}$  N. Previously reported work demonstrated that such bonded devices can be employed

in subsequent micro-fabrication processes such as in [29].  $\mu$ -TP, as an integration technique, is a fully deterministic process that is not exclusive to the material system presented here. Extensive studies on its parameters, yield statistics and accuracy of integration can be found, for instance, in [6] and [27, 30], respectively.

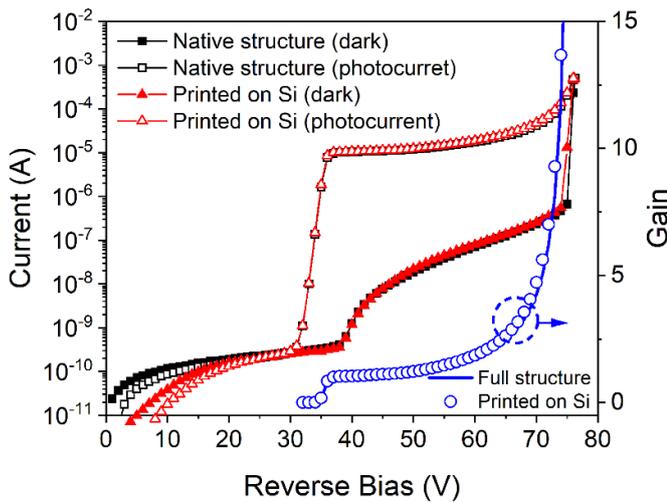
## 5. Results and discussion

Electrical and optical characterisation of the APDs was carried out at room temperature before the undercut etch and after subsequent printing onto a Si receiver wafer. Reverse current–voltage ( $I$ – $V$ ) measurements were performed using a Keysight B2901B source measure unit). A 1550 nm single-frequency, continuous-wave DFB laser diode (Thorlabs LP1550-SAD2) with an output power of  $10 \mu\text{W}$  was used for optical illumination. Figure 4(a) shows the dark and under-illumination  $I$ – $V$  characteristics of APDs with various diameters before the undercut etching process. A sharp increase in the photocurrent was observed at  $-32$  V, corresponding to the punch-through voltage ( $V_{\text{pt}}$ ). At this voltage, the depletion region extends into the InGaAs absorber layer, leading to efficient collection of the photogenerated carriers. The measured breakdown voltage ( $V_{\text{br}}$ ) was  $-74$  V. The avalanche gain ( $M$ ) of the APDs was also determined as a function of voltage as the ratio of the photocurrent at a given voltage to the photocurrent at unity gain and is also plotted in figure 4(a). At  $0.95 V_{\text{br}}$ , the dark current in the 35, 50 and 70  $\mu\text{m}$  diameter devices was  $\sim 87$  nA, 130 nA and 196 nA, respectively. Compared to planar structures [30], mesa devices can be expected to exhibit higher dark currents due to the presence of sidewall surface leakage. The total dark current in mesas comprises bulk leakage current, which is proportional to the mesa area, and surface leakage current, which is proportional to the mesa perimeter. The dark current/area and dark current/perimeter of the APDs as a function of reverse bias are shown in figures 4(b) and (c).

As shown, the current at all voltages is proportional to the perimeter of the mesa and implies that the dark current in these mesa APDs is dominated by the surface leakage. The bulk current and surface current of the 70  $\mu\text{m}$  APDs at  $V = -37$  V ( $M = 1$ ) were obtained as 0.17 nA and 0.92 nA, respectively, by linear fitting of the total dark current density as a function of the perimeter-to-area ratio of the devices. This



**Figure 4.** (a)  $I$ - $V$  characteristics of APDs in the dark and under 1550 nm illumination. The filled symbols indicate the dark current, and the unfilled ones represent the current under illumination. (b) Dark current/area and (c) dark current/perimeter of APDs with different diameters as a function of reverse bias.



**Figure 5.**  $I$ - $V$  characteristics and gain of a 70  $\mu\text{m}$  APD before undercut etch and after being printed onto a Si wafer.

indicates that the surface leakage in the devices is approximately five times higher than the bulk leakage current. Such surface leakage can be significantly reduced through the employment of better passivation techniques, such as the application of benzocyclobutene [31].

Electrical and optical characterisation of the APDs was also performed after transfer printing. Figure 5 shows the reverse  $I$ - $V$  characteristic of a representative 70  $\mu\text{m}$  diameter APD before the undercut etch (native structure) and after printing on the Si substrate. The printed device demonstrates the same  $V_{\text{pt}}$ ,  $V_{\text{br}}$  and photocurrent as the devices before undercut and the electrical characteristics of the device were maintained within the APD operating voltage range. These results indicate that

there has been no apparent degradation in the performance of the device as a result of the  $\mu$ -TP process, and that  $\mu$ -TP does not affect the mesa surface states nor the surface leakage in the APDs. The results also indicate that bulk leakage current does not increase by more than a maximum of a factor of five in these devices (which remain dominated by surface leakage). Future work on planar SPADs will determine any limiting effect of  $\mu$ -TP on bulk current leakage. The higher dark current in the native device at voltages below  $-20$  V is attributed to the leaky behaviour of the sacrificial layer when the APD is not fully depleted [32].

## 6. Conclusion

We have demonstrated the fabrication and  $\mu$ -TP of mesa APDs on Si substrates. We developed a process flow to release the membranes and suspend them using semiconductor tethers. Compared to photoresist tethering systems, this approach involves fewer fabrication steps, making it more cost-effective. Moreover, it eliminates the need for resist removal after transfer printing, which can potentially degrade certain material systems. Devices were characterised before and after transfer printing. The measured dark current at  $0.95 V_{\text{br}}$  was  $\sim 196$  nA for 70  $\mu\text{m}$  diameter devices. The dark current in the mesa APDs was dominated by surface leakage and did not deteriorate after being printed on the Si substrate. The electrical characteristics of the printed device were maintained within the APD operating voltage range, demonstrating that there has been no apparent degradation in the structural integrity or electrical performance of the devices as a result of the  $\mu$ -TP process. To further investigate the effect of  $\mu$ -TP on the bulk leakage, the transfer-printing of planar APD

structures and SPADs will be explored, where the dark current is primarily dominated by the bulk leakage current. This work represents the first demonstration of  $\mu$ -TP of InGaAs/InP APDs onto Si substrates. The results highlight the viability of  $\mu$ -TP for integrating InGaAs/InP APDs with Si-based platforms without affecting their electrical performance and demonstrates strong prospects for the effective heterogeneous integration of InGaAs/InP SPADs with Si PICs for use in 1550 nm applications.

### Data availability statement

All data that support the findings of this study are included within the article (and any supplementary files).

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### ORCID iDs

Yasaman Alimi  <https://orcid.org/0000-0002-5198-6557>  
 Benoit Guilhabert  <https://orcid.org/0000-0002-3986-8566>  
 Dimitars Jevtics  <https://orcid.org/0000-0002-6678-8334>  
 Elisa M Sala  <https://orcid.org/0000-0001-8116-8830>

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