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Ultra-Low Phase Noise 100 MHz Crystal Oscillator

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***Abstract*—This paper describes an ultra-low phase noise 100 MHz crystal oscillator with a phase noise of around -140 dBc/Hz at a 100 Hz offset. The oscillator includes digitally-controlled phase shifter and attenuator elements, which allow for a flexible approach in the oscillator design and a low residual noise quad parallel differential amplifier. The effect of using an attenuator in the oscillator loop to improve phase noise is also explored.**

Keywords—oscillators, low phase noise, crystal oscillators

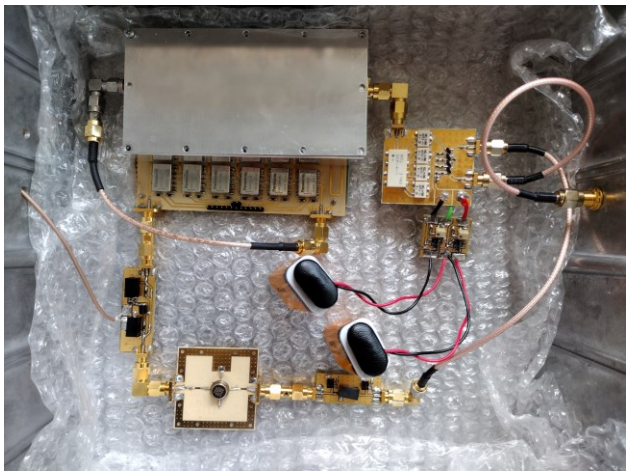

Fig. 1. Photo of the ultra-low phase noise 100 MHz crystal oscillator

I. Introduction

Minimising phase noise and jitter is an important factor in designing oscillators used to provide a very stable reference frequency required for many modern systems. For example, ultra-low phase noise oscillators operating at 100 MHz have applications in communications & RADAR systems, atomic clocks and particle accelerator systems.

There exist in the literature and as commercially-available products 100 MHz oscillators that exhibit a phase noise performance around -140 dBc/Hz at a 100 Hz offset [1] [2], however their construction and architecture are not described in detail.

This research builds on work done by this group in producing low phase noise crystal oscillators operating at 10 MHz [3] [4].

II. Design Overview

A block diagram of the oscillator is shown in Fig. 2. and its constituent components are described in detail in the following sections.

A. Crystal Resonator

The resonator is a KVG #O5SC85105A [4] 5th overtone SC- cut quartz crystal with a stated maximum phase noise of -130 dBc/Hz at a 100 Hz offset. It is operated at a drive level of around 5 dBm.

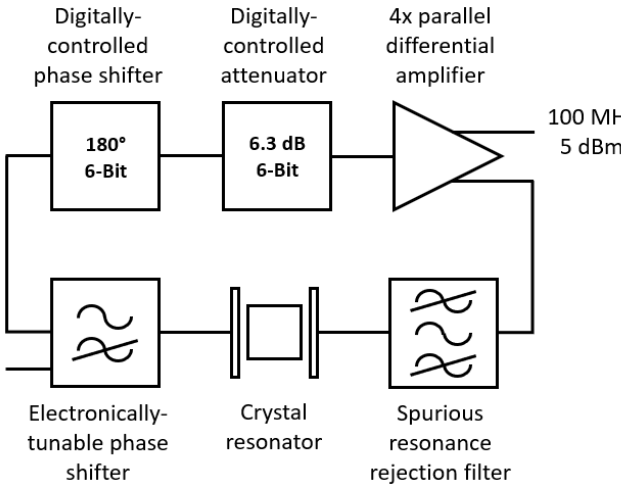

Fig. 2. Oscillator block diagram

B. Spurious Resonance Rejection Filter

An LC band pass filter is used to prevent oscillation at spurious resonant frequencies of the crystal. It is a 3rd-order Butterworth filter with a 40 MHz bandwidth and centre frequency at 100 MHz. The circuit diagram is shown in Fig.3.

C. Electronic Phase Shifter

The electronic phase shifter is used for narrow-band frequency tuning of the oscillator via an external control voltage. The circuit diagram is shown in Fig.4. It is based on the design described in [3]. The circuit is a 5th-order LC high pass filter with a cutoff frequency at around $0.6 \cdot f_0$ where varactor diodes biased through a voltage applied to the centre inductor are used as tuning elements. In addition to allowing the oscillator to be used in a phase-locked loop configuration, the oscillator loop phase can be adjusted to minimise phase noise degradation due to open-loop phase error as described in [5].

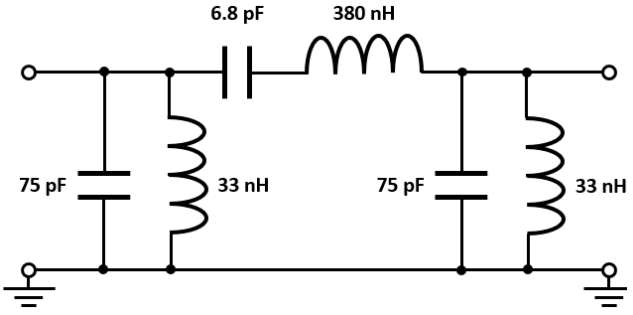

Fig. 3. Circuit diagram of the spurious resonance rejection filter

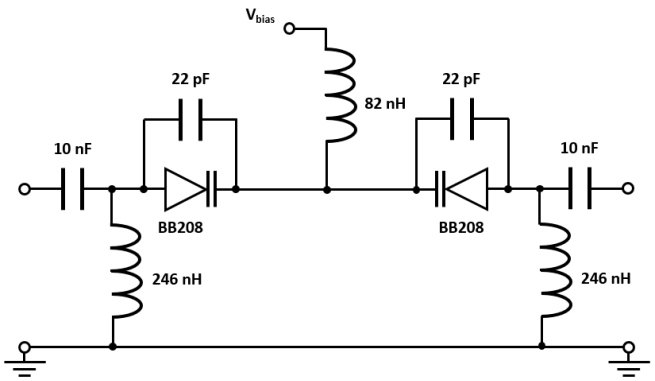

Fig. 4. Circuit diagram of the electronic phase shifter

III. Digitally-Controlled Phase Shifter and Attenuator

The digitally-controlled phase shifter and attenuator are passive devices that use Panasonic ARA220A12 latching RF relays to switch a series of delay line / attenuator elements into the signal path based on a digital control signal. These devices are designed to provide a quick and simple way to test alternative oscillator configurations and amplifier designs that require different operating conditions. The phase shifter and attenuator share a similar construction and in both cases were found to have an insertion loss of less than 0.5 dB. A passive design was selected to minimise flicker noise and it was found to be low enough that it could not be measured on any residual noise measurement systems that were available, including an R&S FSWP [6].

A. 6-Bit 180° Phase Shifter

The purpose of the digital phase shifter is to set the loop phase of the oscillator to roughly 0° so that it can then be fine-tuned using the electronic phase shifter. Having a phase shifter that operates over such a wide range eliminates the need to insert additional lengths of coaxial cable into the loop that must be changed whenever the open-loop phase shift of the oscillator is altered during the design and optimisation process.

The device operates by using microstrip transmission lines as delay elements that can be switched into the signal path or bypassed via a straight-through connection. The most significant bit of the digital control signal corresponds the longest delay line and for each subsequent bit the length of the microstrip is roughly halved, plus a fixed length equal to the length of the straight-through path. This allows the electrical length of the device to be varied linearly according to the binary number represented by the digital control code.

B. 6-Bit 6.3 dB Attenuator

The purpose of the digital attenuator is to set the loop power of the oscillator such that the drive level of the crystal is as high as possible without degrading phase noise performance or driving the amplifier too far into saturation. A 0.1 dB resolution gives reasonable control over the overall loop power.

This device operates in a very similar way to the 6-bit phase shifter, although in this case the microstrip delay lines are replaced with resistive attenuator networks. The most significant bit represents the network with the most attenuation and the attenuation is halved for each subsequent bit.

IV. Quad Parallel Differential Amplifier

The amplifier uses a parallel configuration of 4 long-tailed pair differential amplifiers that is designed to provide a higher maximum available output power compared to a single long-tailed pair amplifier with a similar gain, whilst reducing the quiescent current through each transistor. The complementary outputs of the amplifier allow for one output to be fed back into the oscillator loop while the other is used as a buffered oscillator output signal.

A. Theory of Operation

The single differential amplifier subcircuit used in the design is shown in Fig. 5. and is based on the design described in [3]. It uses a transformer with 2:1 impedance transformation ratio at its input to produce the differential signal required for driving the inputs to the long-tailed pair. The quiescent current through the transistors is set by the approximate current source created by the combination of a negative bias voltage and fixed 680 Ω resistor.

A block diagram of the quad parallel combination of these amplifiers used in the design is shown in Fig. 6. A 0° power splitter is used at the input to supply the signal to each of the differential amplifier subcircuits and the outputs are then combined by connecting the collectors of the transistors together, effectively summing the collector currents. When this is compared with the single differential amplifier in Fig.5. it can be seen that the current through each of the 50 Ω collector resistors is increased by a factor of 4, which corresponds to a 12 dB increases in power due to the parallel combination at the output. Since the maximum available output power of the long-tailed pair is set by the quiescent current through each transistor, this is also increased by 12 dB. The gain of the amplifiers can be compared by considering both the increase to the output power and the -6 dB at the input to each differential amplifier subcircuit due to the power splitter. The gain of the quad amplifier compared to the single amplifier is then increased by $12\ dB - 6\ dB = 6\ dB$.

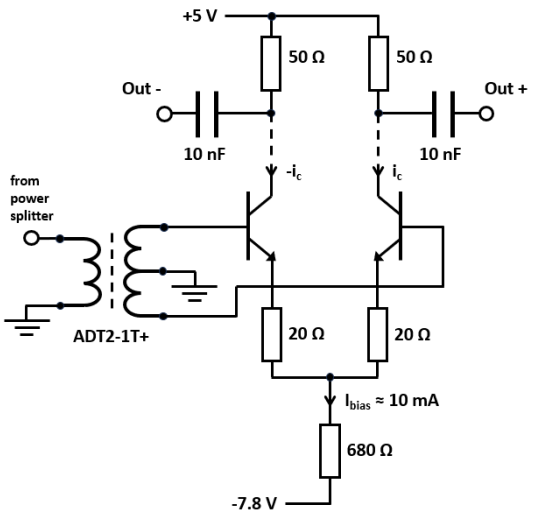

Fig. 5. A single long-tailed pair differential amplifier subcircuit used in the quad parallel differential amplifier

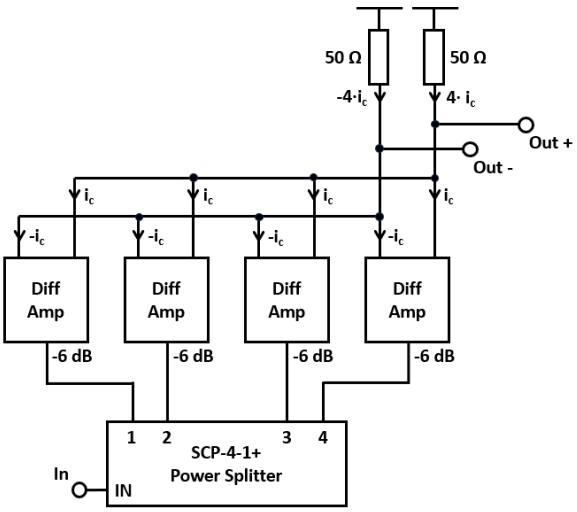

Fig. 6. Block diagram of the quad parallel differential amplifier

B. Measurements

The amplifier has a small-signal gain of 7.6 dB and the 1 dB gain compression point occurs for an output power of around 3 dBm. The noise figure was measured to be 3.8 dB using an R&S FSWP.

Since the close-to-carrier residual phase noise of the amplifier was found not to be sufficiently above the internal noise floor of available residual noise measurement systems, the flicker noise corner of the amplifier, f_c was determined by measuring the absolute phase noise of the oscillator where the crystal was replaced with a comparatively low Q LC resonator. The $1/f^3$ to $1/f^2$ transition point of the oscillator phase noise measurement corresponds to the flicker noise corner of the amplifier [7]. This method was used to determine that the f_c of the amplifier for an output power of 5 dBm is around 80 Hz.

V. Attenuator Placement

The placement of the attenuator at the input of the amplifier was selected to mitigate against issues relating to the impedances presented to the crystal and the amplifier when in the oscillator loop.

The ratio of the loaded Q to the unloaded Q of the crystal, Q_L/Q_0, is an important factor is designing low phase noise oscillators. It is shown in [8] that minimum phase noise occurs when Q_L/Q_0 is equal to approximately 0.5 and can be calculated as follows:

$$\frac{Q_L}{Q_0} = \frac{R_{loss}}{R_{in} + R_{out} + R_{loss}} \tag{1}$$

Where R_{loss} is the effective series resistance of the crystal, R_{in} is the source impedance at the input and R_{out} is the load impedance at the output.

If a crystal is designed for optimal Q_L/Q_0 in a 50 Ω system, then a deviation in the load impedance could result in degradation of the phase noise.

The residual phase noise of an amplifier is also typically characterised for use in a 50 Ω system. The noise performance of an amplifier is often dependent on the source impedance that is presented to it, so if an amplifier with low measured residual phase noise is placed in an oscillator loop where the source impedance is different, the oscillator phase noise could be worse than expected.

A. System Impedances

Fig.7. a) shows a simplified block diagram of the oscillator including only the resonator, amplifier and an attenuator matched to a 50 Ω system at the output of the amplifier. The amplifier is assumed to have an output impedance of 50 Ω, which in the case of the quad parallel differential amplifier is set by the collector resistor, and the output impedance of the attenuator is therefore also 50 Ω. The output impedance of the resonator is represented by Z_R and in this configuration, this is also the source impedance that is presented to the amplifier input, which could affect the noise performance of the amplifier. Similarly, the input impedance of the amplifier, represented by Z_A, is the load impedance presented to the resonator. If Z_A deviates from 50 Ω, which is true in the case of the quad parallel differential amplifier, this could degrade the phase noise by affecting the ratio of Q_L/Q_0.

Fig.7. b) shows the configuration where the attenuator is instead placed at the input to the amplifier. Here the load impedance presented to the resonator is instead the effective input impedance of the attenuator, Z_{in}, and the source impedance presented to the amplifier is the effective output impedance of the attenuator, Z_{out}. It can be shown that Z_{in} and Z_{out} will become closer to 50 Ω as the amount of attenuation increases.

B. Attenuator Impedance Transformation

A resistive attenuator can be modelled as a pi-pad network as shown in Fig.8, where the values of the resistors R_A and R_B can be calculated as follows:

$$R_a = Z_0 \cdot \frac{1+K}{1-K} \tag{2}$$

$$R_b = Z_0 \cdot \frac{1-K^2}{2 \cdot K} \tag{3}$$

Where K is the attenuation of the device in terms of V_{out}/V_{in}.

The effective input impedance of the attenuator when terminated with a load resistance, R_L, can then be calculated by considering the resulting resistor network as follows:

$$Z_{in} = R_a \parallel (R_b + (R_a \parallel R_L)) \tag{4}$$

If Z_0 is 50 Ω then it can be seen from (2) that as K decreases (i.e. for a higher level of attenuation), the value of R_A will tend towards 50 Ω, and from (3) that the value R_B will become much greater than 50 Ω. Applying these to (4) it can be seen that as the level of attenuation increases, the effective input impedance of the attenuator will become closer to 50 Ω even if R_L is mismatched. Since the device is symmetrical the inverse is also true, the effective output impedance of the

attenuator will become closer to 50 Ω even if R_S is mismatched.

Therefore it is believed that the placement of the attenuator at the amplifier input can help to mitigate against degradation of phase noise due to impedance mismatch between the resonator and the amplifier.

VI. Oscillator Measurements

The absolute phase noise of the oscillator is shown in Fig.9. It was measured using an R&S FSWP and a smoothing function has been applied so that frequency spurs, particularly that at 100 Hz due to mains interference, can be ignored. This can be seen overlayed on the raw measurement.

The phase noise at 100 Hz can be seen to be just below -140 dBc/Hz and the far-out noise floor is around -168 dBc/Hz.

VII. Conclusions

A 100 MHz crystal oscillator has been developed that demonstrates phase noise performance comparable to state-of-the-art commercially-available oscillators. Each of the constituent parts of the oscillator has been described in detail and a flexible approach in the construction of the oscillator has been demonstrated.

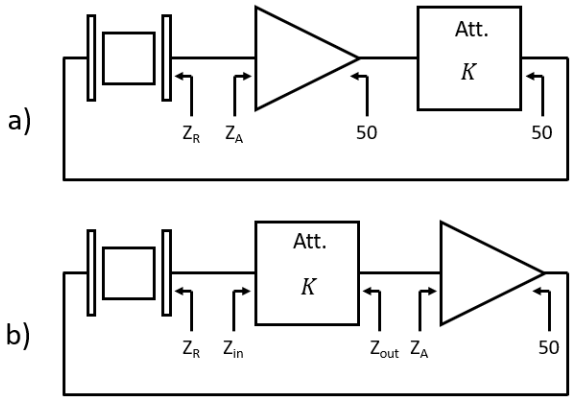

Fig. 7. Simplified block diagram of the oscillator to demonstrate the effects of pre-amplifier and post-amplifier attenuation

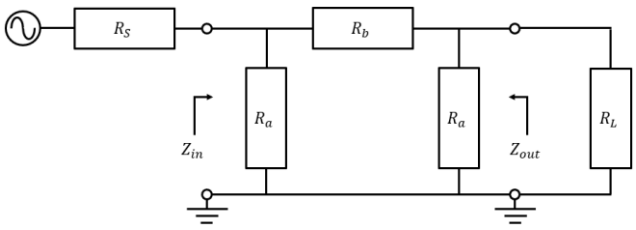

Fig. 8. Equivalent circuit of a resistive attenuator placed between source and load impedances

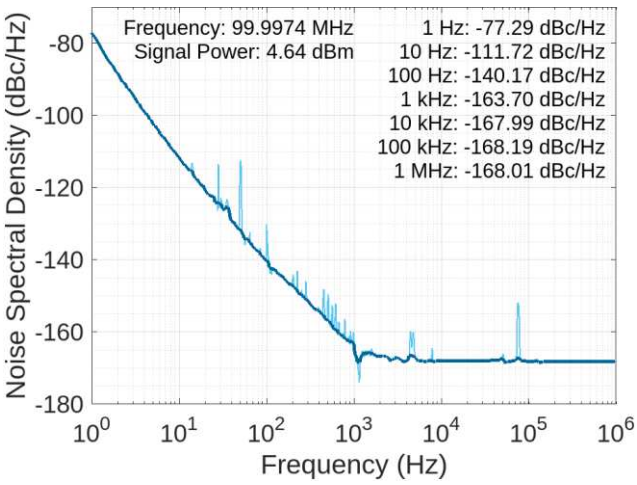

Fig. 9. Oscillator phase noise measured using the R&S FSWP

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