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Ali, Basit, Özkan, Sena Nur, Kerimzade, Umut et al. (5 more authors) (2024) Stencil-Based Selective Surface Functionalization of Silicon Nanowires in 3D Device Architectures for Next-Generation Biochemical Sensors. ACS Applied Nano Materials. pp. 10634-10647. ISSN 2574-0970

https://doi.org/10.1021/acsanm.4c01065

Stencil-Based Selective Surface Functionalization of Silicon Nanowires in 3D Device Architectures for Next-Generation Biochemical Sensors

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KEYWORDS: silicon nanowire, surface functionalization, 3D MEMS devices, stencil lithography, extracellular matrix, heparin.

Abstract: Surface functionalization of 1D materials, such as silicon nanowires, is a critical preparation technology for biochemical sensing. However, existing non-selective functionalization techniques result in non-local binding and contamination, with potential device damage risks. Associated risks are further exacerbated for next-generation devices of a 3D nature with challenging topographies. Such 3D devices draw inspiration from the out-of-plane evolution of planar transistors to FinFETs and to today's gate-all-around transistors. This study is the first reported technological work addressing stencil-based surface decoration and selective functionalization of a suspended silicon nanowire building block embedded within such a device that involves two-order-of-magnitude thicker features compared to the nanowire critical dimensions. A gold pattern resolution of 3.0 µm atop the silicon nanowires is achieved with a stencil aperture critical dimension of 2.2 µm, accompanied by a die-level registration accuracy of 1.2±0.3 µm. Plasma-enhanced chemical vapor deposition-based silicon nitride stencil membranes as large as 300×300 μm^2 are used to define the apertures without any membrane fracture during fabrication and membrane cleaning. The pattern blurring aspect as a resolution-limiting factor is assessed using 24 individual nanowire devices. Finally, gold-patterned silicon nanowires are functionalized using thiolated heparin and employed for selective attachment and detection of

human recombinant basic fibroblast growth factor (FGF-2). With the potential involvement in angiogenesis, the process of new blood vessel formation crucial for tumor growth, FGF-2 can serve as a potential prognostic biomarker in oncology. Demonstrated selectively on nanowires with high pattern resolution, the proposed functionalization approach offers possibilities for parallel sensing using vast nanowire arrays embedded in 3D device architectures developed for next-generation biochemical sensors in addition to serving various encapsulation and packaging needs.

1. Introduction

1D nanostructures such as nanowires (NWs), nanodots, and nanotubes have drawn considerable interest in the past decade owing to their wide-ranging applications in biomedical devices, biochemical and physical sensors, and energy storage systems.[1–7] Performance improvements achieved through NW use, such as high sensitivity and low limit of detection, low power requirements, efficient use of real estate, and fast response time remain unmatched by their microscale counterparts.[3,6,8,9] Mainly reported as laboratory-scale demonstration studies, their full potential can only be improved with appropriate production and preparation techniques that are batch-compatible, i.e., applicable to parallel operation over nanowire arrays with the potential of automation. Among all 1D materials, semiconductor silicon nanowires (Si NWs) are leading candidates for next-generation sensor systems due to their ubiquitous use, IC compatibility, mature manufacturing technologies, and well-understood semiconductor and piezoresistive behavior.[6,10,11]

Semiconductor device architectures continuously transform from planar to 3D systems in commercial CMOS electronics in pursuit of enhanced performance, minimized footprint, and lower power requirements, such as the nanoplate stacks used in gate-all-around (GAA) transistors.[12] This transformation to 3D architecture has already been evident from the growing interest of the semiconductor market in the transition from planar to nonplanar transistor

architecture. Over the last two decades, this transition resulted in successful technology nodes incorporating fin-type field effect (FET) to GAA transistors.[13–16] It is the semiconductor manufacturing technologies rather than bottom-up synthesis, such as vapor-liquid-solid (VLS) growth that can answer to the strict requirements of system-level alignment and dimensional tolerances, which are necessary for acceptable levels of production yield. Among such challenging applications are the next-generation physical sensors based on the integration of Si NWs with microelectromechanical systems (MEMS),[6,9,17–19] where 3D topography and related technology challenges are to be addressed within the bounds of batch fabrication.

Similarly, the augmented surface-to-volume ratio and miniature size of Si NWs enable highly sensitive detection of gases, biological molecules, and cells, along with tissue-based engineering strategies.[8,24–27] A few examples include metal ions, chemical gases such as hydrogen, key biomarkers and various biological antigens. [8,28–32] Furthermore, functionalized Si NWs hold the potential for detection of key biomarkers for conditions such as wound healing and cancer. For example, elevated levels of fibroblast growth factor (FGF-2)[1] in tumor conditions is often a sign that the cancer is more aggressive or likely to progress at a faster rate. Hence, detection holds the potential for determining the therapeutic course of action.[33]

As bare Si NWs do not bind to biochemical substances, their surface functionalization is a prerequisite for any such sensor application. This functionalization involves modifying or coating the NW surface through techniques such as salinization, self-assembled monolayer, polymer, or

[1] FGF-2 is a protein that plays a role in cell growth, proliferation, and differentiation, hence being involved in various biological processes, including angiogenesis, wound healing, and embryonic development.[68]. In cancer, FGF-2 can promote tumor growth by stimulating the proliferation of cancer cells and the formation of new blood vessels through angiogenesis. By promoting cell growth and survival, FGF-2 can also enhance resistance to treatment. Therefore, FGF-2 being a potent inducer of angiogenesis serves as a potential target for anti-cancer therapies.[69]

oxide coating, which facilitates the binding of the target analyte to the NW surface.[34–38] Although the choice of functionalization techniques depends on the desired application, available Si NW surface functionalization approaches rely on non-selective protocols, potentially resulting in analyte binding to the Si NW surface as well as to the remaining Si areas exposed on the substrate. Therefore, any process steps that modify the surface properties of Si NW also change the surface characteristics of the Si substrate, upon which the employment of functionalization technologies potentially causes additional issues due to the corrosive nature of the chemicals and expensive or lengthy multi-step functionalization processes.[39,40] In addition to biological functionalization, specific needs for the encapsulation or surface protection of Si NWs might arise leading to similar challenges mentioned above.[31,41,42]

Although the majority of prior work addressing such surface modifications is based on non-selective surface coating,[28,29,32,36–38,43–46] few solutions that exist for selective functionalization employ microchannels for guiding the target analyte to the NW region,[31,41,42] an exceptionally challenging technique for suspended NWs. An alternative approach based on resist lift-off was also reported for chemical sensing.[2,47,48] However, no technique can fully avoid surface contamination risks. It is clear that with the 3D multiscale device architecture of next-generation sensors, such technology requirements will become more challenging and multifaceted, for which no viable solutions exist to the best of the authors' knowledge.

Stencil lithography (SL) emerges as a unique approach addressing most of the aforementioned challenges regarding surface metalization of Si NW in 3D architectures. It is, in principle, a shadow mask technique with the potential of selective and lift-off-free functionalization through surface patterning without any contamination and non-local binding risks for adjacent components and systems on the chip. The stencil employed in this technique involves an aperture fabricated in a

thin membrane positioned in close proximity to the substrate, followed by material deposition via physical vapor deposition (PVD). This results in a selective coating of the region below the aperture.[49] Surface patterning via SL offers significant advantages, including reduced fabrication process steps and minimized complexity, along with the reusability of the stencil.[4,50] However, despite the benefits, the SL of suspended Si NWs in a 3D multiscale device architecture is particularly challenging due to the miniaturized feature size, potential substrate-stencil contact-induced damage to suspended NWs, and the 3D topography. Therefore, the available literature on NW SL mainly involves planar architectures,[8,51,52] with only a few exploring SL for Si NWs embedded within a 3D multiscale device architecture.[53,54] However, large aperture widths and spacer thicknesses limit both the pattern resolution and the coating thickness, making sub-10µm selective patterning a challenging task. For example, for a standard Si NW length of 10 µm, the recently demonstrated minimum pattern resolution of sub-15µm range[54] poses electrical short circuit risks. More importantly, for compatibility with semiconductor manufacturing, achieving such resolution at the wafer-level raises the need for the development of strategies and related integration philosophies for alignment. Thus, the existing SL-based approaches have to be improved and adjusted for surface patterning of Si NW for biochemical applications. This entails achieving pattern registration accuracy down to 1µm, development of alignment strategies for chip-level NW patterning, improvement of the patterning resolution to sub-5 µm level through miniaturization of the stencil aperture and spacer thickness, and finally, potential demonstration of the surface functionalization of Si NWs embedded within challenging 3D architectures such as MEMS.

In the remainder of this paper, the SL approach based on the preparation of a nitride membrane with an aperture will be described first, followed by the details of the stencil and Si NW-based 3D

multiscale device architecture. An explanation of the alignment procedure between the stencil and the chip, containing multiple NW devices, will be described in the subsequent section. Later, we present the results regarding chip-level selective patterning along with investigating the parameters affecting the pattern resolution. Selective patterning is later verified through selective surface functionalization of Si NWs via heparin and through selective binding and detection of the FGF-2.

2. Methodology for Selective Surface Functionalization of Si NW

Selective surface metallization of single-crystalline suspended Si NWs is performed, followed by functionalization and detection of ligand-heparin interactions , as depicted in **Figure 1**. Figure 1a shows the device layout with the free-standing Si NW embedded within a two-order-of-magnitude thicker MEMS structure. Both components are generated by etching the same silicon-on-insulator (SOI) substrate device layer, as explained elsewhere.[11] Selective patterning is performed via SL, Figure 1b, where a gap-controllable stencil is designed with an embedded spacer to avoid direct contact between NW and stencil and, hence, any potential damage to NW during SL. After the stencil assembly with the die containing NW, metal deposition through PVD is carried out (Figure 1b). Deposition selectively coats the NW surface via the stencil aperture while the rest of the die surface remains protected. After the deposition, the stencil is removed from the die, thereby exposing selectively coated NW metal on the die surface (Figure 1c). The utilized approach is demonstrated to selectively coat the NW surface with pattern resolution down to 3 µm. Functionalization is then demonstrated by the selective binding of thiolated heparin onto a gold-

coated NW surface, followed by further validation through ligand- extracellular matrix (ECM[2]) molecule interactions on the gold-patterned NW surface (Figure 1d).

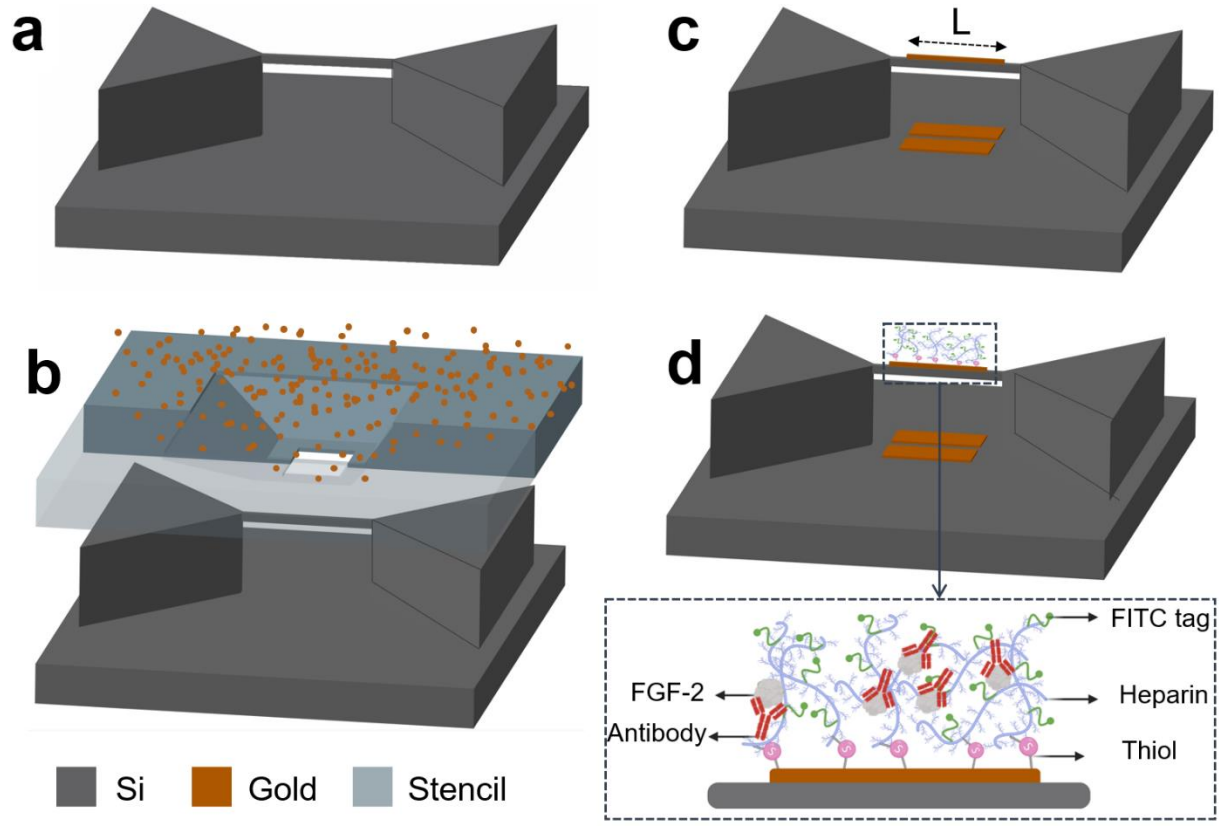

Figure 1. Schematic of the selective surface functionalization process of Si NWs within a multiscale device architecture. (a) suspended Si NW integrated with a 3D multiscale device. (b) Selective metallization of Si NW via SL, where the mask is depicted in an isometric view with an aperture machined at its center. (c) Patterned Si NW across a region of length L. (d) Conjugation

[2] Extracellular matrix (ECM) is a highly complex heterogenous entity specialized for distinct tissues to provide structural support to cells.[70] The unique interactions of the cells with their surrounding ECM regulate physiological processes in tissue homeostasis and disease. ECM components such as sulfated glycosaminoglycans (sGAGs) control the availability of ligands and their interactions with cells via exerting tunable affinity towards them.[71]

of Fluorescein isothiocyanate (FITC)-labeled thiolated heparin onto Si NW via thiol-gold coupling followed by selective antibody and growth factor (FGF-2) attachment.

2.1. Stencil and Si NW-Based 3D Device Architecture

For selective patterning of Si NW, the stencil aperture is made out of a thin Si nitride (Si_xN_y) membrane (Figure S1), where Si_xN_y is chosen due to its robust nature and excellent etch selectivity against Si and various metal etchants.[4,50] This ensures successful manufacturing as well as reusability despite repeated cleaning against aperture clogging without any significant damage to the membrane.[4,50,53] Moreover, a spacer with controllable thickness h (0.5 µm<h<90 µm) is available on the stencil to prevent direct stencil-die contact during SL, thereby avoiding any potential contact-induced damage to the fragile suspended NW. **Figure 2a** shows a scanning electron microscope (SEM) image of the top view of the stencil. The stencil is made out of a 525 µm-thick double-side polished Si wafer, coated with a 100nm-thick Si_xN_y layer on both sides by plasma-enhanced chemical vapor deposition (PECVD). Selective removal of Si_xN_y from the top surface, followed by KOH etching of the Si, results in the Si_xN_y membrane at the bottom. Subsequent maskless lithographic patterning and etching of this Si_xN_y membrane by reactive ion etching (RIE) in CHF_3 chemistry results in an opening, referred to as the stencil aperture. Stencil aperture width, in this case, represents the critical dimension (CD) during the patterning of the stencil mask. The inset of Figure 2a shows the cross-sectional view of the stencil, depicting both the characteristic V-shaped anisotropic profile of KOH etching and the membrane at the bottom, which is partially fractured during cleavage. Raw image of the stencil and its cross-sectional view without false coloring are provided in supporting information (Figure S2).The rigidity of the Si_xN_y in stencil membrane is an important aspect in avoiding membrane rupture during stencil fabrication or the SL process. The use of PECVD not only simplifies the stencil fabrication process but also

reduces the thermal budget of the fabrication. Although low-pressure chemical vapor deposition (LPCVD)-based approaches with process temperatures in excess of 425 °C are usually utilized as compared to the low-temperature PECVD technique due to their low intrinsic stresses, careful optimization of the PECVD deposition parameters is shown here to yield successful membranes and stencil apertures with extra-large membrane sizes of 300×300 μm^2, with rupture occurring only for the increased membrane size due to insufficient membrane rigidity and residual stresses (Figure S3-S4).

The spacer, made out of thick photoresist, is fabricated on the backside through maskless lithography followed by hard baking (Figure S5). The patterning of the spacer onto the stencil is conducted before the stencil aperture is fabricated.

Conventional approaches for the use of a spacer to maintain a safe stencil-substrate gap include employing Kapton® tapes [55] or photoresists [56] or generating protrusions on the stencil by etching.[57] Moreover, these approaches need coating/removal of single-use photoresist or Kapton® tape onto each substrate every time SL is conducted onto it to maintain the stencil-substrate gap. Additionally, electrostatic approaches were also reported,[58] with few works putting the stencil in direct contact with the substrate.[59] However, most of the prior work conducted on planar substrates does not address specific challenges associated with SL for 3D multiscale device architecture with suspended NWs. For example, a much lower spacer thickness, especially below 20 μm, is required to improve pattern resolution while minimizing blurring. Moreover, surface contamination resulting from the spin-coating photoresist onto substrate or limitations available with achieving and handling lower thickness of Kapton® tape (sub-20 μm) as well as potential damage of fragile NWs due to the use of high electromagnetic forces in electrostatic clamping render these techniques incompatible. Our approach offers a dry and fixed spacer-embedded stencil with

controllable spacer thickness down to 0.5 µm in order to minimize blurring and improve pattern resolution. This, in turn, provides a multi-use spacer embedded directly onto the stencil, without any placement and removal efforts for photoresist/Kapton tape® and the contamination they bring, each time SL is conducted.

Figure 2b shows an SEM image of the device architecture obtained through a recently developed top-down monolithic fabrication technology.[11,53,60] Overall, it provides an overview of the geometry representative of the 3D multiscale device architectures involving nanoscale transduction element as well as thick microelectromechanical systems (MEMS) structure,[53] on which selective patterning will be carried out on the NW region only. A close-up view of the NW region features a released Si NW anchored from its extremities to the surrounding MEMS structure. It has a CD of 100 nm, whereas MEMS thickness is 10 µm. In comparison with the available alternative approaches, which involve the fabrication of the Si NW at the bottom of the device layer defined by the deposition of a thicker poly-Si layer for MEMS,[3,9,10,18] the utilized approach allows i) monolithic fabrication of Si NW and MEMS within the same crystal, and hence, a strong interface between and lithographic definition of Si NW crystal orientation, and ii) post-processing steps such as encapsulation, surface preparation, contact formation, and doping, as the NW is strategically placed at the top surface of the device.

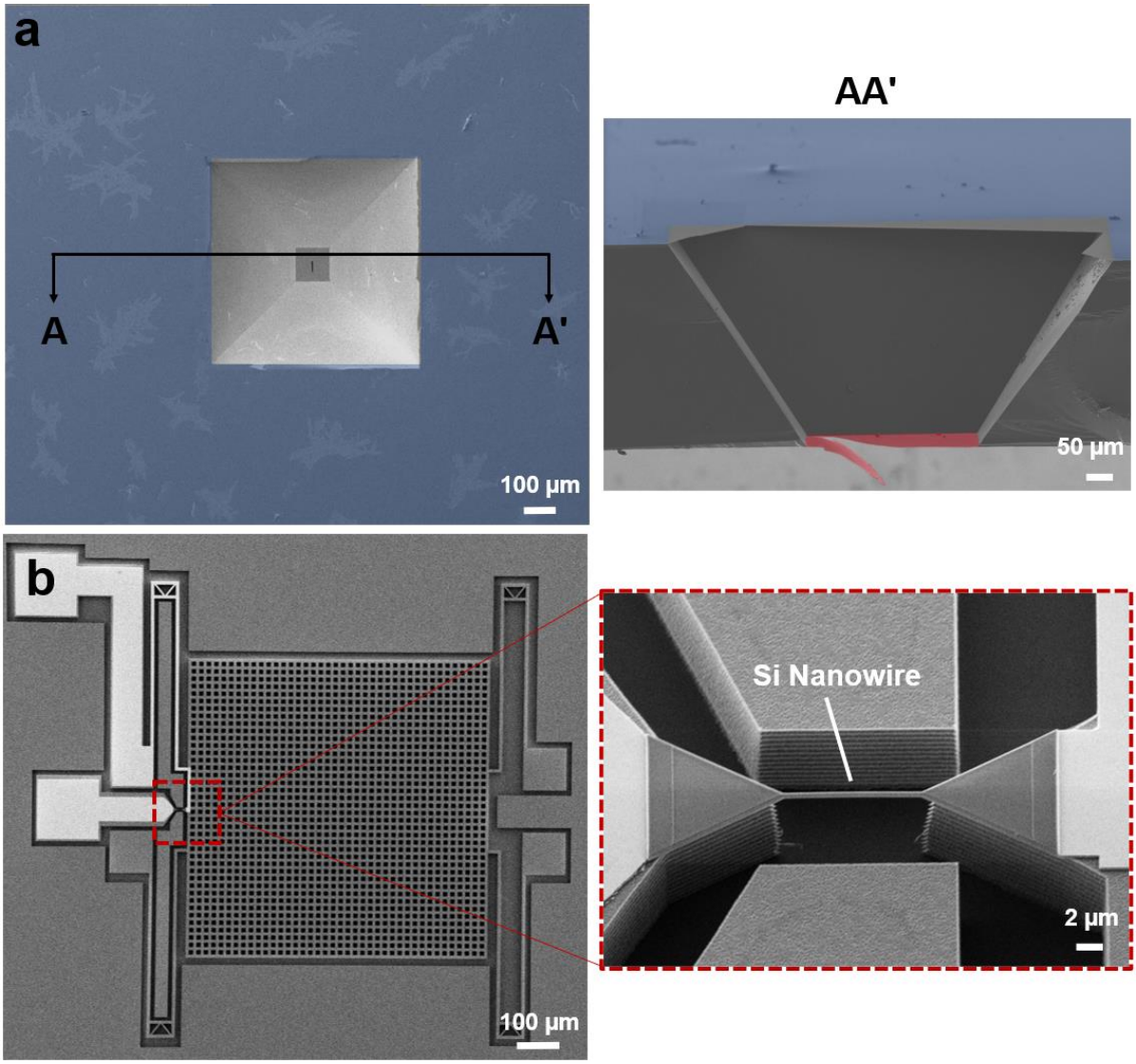

Figure 2. Stencil and the Si NW-based multiscale device utilized for the patterning of Si NW. (a) SEM image of the stencil and cross-section AA'. False coloring is used to designate the upper surface and the Si_xN_y membrane at the bottom. (b) Si NW-based 3D multiscale device with a close-up depicting the NW region. Raw SEM images of panel (a) without false color are available in Figure S2.

2.2. Alignment and Metallization

A micromanipulation setup with seven degrees of freedom (DOF) is designed for the alignment between stencil and die (**Figure 3a**). The setup involves a set of computer-controlled motorized actuators, allowing translational and rotational movement to control the relative position of the NW and stencil in an independent manner (Figure S6). All translational motorized actuators have a resolution of 200nm, while the rotational stage – chosen due to its provision for large rotation angles – is controlled manually with a sensitivity of 24 μrad. For manipulation, the stencil is placed inside the holder and fixed via 3D-printed compliant clamps, whereas the chip is placed on the rotational stage without any clamping. The position of the chip can be adjusted in four DOFs (three translations and one rotation around the Z axis), while the holder (encompassing chip and stencil) has 2 DOFs (in-plane translational motion through an auxiliary set of computer-controlled alignment stages). Through auxiliary stage movement, the setup moves as a whole under the objective lens. Hence, the relative position of the chip and the stencil is kept fixed, overcoming vibration-related issues.[54] The stencil-chip alignment procedure is performed in two steps. Course alignment (including θ_z) is followed by fine alignment, which should ideally provide alignment accuracy up to sub-2 μm. The details for the alignment procedure are provided in the experimental section.

Alignment and patterning features are depicted in false color in Figure 3a. Alignment is carried out with the bigger square openings in the stencil (depicted in green) that are aligned with the square pads on the die. This alignment leads to the chip-level registration and placement of the stencil aperture on the midsection of each NW (Figure S7), which is necessary for patterning, as depicted in pink.

Optical micrographs of a stencil and a die are presented with the same magnification in Figure 3b. Each die hosts 8 NW devices, numbered D1-D8, with an overall chip size of 12×12 mm^2. The

stencil holds the same number of apertures. Two of these stencil apertures ($D4$ and $D5$) are used for alignment purposes, as explained above. The SEM micrographs on the right (in green) depict the alignment features both on the stencil and the die. The closeup of the SEM micrograph depicts the alignment aperture with a size of 140×140 μm^2 patterned within the stencil membrane. This clearly highlights the structural integrity of the rather fragile nitride membrane despite the aperture of rather large dimensions. On the die, a pad of the same size (lower SEM micrograph) is used for alignment purposes. Despite the fact that the pads were not designed strictly as alignment marks, the resulting success of alignment indicates the promising nature of the proposed technique. Following the alignment, the desired position of the stencil aperture above the die is depicted by the red line. Similarly, corresponding patterning features are depicted in pink on the left-hand side.

The resulting stencil-NW chip assembly is removed from the holder by untightening the stencil clamps and mounted on a carrier substrate, followed by verification of the alignment accuracy via an optical microscope. Figure 3c provides a practical demonstration of the alignment performance. Both the stencil aperture and the underlying nanoscale features can be observed under the microscope thanks to the transparency of the 100nm-thick Si_xN_y membrane. Due to the presence of a 10µm-thick spacer between the stencil and the underlying die, this requires a change of the focus plane, thereby providing point-by-point verification of alignment success. More on the quantification of the pattern registration accuracy will be provided in the Results section.

Following the validation of stencil aperture-NW alignment, surface metallization (5 nm of Cr / 100 nm Au) is carried out via e-beam evaporation. To eliminate any errors induced by the transfer and mounting of the stencil-NW chip assembly, the assembly is first mounted onto a carrier wafer (Figure S8) and then fixed through Kapton tape onto the holder of the e-beam evaporation

chamber. Following the gold deposition, the stencil-NW chip assembly is removed from the carrier wafer and separated from each other.

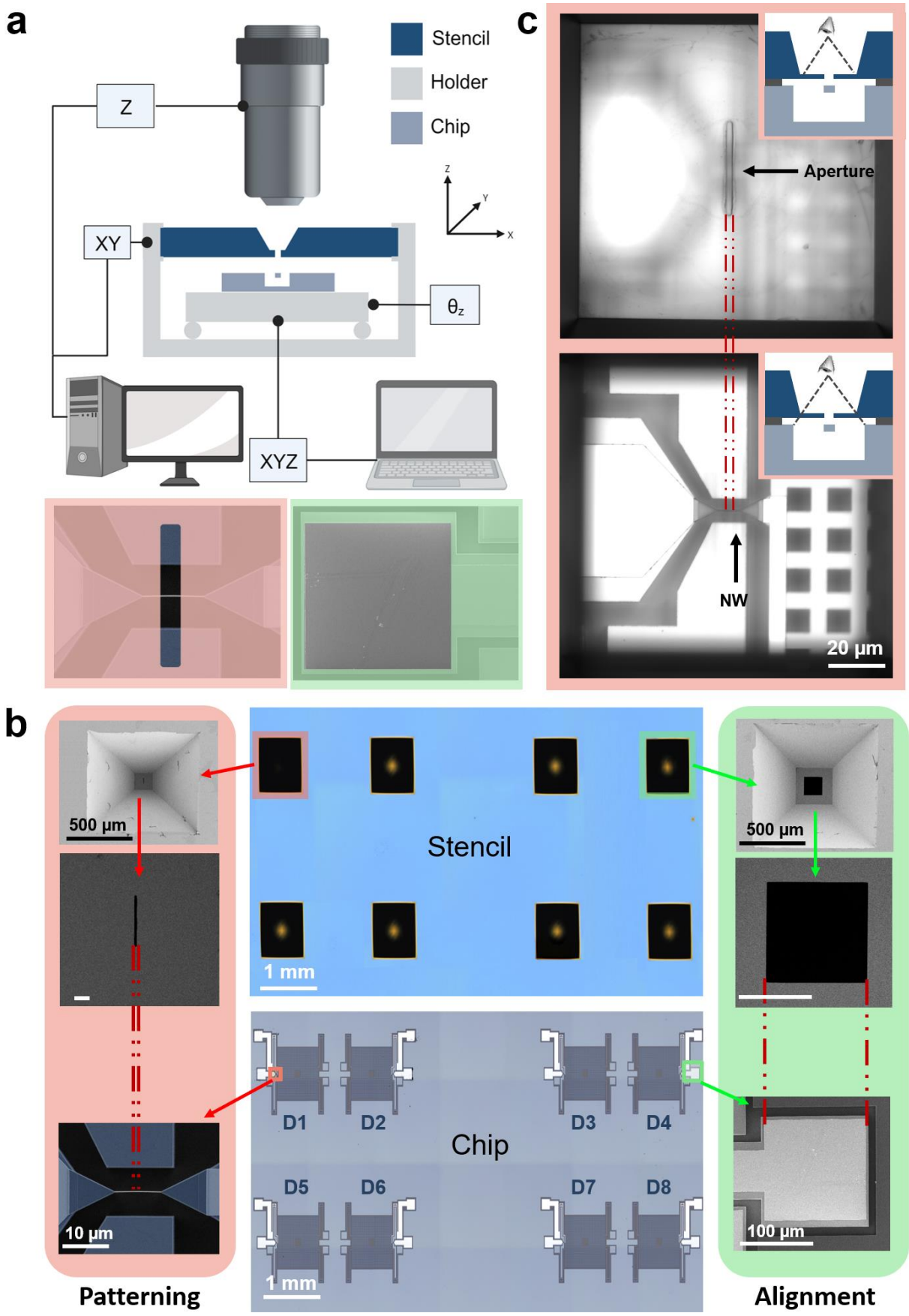
a
Stencil
Holder
Chip
Z
XY
θz
XYZ
c
Aperture
NW
20 μm
b
500 μm
10 μm
Patterning
Stencil
1 mm
D1
D2
D3
D4
D5
D6
D7
D8
Chip
1 mm
500 μm
100 μm
Alignment

Figure 3. (a) Schematic of the 7 DOF micromanipulation setup with representative alignment and patterning features highlighted in green and pink, respectively. (b) Representative layout for the stencil and the die with eight devices. Both patterning and alignment features depict apertures and the underlying architecture on the die. While $D4$ and $D5$ along the die diagonal are used for alignment, the rest of the layout can be directly patterned via SL. (c) Stencil aperture-NW alignment verification via optical imaging of the stencil aperture and Si NW (underneath stencil) after alignment. With the transparent stencil membrane, it is possible to focus both on the stencil aperture (top panel) and the Si NW underneath.

3. Results and Discussion

3.1. Patterning

SEM is utilized to study gold coating on Si NWs, **Figure 4,** and to investigate resolution limiting factors such as blurring, **Figure 5**. First of all, Figure 4a shows the particular stencil aperture geometry for which the subsequent patterning analysis is carried out. The specific rectangular aperture shape is chosen due to its ease of detection after metalization, both in the confocal microscope and in SEM. Additionally, the selected stencil aperture geometry design allows leniency in the alignment process. This way, the critical alignment direction is confined to the transverse direction, i.e., along the width of the aperture.

Figure 4b shows a sample gold metallization pattern on the NW with a close-up in Figure 4c. A comparison of the dimensions of the gold pattern with that of the aperture (10 μm spacer thickness) indicates a widening, which will be discussed later under blurring. Further widening of the gold pattern at the bottom of the 10-μm-thick Si device layer, also visible in Figure 4c, compared to

that on the NW, verifies the blurring effect, as it is a direct outcome of the increase in the gap to stencil. The presence of gold on NWs is further validated by energy-dispersive X-ray spectroscopy (EDX)-based elemental mapping of the NW for the Si, Au, and their combination (closeup in Figure 4c). In this context, while EDX measurements validate the successful metallization, the SEM image functions as a reliable tool for ascertaining the width of the gold patterns and, thus, the pattern resolution achieved with SL. For a minimum aperture width of 2.2 µm, the gold pattern resolution on the die is found to be 3.0 µm.

The success of chip-level patterning is quantified by registration accuracy or overlay[61,62]. Registration accuracy is defined as the amount of positioning error in the overlap of the centers of the gold pattern and Si NW. For this purpose, the whole 12×12 mm^2 area of the die is considered in Figure 4d with six devices patterned ($D1-3$, $D6-8$) and two devices employed for alignment ($D4$ and $D5$) as discussed above in Figure 3, with chip-level low-magnification views are provided in Figure S9. Figure 4e represents a schematic layout of the NW devices distributed over the 12×12 mm^2 chip, indicating alignment devices $D4-D5$ with a microscope symbol. Registration accuracy is calculated as 1.2±0.3 µm by considering the remaining six devices. It is pertinent to mention that the achieved level of registration accuracy is obtained using the already existing alignment pads with a quite large size of 140×140 μm^2. Further engineering of the alignment marks will surely enhance the registration accuracy to submicron levels. In comparison to the state of the art regarding the patterning resolution of NWs inside 3D architectures,[54] a 5-fold improvement is achieved due to the engineering of aperture CD and spacer thickness. The demonstrated pattern resolution combined with chip-level patterning and pattern registration accuracy of 1.2±0.3 µm offers the parallel processing of multiple NW devices within a single chip. This new set of

developments enables Si NW surface patterning with thickness more than 100nm without any electrical short circuit. Electrical characterization of the NW after gold SL verifies the same.

E-beam evaporation is utilized due to its directional deposition nature and longer (~1 m) mean free path. It predominantly coats NW top surface as opposed to its sidewalls. Although this proved to be sufficient for microscope-based characterization of the current work, other deposition techniques such as sputtering or atomic layer deposition can be used to utilize hidden sides of the NW transducer.[53] However, as the critical dimension of the stencil aperture is sub-50 μm, one should be careful in selecting a deposition technique. For example, in the case of sputtering, reduced mean free path and resultant low directionality of to-be deposited metal particles, compared to e-beam evaporation, could significantly affect the deposition yield onto the substrate through the stencil aperture.

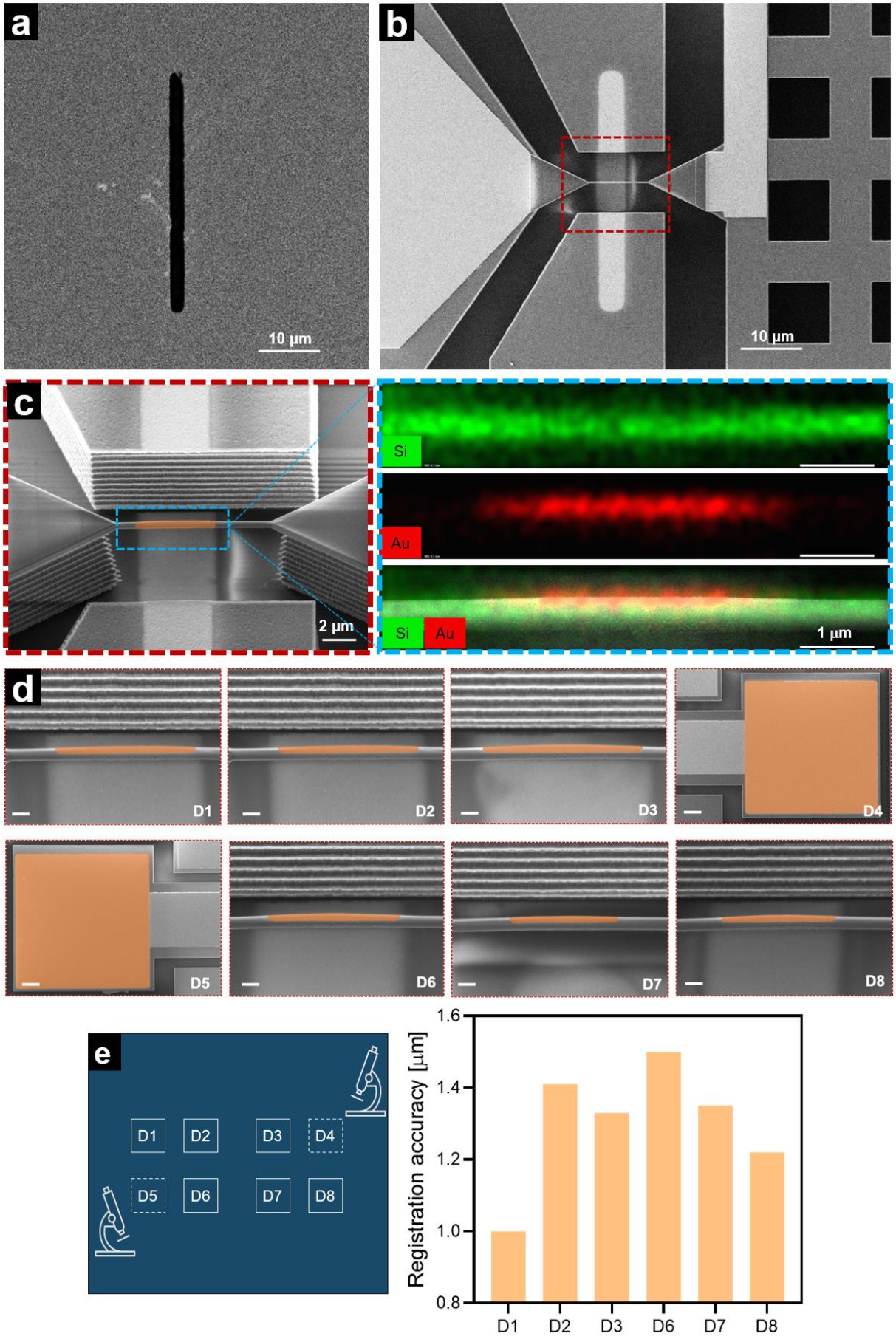
a
10 µm
b
10 µm
c
2 µm
Si
Au
Si
Au
1 µm
d
D1
D2
D3
D4
D5
D6
D7
D8
e
D1
D2
D3
D4
D5
D6
D7
D8
Registration accuracy [µm]
1.6
1.4
1.2
1.0
0.8
D1
D2
D3
D6
D7
D8

Figure 4. Selective gold patterning of Si NWs. (a) SEM micrograph of the particular stencil aperture. (b) SEM micrograph of the corresponding metallization pattern on the die with Si NW. (c) Close-up view of the gold-coated region in false color. The right panel shows verification of the presence as well as the amount of spread of the gold pattern via EDX-based elemental mapping. (d) Success of chip-level selective gold patterning, with the demonstration of minimum pattern resolution of 3 μm. Scale bars designate either 500 nm for devices $D1-3$, and $D6-8$ or 20 μm for $D4-5$. (e) Registration accuracy across the 12×12 mm^2 die containing 6 NW devices.

3.2. Blurring Effect and Repeatability

Blurring is defined as the unintended enlargement of the feature size patterned on the die compared to the dimensions of the stencil aperture. It is a function of the stencil-die gap, evaporation source size, evaporation source to stencil aperture distance, and type of substrate material.[1,55,57] To analyze specifically the effect of spacer thickness as a SL component, a series of different spacer thicknesses were employed on blank Si dice using the same e-beam evaporation equipment and configuration. Hence, any geometric blurring observed during the process depends entirely on the stencil-die gap.

Figure 5a shows the main set of geometrical parameters required in the treatment of blurring. The stencil aperture of width w is kept apart from the substrate by a spacer of thickness h. Surface coating via line-of-sight deposition by evaporation leads to a pattern of width, x, and a thickness of v. x is usually greater than w, with the increase becoming prominent at higher h, an indication of lateral blurring. On the contrary, v usually drops as h increases. For a thorough characterization, SL is conducted on a bare Si surface with h=0 μm (direct contact), 10 μm, and 90 μm. A direct contact scenario is used to benchmark the minimum level of blurring. SL is performed at six

different spots for repeatability purposes, where all sites are found to exhibit the same blurring behavior.

Figure 5b provides the AFM-based 3D profile of the pattern obtained for different h. Pattern width is observed to increase with increasing h (Figure S10). To gain further insight, 2D line scans (through the midsection of the line patterns) are plotted in Figure 5c. Without any spacer, minimum blurring is obtained with nearly vertical sidewalls. With the introduction of the spacer, linewidths, x, increase while their sidewalls change from nearly vertical to a slanted configuration. x for h=90 µm turns out to be more than double the value for the case of direct contact. Finally, v drops from roughly 110 nm to 65 nm with h=90 µm. Using spacer-embedded stencil allows us to investigate blurring with much lower stencil-die gaps (as low as 10 µm for the current case). This surpasses the blurring investigations previously reported with Kapton® tape spacers with a minimum thickness of 25 µm.[55] Figure 5d provides a detailed picture of the evolution of blurring as a function of h as well as w. Although h is fixed to 10 µm for all SL work on NWs, further reduction in h can be the most practical way forward to improve the pattern resolution for a given stencil geometry.

Finally, figure 5e shows the dependence of the pattern length, L, on the stencil aperture CD for h=10 µm. The trend also indicates SL repeatability upon repeated use of the same stencil, as demonstrated on a sample set of 24 NW devices. Regarding the pattern widths, a distinct notation of L is employed instead of x to distinguish between results obtained on planar substrates and on NWs. The stencil aperture is cleaned after each SL cycle via gold removal in a wet gold etchant.[4,53] One key point to mention here is the slight reduction of blurring in NW devices compared to the stencil patterning conducted onto the bare Si surface. Although the exact reason for the minimized blurring might be challenging to ascertain, we believe this slight blurring reduction compared to

bare Si surface is caused by the reduced area available to metal particles onto NW for the diffusion, as metal particles on bare Si surface can diffuse in all directions and hence can contribute to larger blurring. It is pertinent to mention that whole length of the NW can also be coated by adjusting either stencil spacer or the stencil aperture, however , L<10μm is implemented in this work to demonstrate the miniaturization capability and the selective nature of SL-based gold coating.

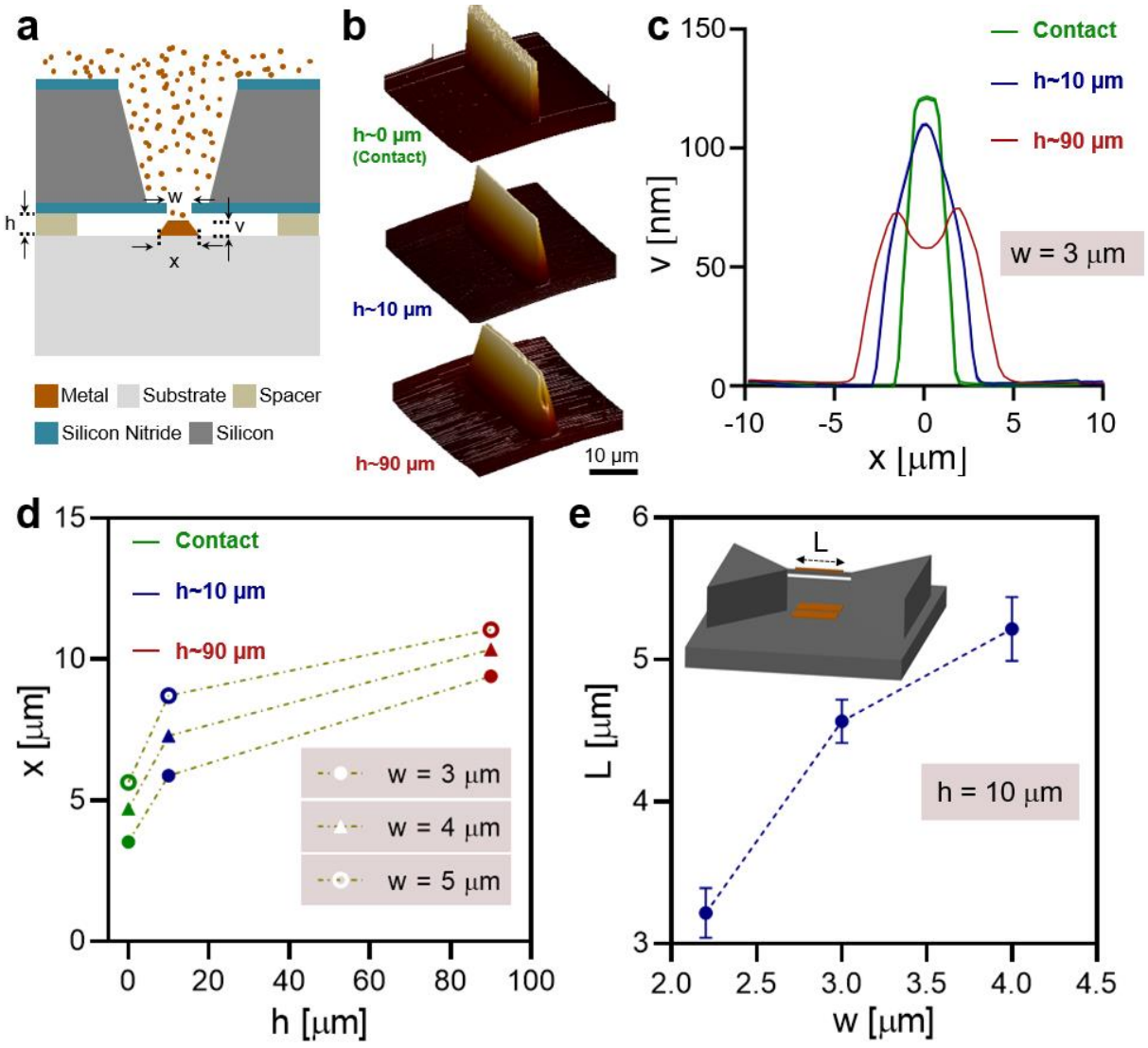

Figure 5. (a) Parameters considered in the characterization of blurring. Deposition through a stencil aperture of width w using a spacer thickness of h yields a pattern underneath the substrate with a width of x and a thickness of v. (b) AFM profiles after patterning with h=0 μm, 10 μm and

90 µm for the same stencil aperture and the same amount of material deposited. (c) AFM line scans of the patterns of b). (d) Pattern width, x, as a function of w and h. (e) The dependence of pattern length, L, on w with the resulting trend is verified using data from 24 devices during repeated use of the same stencil. Deviations do not exceed 10% of the mean values. A separate notation of x and L is used in order to differentiate the results obtained on planar substrate from the ones on NWs.

3.3. Surface Functionalization

Fluorescein isothiocyanate (FITC)-tagged thiolated heparin is used for surface functionalization of Si NWs. FITC-tag allows for monitoring the selective attachment of heparin to the gold-coated NW surface via fluorescence detection, while thiol modification enables coupling to gold. The gold-coated NW is then used to monitor sulfated glycosaminoglycans (sGAG)-growth factor interaction. In this work, heparin is used as sGAG material. sGAGs are crucial ECM constituents that control the bioavailability of cell instructive ligands in tissues and regulate various signaling mechanisms in health and disease.[63] The diversity of the sGAG structure and protein structure of ligands modulate their affinity towards each other. This way, tissues maintain the dynamicity of ligand presentation and signaling.[64] Elucidation of structure and interaction relationships between sGAGs and cellular ligands is vital for better understanding the subsequent biological events that they modulate. This calls for smart tools that can be used to investigate such interactions.

Before and after the surface functionalization, a confocal microscope (Leica DMI8 SP8 DLS/CS) is utilized to image FITC-labeled heparin coating atop NW, **Figure 6**. Figure 6a shows a brightfield image of the multiscale device architecture, with a closeup showing NW after the selective gold patterning prior to surface functionalization. The corresponding field on the same device is imaged after surface functionalization. Figure 6b shows the schematic for coupling thiolated heparin on gold-coated Si NW. To further demonstrate the potential of the selective

surface functionalized Si NWs, Si NWs are utilized as a platform for monitoring sGAG-growth factor interactions. A heparin-binding growth factor, human recombinant basic fibroblast growth factor (FGF)-2, is added as a ligand to assess and monitor its interaction with heparin. FGF-2 regulates cellular processes, including cell growth, differentiation, and migration.[65] Figure 6b shows the interaction sequence between the gold-coated Si NW and FGF-2 interaction with heparin-conjugated sections on the gold-coated NW, which was detected with an Alexa Fluor 647-tagged anti-human secondary antibody. FGF-2 (100 nM) was added onto the heparin-gold coated Si NW via drop-wise method and incubated for four hours under dark conditions. The sample was washed twice for 10 min to remove excessive, unbound FGF-2. For the detection of FGF-2, a sandwich approach was implemented. The Alexa Fluor 647-tagged (1:500) secondary antibody was incubated for 2 hours at room temperature to bind human FGF-2 and imaged via confocal microscopy.

Figure 6c shows a confocal microscopy image of the heparin (in green color) selectively attached to the gold-coated region at the center of the NW. A comparison of Figures 6a and 6c demonstrates the direct correspondence between the gold-coated region and green-colored heparin zone with consistent dimensions. The upper close-up view in Figure 6c shows the NW within this functionalized region. In the two bottom close-up views in the same figure, the growth factor detection is shown with the green color indicating the heparin, while the red signal represents the attachment of growth factor FGF-2. Following the establishment of gold-thiol bond, heparin polymers can function as a hub for the ligands. Therefore, FGF-2 can bind the polymer through the heparin-binding domain of the protein via electrostatic interactions. The successful attachment of the growth factor reveals that selective gold coating on Si NWs can be conjugated selectively with ECM molecules such as heparin to monitor their interactions with active ligands. Thus, this

platform holds the potential for diverse investigations pertaining to growth factors and also underscores the prospective utility in biochemical applications.

Growth factor delivery is a widely pursued approach in regenerative medicine.[66] Furthermore, the protein engineering field has demonstrated growth factors with super-affinity towards ECM, which enhanced tissue regeneration.[67] sGAGs, on the other side, undergo structural changes in pathological conditions such as cancer, i.e., aberrant sulfation, which alter their affinity towards ligands and contribute to disease progression.[63,64] Therefore, developing platforms that enable a better understanding of ligand-heparin interactions will serve an essential need in these fields.

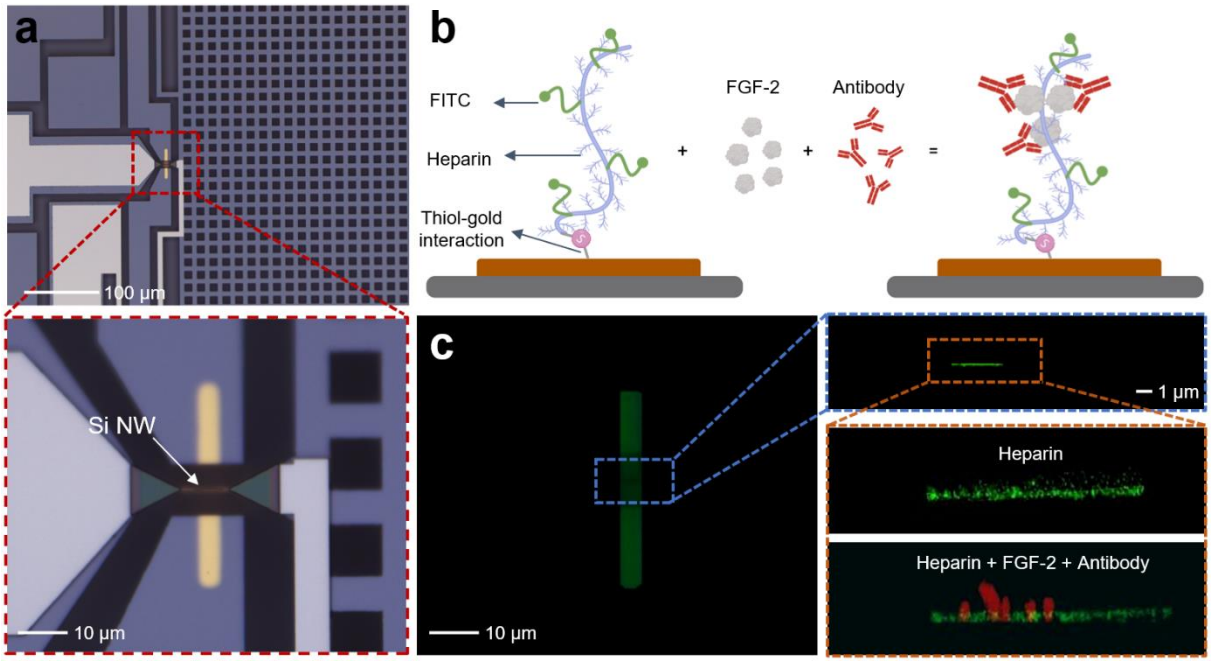

Figure 6. Surface functionalized Si NW as an sGAG-growth factor sensor. (a) Brightfield microscopy of the gold-coated region of the device. (b) Scheme of coupling FITC-tagged thiolated heparin onto the gold coating and course of action for growth factor binding and detection. (c) Confocal microscopy imaging of heparin on the gold-coated NW region and close-up images of the control and growth factor bound to Si NW.

At this point it is now also pertinent to detail the limitations of the current approach and explore avenues for improvement to achieve future targets described above. One key improvement involves enhancing the reusability of the stencil for NW patterning. For this purpose, stencil cleaning is necessary to retain the transparency of the membrane as well as unclogging the aperture. Secondly, the alignment process utilizing current micromanipulation setup requires a stencil size bigger than the NW die in order to clamp the stencil at both ends, leading to unutilized real estate (Figure S5-S6, S8). The alignment setup can thus be modified to redesign the stencil clamping method. Finally, increasing the throughput is the most critical parameters. For this purpose, through-etching of vias by deep reactive ion etching can result in nearly vertical etch profiles enabling one to increase the device density as the larger KOH etch features are eliminated.

4. Conclusion and Outlook

This study presents a multifaceted approach to the selective patterning and subsequent functionalization of Si NWs within a novel multiscale 3D device architecture. The process employs NW-based devices fabricated via a top-down technique, allowing monolithic integration of single crystal Si NWs with traditional MEMS components, significantly enhancing the versatility of Si NW-based devices. Moreover, selective patterning of Si NW is achieved through gold SL using a micromanipulation setup with seven DOFs. This precise alignment is critical for attaining both higher pattern resolution and pattern registration accuracy in subsequent processes, where a pattern registration accuracy of approximately 1.2±0.3 µm is achieved without any expensive commercial setup that offers similar accuracy.

A pattern resolution of 3.0 µm is achieved in current work as a pilot study, where high-resolution pattern metallization paves the way for various applications, particularly in nanoscale electronics

and biochemical sensors. Moreover, as the functionalized gold-coated region onto NW depends on stencil aperture, further miniaturization of the stencil aperture to the nanoscale dimensions through e-beam lithography can offer potential nanoscale surface functionalization of Si NWs in multiscale device architecture. We also emphasize the repeatability and reusability of our stencil apertures, a practical advantage for scaling up the fabrication process. Further expanding the functionality of Si NWs, we successfully surface-functionalize the selectively coated gold regions with fluorescently tagged and thiolated heparin. The fluorescence imaging demonstrates the selective attachment of heparin to the gold-coated NW surfaces. This surface functionalization also sets the stage for monitoring sGAG-growth factor interactions, a critical aspect of tissue engineering and regenerative medicine. We highlight the ability to monitor the binding of heparin-binding growth factors, such as FGF-2, to the heparin-coated Si NWs, showcasing the potential of this platform for studying ligand-ECM molecules interactions. The integrated approach offers a robust foundation for the fabrication, alignment, selective patterning, and surface functionalization of Si NWs within a multiscale 3D device architecture.

No membrane rupture is found during stencil fabrication, stencil aperture-NW alignment, or during the SL process, as evidenced by transferring the designed square metallization region onto the devices $D4 - D5$, Figure 4c. Moreover, for other devices, Si NWs are selectively metalized with 100% yield using the SL, as evident from the closeup images (Figure S9).

Overall, the surface functionalization process on Si NW is resistless, without thermal loads, and does not involve any mechanical pressure and hence bypasses any available NW-selective surface functionalization approaches in the literature for monolithically fabricated multiscale device architectures. Additionally, the method allows localized Si NW surface functionalization for

potential enhanced performance in biochemical applications due to its patterning selectivity to Si NW as compared to available non-selective literature.[8,37,47]

In particular, the ability to precisely tailor the surface properties of silicon nanowires enables the investigation of complex biological interactions and biochemical sensing. By coating the selectively functionalized surface with extracellular matrix (ECM) biomolecules, such as heparin in our study, we demonstrate the platform's utility for sensing growth factors with high specificity. Furthermore, functionalizing silicon nanowires with biomolecules opens up possibilities for developing next-generation biosensors, drug delivery systems, and tissue engineering scaffolds, where the precise manipulation of biological interactions is paramount. In addition to its utility in biochemical sensing, our technique holds promise for various fields, including nanoelectronics and nanomedicine. For nano-scale systems, this kind of selective functionalization is crucial since it enables the integration of silicon nanowires into complex circuits with enhanced performance, precision, and reliability. Briefly, future research endeavors could explore the potential of our selective functionalization technique in diverse applications, ranging from advanced nanoelectronics devices to innovative biomedical technologies.

In the future line of work, incorporating electrical readout would be necessary for label-free and quantitative detection of FGF-2. Furthermore, a comprehensive investigation into the dependence of NW electrical response on the thickness of surface decoration materials for NW is crucial before extending the application of these devices for surface functionalization. Moreover, since the proposed approach only decorates the top surface of the NW and partially covers the side surface, there is a need to explore conformal coating technologies such as atomic layer deposition through SL to selectively coat and functionalize the maximum achievable surface area of the NW for binding of FGF-2. This way, functionalization efficiency of the NW can be enhanced. Eventually,

for increased performance, incorporating SL process on next-generation sensor configuration such as stacked nanowires (NW) within a 3D substrate is crucial.

Finally, originating from the similar technological process and performance requirements, next-generation NW-based biochemical sensors with similarities to GAA transistors, functionalized in a selective manner, can facilitate wafer-scale integration of selectively surface-decorated biochemical sensors. This work, through introduction of a SL-based surface decoration approach, thus advances the capabilities of Si NW-based nanodevices and presents a potential versatile platform for investigating complex biological interactions, with implications for various fields, including nanoelectronics and biochemical sensing.

5. Experimental Section/Methods

Materials. Photoresist AZ 5214E (Microchemical), nLof 2070(Microchemical), KOH pellets, acetone (Technic), isopropyl alcohol (Technic), hydrofluoric acid (Technic, 50%), photoresist AZ MIF 726 developer (Microchemical), chromium pellets (Kurt J. Lesker, 99.95%), and gold pellets (Kurt J. Lesker, 99.99%) were utilized as a part of the fabrication process flow for technology development. The deionized (DI) water was used during these experiments to wash samples. For the biological surface functionalization, Fluorescein Heparin Thiol, M.W. 27 kDa (HAWORKS, FITC-HP-Thiol), Triton-X-100 (0.1%)(Merck, 112298), BSA (100 µM), Sodium citrate Buffer (10%), NaOH (1M) (Sigma, S5881), FGF-2 (100 nM), goat-derived anti-human antibody (ThermoFisher, A-55749)(1:500) were utilized. Acetone and dH20 were used to wash the NW sample consecutively.

Si NW definition. A 4" diameter, < 100 > wafer with a 10-µm-thick device layer, a 1-µm-thick BOX, and a 380-µm-thick handle layer is used. The wafer is first doped with phosphorus to a mean resistivity of 5×10−4 Ωcm. For e-beam lithography, Si NW is patterned with a 600-nm-thick e-beam resist HSQ 21% (Hydrogen silsesquioxane) in < 100 > crystal orientation via the Raith e-beam lithography system. A 400-nm-thick PMMA 495k A8 and 160-nm-thick PMMA 950k A4 e-beam resists are used for lift-off. After the metallization, the sample is put into acetone overnight for the lift-off process. Followed by DRIE, resist removal is conducted in an oxygen plasma system with a power of 600 W, followed by 5 mins of vapor etching in hydrofluoric acid (HF) at 40°C.

PECVD Si_xN_y coating for Stencil. For Si_xN_y deposition, PECVD with a temperature of 80 ℃, ICP power, and RF power of 500 W and 50 W, respectively, is utilized. The deposition process was conducted at a pressure of 12 Pa, with gas flows for NH_3, Ar, and SiH_4 as 9, 140, and 145 sccm, respectively. Before the deposition, a 10-minute cleaning of the equipment was conducted via a plasma mixture consisting of CF_4, O_2, and Ar. The Si_xN_y was coated on the top surface of the Si substrate. For the bottom surface, the substrate was removed from the equipment after top surface Si_xN_y deposition, inverted, and subjected to the same deposition condition as the top surface.

Etch masks for Stencil. Photoresist AZ 5214E is spin-coated at 5000 rpm for the first nitride etch, followed by a 55s soft bake at 110°C. Following the RIE of Si_xN_y, a resist strip is performed using acetone and oxygen plasma cleaning at an ICP power of 200 W and RF power of 100 W. To prepare the KOH solution, KOH pellets weighing 40 grams are mixed with 150 mL DI water and slight IPA is added to minimize Si etch roughness. After the completion, a thick photoresist (AZ

nLof 2070, SU-8, etc.) is coated on the wafer's backside, and a spacer is patterned onto the fragment using Heidelberg MLA100. Hardbake for adhesion is conducted at 150 °C for 6 minutes. At the backside, AZ 5214E with 6000 rpm is coated. After the Si_xN_y etch, flood exposure to the sample via UV intelliRay 600 for 2s is conducted, and the sample is washed with AZ 726 developer to remove the AZ 5214E selectively. Slight O2 RIE is performed to remove the remains of AZ 5214E and clean the stencil from any residues.

E-beam evaporation. Chromium is deposited with a 0.05 Å/s deposition rate, while gold is deposited at a 0.25 Å/s deposition rate. All depositions are performed at the same chamber pressure. The stencil is clamped to the substrate, followed by the evaporation of 110 nm gold (same for all h values) after a 5-nm-thick chromium at a chamber pressure of 5×10^{-6} torr without substrate heating. All thickness values are monitored during the deposition via a quartz crystal microbalance (QCM) inside the e-beam evaporation equipment. For the blurring analysis, following the SL with different h, the material profile onto the substrate is analyzed via atomic force (AFM) and confocal microscopy. For the confocal microscope measurement, 100 nm Si RIE is performed, with metal serving as an etch mask, to increase the contrast between the substrate and the deposited metal for imaging purposes. As an outcome, the pattern width, x, onto the substrate as a function of spacer thickness, h, is determined to establish the extent of geometrical blurring.

Stencil-NW die alignment protocol. As part of the stencil-NW chip protocol, first of all, relative XYZ coordinates of the stencil aperture and device $D4$ are determined, followed by which the NW chip position is adjusted in in-plane with respect to stencil alignment positions via NW manipulation stages. Meanwhile, the z-coordinate of the NW chip is preserved, and the objective

is focused individually onto the stencil and NW chip during the process. For chip-level alignment, following confirmation of course alignment for one diagonal, e.g., $D4$, the whole stencil-NW chip assembly is moved to inspect the alignment marks along the other diagonal, e.g., $D5$, while the microscope objective stays at its position. This movement does not disturb the relative NW-stencil aperture position. Usually, the course alignment takes 2-3 cycles, e.g., going back and forth between $D4$ and $D5$ alignment positions to completely align the aperture on the stencil with the pad onto the NW device in both in-plane translation and rotation axis. Followed by course alignment, the NW chip is moved upward through the z-controller and placed at a gap of ~100µm to the stencil along the z-axis. At this point, a fine alignment is conducted. For the fine alignment, we rely on the transparency of the nitride membrane housing stencil aperture. Here, since the 100 nm-thick stencil aperture membrane is transparent, this allows the opportunity to see-through the stencil membrane and watch the alignment feature onto $D4$ through just a change of microscope objective focus position along the z-axis. The NW chip is slowly moved upward through its z-actuator while the objective focus is adjusted in parallel via the z-actuator to see both the $D4$ feature and the stencil aperture position and monitor any error due to non-zero in-plane translational movement of the NW z-actuator. Finally, contact is made between the stencil and the NW chip, which is determined by the z-actuator position. Moreover, the NW chip is slightly moved upwards via a z-actuator through a distance of 25 µm to ensure firm contact and remove any unwanted excessive gap resulting from anything but the spacer. The compliant clamps on the stencil holder support the stencil in case of excessive push force by the substrate and prevent any damage to the stencil membrane/NW chip features. The stencil-NW contact and the resultant slight upward movement of the stencil is monitored from the objective where upward movement of the stencil causes loss of optical focus onto stencil features. After stencil-NW chip contact, they get

joined via drop (<10µL) of photoresist AZ5214E as an adhesive. Following this, the z position of the NW actuator is fully lowered while the NW chip stays stuck and in contact with the stencil.

Surface functionalization protocol. Before the experimental procedures, the gold-coated NW was rinsed with a solution containing 0.1% Triton-X-100 and 100 µM Bovine serum albumin (BSA) for 2 hours to prevent non-specific biomolecule interactions. This step is also required for the stability of further interactions. The wire was air-dried for an hour at room temperature. FITC-tagged thiolated heparin in lyophilized form was first resuspended in a 10% sodium citrate buffer solution. The solution was gently mixed while adding the solvent to prevent clump formation. The resuspended solution was stored at +4 °C until further use. The pH of the solution was adjusted to pH 8.0 with NaOH to increase the interaction strength. Following this, FITC-tagged thiolated heparin in a solution form is attached to the surface through thiol-gold interactions. The solution was added to the coated surface via the drop-wise method under a brightfield microscope. Surface-heparin coupling was established after 6 hours of incubation at 37℃. Next, excessive heparin is washed away with acetone and distilled water consecutively. The remaining water is air-dried.

Supporting Information

Optimization of the stencil fabrication utilizing PECVD membrane (Figure S1), Raw SEM image of stencil top and cross-section (Figure S2), Chip-level SL onto NW with damaged membranes along diagonals (Figure S3), Chip-level SL onto NW with ~ 300×300 μm^2 membrane size along diagonals without any damage (Figure S4), Stencil with a spacer thickness of ~10 µm (Figure S5), Alignment setup for micromanipulation of stencil with respect to NW die (Figure S6), Validation of stencil-NW die alignment after attaching stencil to die (Figure S7), Mounting setup for stencil-

NW die assembly for evaporation (Figure S8) Confocal image of the NW die before and after selective gold coating (Figure S9) AFM image of the stencil patterning on a planar substrate with different spacer thicknesses to signify blurring effect (Figure S10).

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The manuscript was written through contributions of all authors. All authors have given approval to the final version of the manuscript.

Funding Sources

B. Erdem Alaca and Basit Ali gratefully acknowledge the financial support by Tubitak under grant no. 118C155 and 123E455.

ACKNOWLEDGMENT

The authors would like to thank Dr. Barış Yağcı from KUYTAM-Koç University Surface Technologies Research Center for assistance with detailed SEM and EDX measurements. The authors acknowledge the use of facilities of the n^{2}STAR-Koç University Nanofabrication and Nanocharacterization Center for Scientific and Technological Advanced Research, and

KUYTAM-Koç University Surface Technologies Research Center. The schemes in Figure 1d, Figure 3a, Figure 6b, and ToC figure are partly created with BioRender.com

ABBREVIATIONS

SL, stencil lithography; PVD, physical vapor deposition; Si NW, silicon nanowire; ECM, extracellular matrix; sGAG, sulfated glycosaminoglycans; CD, critical dimension; PECVD, plasma enhanced chemical vapor deposition; SOI, silicon-on-insulator; LPCVD, low pressure chemical vapor deposition; FITC, Fluorescein isothiocyanate; FGF, fibroblast growth factor.

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