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Enhanced UPQC Control Scheme for Power Quality Improvement in Wave Energy Driven PMSG System

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Abstract—This article focuses on enhancing power quality (PQ) in a wave energy-driven permanent magnet synchronous generator (PMSG) system with unbalanced and highly inductive nonlinear loads using a unified power quality conditioner (UPQC). Our proposed control system improves voltage quality, compensates for reactive power, and mitigates harmonics. It ensures constant voltage amplitudes during supply voltage faults, achieving harmonic rejection, reactive power compensation, and enhanced voltage quality through the UPQC's parallel converter. Compared to previous methods, we introduce a frequency-fixed second-order generalized integrator (FFSOGI) quasi-type-1 PLL for efficient load harmonics extraction and source voltage fault detection. Additionally, a robust nonlinear proportional-integral (N-PI) controller, with a feedforward term, regulates the DC-link voltage swiftly and mitigates fluctuations. Our approach ensures compliance with IEEE standards for source current and load voltage harmonics. Comprehensive PSCAD/EMTDC results, utilizing experimental torque and power data from a wave energy converter at the Australian Maritime College model test pool, highlight the advantages of our proposed approach over conventional methods.

Index Terms—Wave energy converter, UPQC, nonlinear loads

NOMENCLATURE

ANF	Adaptive notch filter
CF	Comb filter
DLG	Double line-to-ground
EPLL	Enhanced PLL
FFSOGI	Frequency-fixed SOGI
FLPID	Fuzzy logic proportional-integral-derivative
GDSC	Generalized delayed signal cancellation
LMS4	Least mean fourth
LPF	Low-pass filter
MAF	Moving average filter
NLLs	Nonlinear loads
N-PI	Nonlinear proportional-integral
PMSG	Permanent magnet synchronous generator
PCC	Point of common coupling
PQ	Power quality
QSG	Quadrature signal generator
QT1	Quasi-type-1
SLG	Single line-to-ground
SOGI	Second-order generalized integrator
SRF	Synchronous reference frame
THD	Total harmonic distortion

UPQC	Unified power quality conditioner
VSCs	Voltage source converters
WECs	Wave energy converters
Γ_g	Reactive current control gain
h	Harmonic order
x	a, b, c phases
s^+	Positive sequence
s^-	Negative sequence
λ_s	Tuning gain of FFSOGI
λ_l	Loop filter gain
τ_s	Time constant
P^*	Reference Active Power
T_w	Window length
ε, μ	Tuning gains of nonlinear function
$\lambda_{kp}, \lambda_{ki}$	Positive tuning gains of N-PI
τ_q	SOGI time constant
τ_m	LPF time constant

I. INTRODUCTION

Recent advancements in renewable energy systems provide opportunities to decarbonize power generation in remote coastal communities. Wave energy, with its low environmental impact, holds promise for sustainable energy in these areas. Numerous successful wave energy converters (WECs) are now operational globally [1]. Existing literature has explored WECs ranging from kilowatt [2]–[4] to megawatt-scale [5], highlighting their adaptability to various power-level requirements.

A standalone power generation system, featuring a three-phase PMSG driven by wave energy, is an ideal solution for small-scale island communities. Its inherent advantages, such as self-excitation and easy voltage build-up, make it the preferred choice. Effective control is crucial to ensure unity power factor operation (UPF) operation under diverse loading conditions, including nonlinear, unbalanced, and highly-inductive loads, ensuring overall system performance. However, as the PMSG ages, its voltage generation capacity may decline, and faults can lead to fluctuations in output. This will require mitigation of the supply voltage fluctuation propagation to the voltage sensitive load. To address these issues, integration of a UPQC [6] ensures consistent voltage, improved power factor, reduced harmonic distortion, and decreased reactive power. UPQC allows concurrent and/or independent mitigation of voltage and current related PQ issues. This enhances the efficiency and reliability of the system. Utilizing series and parallel voltage source converters (VSCs) with common DC-coupling, the UPQC effectively mitigates various power-quality concerns, a novel approach in this study. To the

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authors' knowledge, prior research has not explored UPQC integration with WECs. Note that while both unified power flow controller (UPFC) and UPQC are flexible AC transmission system devices utilized for power system control, the UPFC focuses on transmission system optimization, power flow, and power factor correction, whereas the UPQC is primarily employed to mitigate PQ issues in distribution power systems, which is the considered case in this work.

Given the importance of an effective control strategy for UPQC to enhance power quality, recent proposals include various control methods. In [7], authors utilized an ANF for series converters and a logarithmic absolute filter for parallel converters. However, the ANF lacks gain normalization, potentially slowing convergence during significant voltage sag/swell depths, and the study did not present systematic gain tuning results for the chosen filters. In [8], a quarter-delay-based QSG approach was explored, but it's sensitive to grid-frequency variations common in isolated power systems. Another method in [9] employed multiple complex coefficient filters and SOGI, increasing computational complexity. Additionally, a FLPI controller was proposed for DC-link voltage regulation in the same study, which can be challenging to tune and may increase sensitivity to noise when derivative terms are incorporated.

In [10], SOGI with a frequency-adaptive CF is employed for UPQC control, introducing substantial computational complexity. Conversely, in [11], a GDSC filter is used to avoid fractional delay implementation, but this choice restricts the control system's switching frequency and complicates filter design. Meanwhile, in [12], an LMS4 filter is utilized, but the absence of amplitude normalization may impact response rates during sudden high-amplitude sag/swell in the source voltage. [13] employs sliding-mode control with a disturbance observer for robustness; however, the conventional proportional-integral (PI) controller for the DC-link restricts overall control performance, leading to high THD. An adaptive vectorial filter is used for UPQC control in [14], but lacks a presented tuning method. The employed FLL lacks design flexibility due to the absence of tuning gain. In contrast, the variable leaky least-mean-square (LMS) algorithm in [15] enhances conventional LMS filter performance with an adaptive leakage factor and step size. However, this approach increases computational complexity, limiting its suitability for real-time implementation in low-cost embedded systems.

In this article, we use the frequency-fixed SOGI (FFSOGI) as our filtering method and adopt a quasi-type-1 PLL (QT1-PLL) for grid synchronization. The PLL, equipped with an in-loop moving average filter, effectively mitigates odd-order harmonics mentioned in IEEE Std. 519 [16]. It's worth noting that this PLL has a single tuning gain, simplifying the tuning process and reducing complexities. Since FFSOGI operates independently of the PLL, separate tuning is possible. We've developed single-phase and three-phase versions for UPQC control in series and parallel converters. Additionally, we've integrated a nonlinear PI controller to ensure swift responsiveness in the DC-link voltage control loop, eliminating voltage fluctuations. We've also introduced a feed forward term to enhance dynamic response, improving performance even during substantial voltage sag/swell events. We offer

a detailed small-signal model, PLL tuning details, and an explanation of the nonlinear PI controller method.

The main methodological contribution of this work is the development of FFSOGI-QT1-PLL for the UPQC system. A single-phase version of this PLL is proposed for per-phase fault detection and series converter control to maintain a constant load voltage, while a three-phase version is proposed to enhance harmonics robustness, reduce reactive power due to load imbalance, and extract load voltage and current positive sequences. The application of wave energy-driven PMSG (with experimentally collected torque and power data from a WEC) as a power source for powering sensitive local loads with high PQ in remote coastal locations is the primary applied contribution of this work. Additionally, effective and rapid DC-link voltage regulation through an N-PI controller, and consequently improving the efficiency of the overall system, is the secondary applied contribution of this work.

The article is structured as follows: The considered system topology and proposed UPQC control system are given in Sec. II. PSCAD/EMTDC results are given in Sec. III and the article is concluded in Sec. IV.

II. UPQC IN WAVE ENERGY DRIVEN PMSG SYSTEM

A. Systems Description and Control System Development

The WEC-driven system's architecture is shown in Fig. 1, with the UPQC installed between the wave energy-driven PMSG and NLLs. A substation with a transformer (TR) connects the WECs together and transmits the total power to the shore. We use an oscillating water column-type WEC with a single-stage unidirectional air turbine system as the energy source. This turbine generates power during the air intake phase, using any torque produced during pressure drops as mechanical input to the generator. Preliminary experiments and existing literature confirm its higher efficiency compared to the bi-directional counterpart. Importantly, variable-speed operation is not strictly required for this WEC. To further study the system, we rely on experimentally collected torque and power data obtained during tests in the model test pool at the Australian Maritime College (AMC) [5]. In the obtained data, the period of fluctuation of the wave is nearly 0.8 sec. Based on the experimental results, an empirical relationship is established between the mechanical torque (T_m) and pressure drop (ΔP) with $\rho_1, \rho_2 > 0$ as follows:

$$T_m = \rho_1 (\Delta P)^2 - \rho_2 \Delta P. \quad (1)$$

The theoretical basis for the above empirical relationship can be found in [17]. The proposed control algorithm for the UPQC system, which consists of four parts, is shown in Fig. 2. Parts a-b and c-d involve the control of series and parallel converters of the UPQC system, respectively. The series converter and its control are utilized to eliminate voltage PQ issues, ensuring the maintenance of sinusoidal, balanced, and constant amplitude voltages at the load terminals, regardless of changes in the system. The control of the series converter reduces losses during reactive power draw from the source and enables it to operate at unity power factor. Additionally, the parallel converter, along with its control method, provides

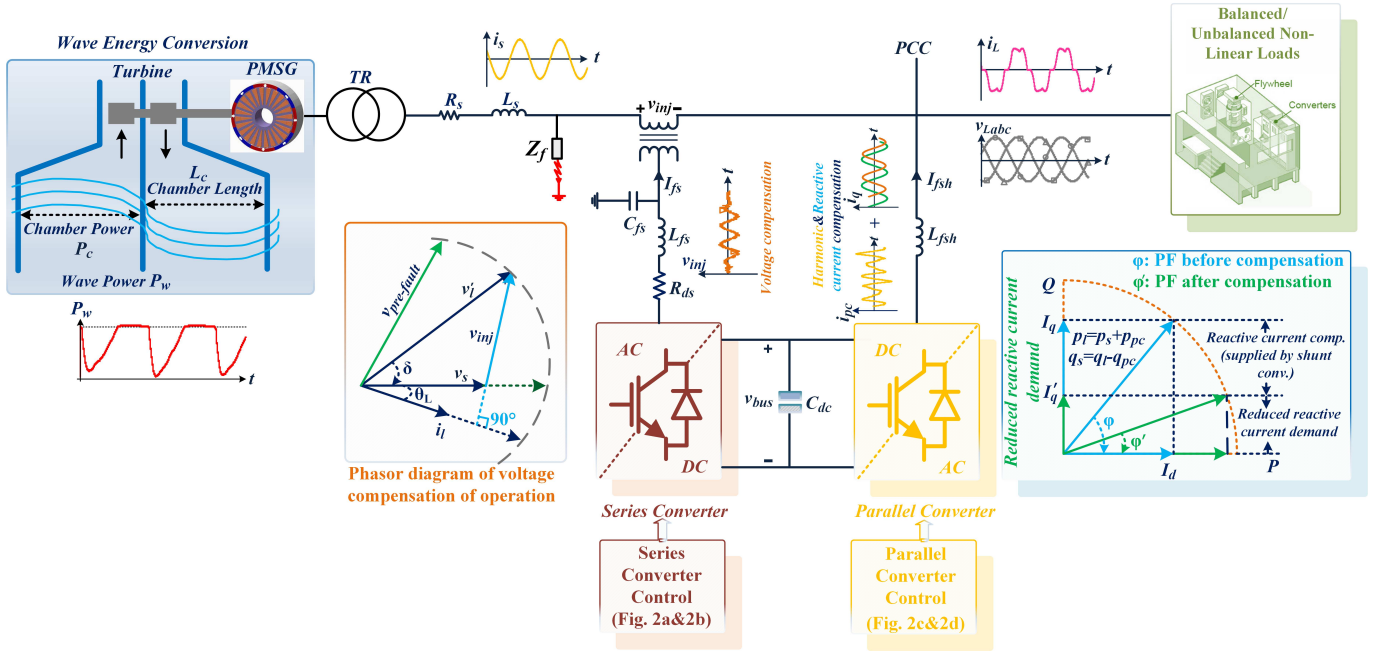


Figure 1. Configuration of the proposed OWC wave energy converter driven PMSG system with UPQC integration.

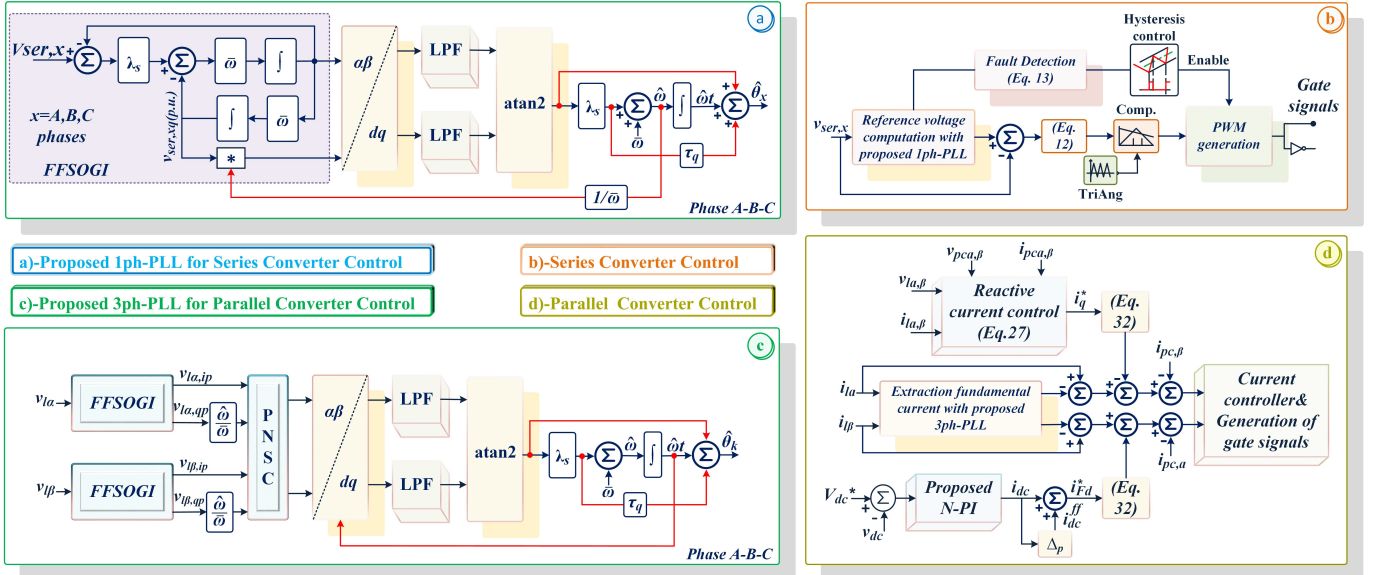


Figure 2. The proposed control scheme including a) proposed 1-phase PLL, b) proposed control for the series converter control, c) proposed 3-phase PLL, and d) proposed control for the parallel converter control.

improvements in current quality such as reactive power compensation, harmonic elimination, and power factor. For system losses in UPQC-based systems, [18] can be consulted.

B. Proposed PLL

1) Single-Phase PLL

Individual phase ($x = a, b, c$) ideal grid voltage including the positive (s^+) and the negative (s^-) sequences is given by:

$$v_{ser,x}(t) = \sum_{k=s^+}^{s^-} V_k \cos(\omega t + \phi_k), \quad (2)$$

where the phase amplitude, actual grid frequency, and initial phase angle are denoted by V , ω and ϕ , respectively and the subscript k depicting the sequence. Note that the individual sequence phase angle can be denoted by $\theta_k = \omega t + \phi_k$ and the actually frequency is modeled as $\omega = \bar{\omega} + \tilde{\omega}$, where the nominal and deviation frequency are denoted by $\bar{\omega} = 100\pi$ rad./sec. and $\tilde{\omega}$. For the series converter control, estimation of V_k and θ_k are necessary from the measured signal (2), which is often polluted by harmonics and noise. This can be effectively handled by PLL and adopted here for the same. Overview of the developed PLL is given in Fig. 2 (a). As individual phase estimation is considered here,

a QSG is essential for the subsequent development. We are considering the FFSOGI [19] filter here for its excellent harmonic filtering property and frequency-fixed structure, as it allows independent tuning of the QSG and the PLL loop filter without any direct feedback path involved. Denote the in-phase estimated quantity by $v_{ser,x,ip}$ while the quadrature-phase component by $v_{ser,x,qp}$. Transfer function of the FFSOGI are given by for the tuning gain $\lambda_s > 0$ [19]:

$$\mathcal{G}_{ip} = \frac{v_{ser,x,ip}}{v_{ser,x}} = \frac{\lambda_s \bar{\omega} s}{s^2 + \lambda_s \bar{\omega} s + \bar{\omega}^2}. \quad (3)$$

$$\mathcal{G}_{qp} = \frac{v_{ser,x,qp}}{v_{ser,x}} = \frac{\lambda_s \bar{\omega}^2}{s^2 + \lambda_s \bar{\omega} s + \bar{\omega}^2}. \quad (4)$$

Whereas in time-domain, the dynamics of the FFSOGI can be approximated by the following first-order transfer function:

$$\mathcal{G}_{qsg}(s) = 1/(\tau_q s + 1), \quad (5)$$

where the SOGI time constant is τ_q is given in eq. (6). FFSOGI works with nominal grid frequency. When the input signal's actual frequency deviates from the nominal frequency, it will introduce error in the amplitude and phase of the estimated signals by (3) and (4). For the in-phase transfer function, these errors are reported to be [20]:

$$\begin{aligned} \angle \mathcal{G}_{ip}(j\omega) &\approx -\frac{\omega^2 - \bar{\omega}^2}{\lambda_s \omega \bar{\omega}} \approx -\frac{2}{\lambda_s \bar{\omega}} \tilde{\omega} \approx \tau_q \tilde{\omega}, \\ |\mathcal{G}_{ip}(j\omega)| &\approx (\lambda_s \omega \bar{\omega}) / \sqrt{(\bar{\omega}^2 - \omega^2)^2 + (\lambda_s \omega \bar{\omega})^2}. \end{aligned} \quad (6)$$

These errors need to be corrected for accurate estimation. PLL phase detector (PD), which is the conventional demodulation-type park transformation, uses the estimated signals as the input. It was found in [20] that amplitude error in the estimated signal causes double frequency oscillation in the PD output. As such, a scaling factor $(\omega/\bar{\omega})$ is applied on the estimated quadrature signal before the PD to eliminate this. In the proposed case, a quasi type-1 PLL structure [21] is considered. By utilizing low-pass filter (LPF) (with a time constant $\tau_m > 0$), this PLL can significantly attenuate the negative sequence component induced double the fundamental frequency oscillation in the PD output, which is different from the amplitude error induced oscillation.

2) PLL Gain Tuning and Comparison

The small-signal model of the proposed PLL is depicted in Fig. 3(a). As previously explained, there is no direct feedback path between the FFSOGI and the PLL. Consequently, the FFSOGI functions as a pre-loop filter in the synchronous reference frame (SRF). Moreover, a phase error compensation term has been incorporated into the small-signal model to offset the phase error induced by the fixed-frequency operation of the pre-loop filter.

The proposed PLL has three parameters to tune, namely FFSOGI gain λ_s , LPF time constant τ_m , and the loop filter gain λ_l . In the SOGI literature [19], [20], it has been found that setting λ_s as $\sqrt{2}$ strikes a good balance between the disturbance rejection and the dynamic performance for the FFSOGI filter. The same is adopted here. To tune the LPF

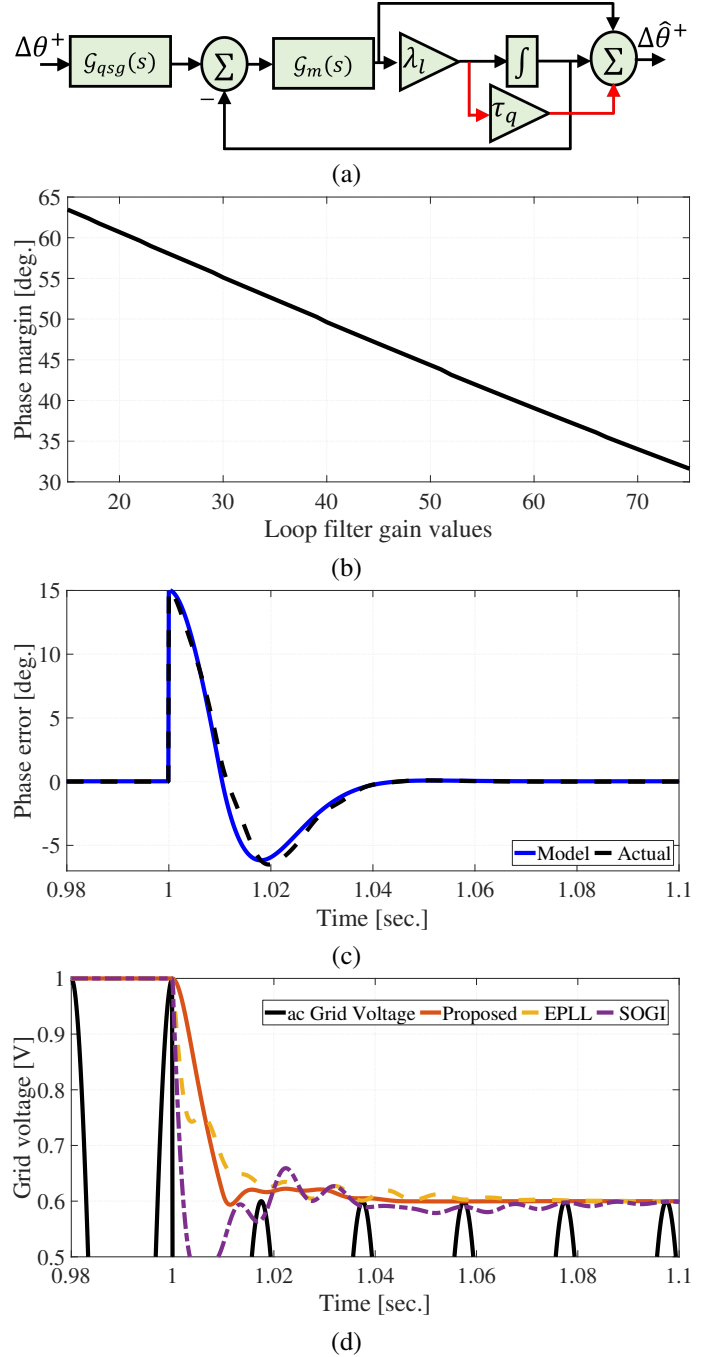


Figure 3. Proposed PLLs (a) Small-signal model, (b) loop-filter gain tuning, (c) small-signal model validation, (d) performance comparison.

time-constant, analogy with the moving average filter (MAF) will be used. In the synchronous reference frame, half-cycle window length MAF can eliminate all odd-order harmonics and the double frequency oscillation caused by the negative sequence component in the measured voltage. In [22], it has been found that the first-order Padé approximation of the MAF, is equivalent to a first-order LPF and the time constant of that LPF is given by $T_w/2$ with T_w being the window length. Half-cycle equals to $T_w = 10$ msec. in the nominal case, which corresponds to a time constant of 5 msec. As such, this value has been selected for τ_m . Finally, to tune λ_l , open-

loop phase margin can be considered. Using the small-signal model in Fig. 3 (a), the open-loop phase margin has been calculated for different value of the loop filter and plotted in Fig. 3(b). A phase-margin between $30^\circ \sim 60^\circ$ is often recommended for PLL gain tuning [23]. The mid-point (i.e. 45°) of this range has been selected for a suitable trade-off between the fast dynamic response and disturbance rejection, which corresponds to $\lambda_l \approx 50$. With respect to the selected values, validation of the small-signal model is presented in Fig. 3(c) for a sudden phase angle change of $+15^\circ$. Results show that the model can accurately track the phase. While tuning the PLL parameters, we've assumed an ideal scenario. However, if the measured signal is excessively noisy or distorted with specific frequency components, addressing these issues is crucial. The PLL's LPF has a 200 Hz cut-off frequency, which can be further reduced in very noisy measurements to slow down the PLL and mitigate noise effects. Additionally, an extra pre-loop noise mitigation filter, like an exponential MAF [24], can simultaneously enhance the proposed PLL's harmonic disturbance rejection.

To assess the suitability of the proposed PLL compared to existing literature, a comparative study has been conducted with similar state-of-the-art methods: SOGI-PLL and EPLL [25]. The series converter is expected to respond rapidly to any changes in the source voltage. Therefore, for the purpose of this comparative study, a voltage sag of -0.4 p.u. has been considered, and the results are presented in Fig. 3(d). The results indicate that the proposed PLL detected the amplitude change faster than the comparison techniques. This finding suggests that it is a suitable method for per-phase fault detection in the series converter control of UPQC systems.

C. Three-Phase PLL

This PLL will be used in monitoring the load voltage and currents, which will subsequently be used for controlling the parallel converter of the UPQC. In the stationary reference frame ($\alpha\beta$), load voltages and currents can be modeled as:

$$\chi l_{\alpha} (t) = X_{\alpha s+} \cos(\omega t + \phi_{s+}) + X_{\alpha s-} \cos(\omega t + \phi_{s-}), \quad (7)$$

$$\chi l_{\beta} (t) = X_{\beta s+} \sin(\omega t + \phi_{s+}) - X_{\alpha s-} \sin(\omega t + \phi_{s-}), \quad (8)$$

where $\chi \in \{v, i\}$ indicates the instantaneous voltage/current and $X \in \{V, I\}$ indicates the voltage/current magnitude. The remaining variables retain the same meanings as defined in the single-phase PLL section. This PLL is responsible for extracting the positive and negative sequence components along with their corresponding phase angles from eqs. (7) and (8). This can be achieved by applying the symmetrical components theory, as championed by Lyon in his seminal work [26]. According to this method, the sequences can be extracted from the original signals and their corresponding quadrature versions, denoted by $\chi l_{\alpha}^{\perp}(t)$ and $\chi l_{\beta}^{\perp}(t)$ that can be obtained using FFSOGI as:

$$\begin{bmatrix} \chi l_{\alpha s+} \\ \chi l_{\beta s+} \\ \chi l_{\alpha s-} \\ \chi l_{\beta s-} \end{bmatrix} = \begin{bmatrix} \frac{1}{2} & 0 & 0 & \frac{1}{2} \\ 0 & \frac{1}{2} & \frac{1}{2} & 0 \\ \frac{1}{2} & 0 & 0 & \frac{-1}{2} \\ 0 & \frac{1}{2} & \frac{-1}{2} & 0 \end{bmatrix} \begin{bmatrix} \chi l_{\alpha}(t) \\ \chi l_{\alpha}^{\perp}(t) \\ \chi l_{\beta}(t) \\ \chi l_{\beta}^{\perp}(t) \end{bmatrix}. \quad (9)$$

Overview of the three-phase FFSOGI QT1-PLL is given in Fig. 2 (c). As the tuning of this PLL is the same as that of the single-phase counterpart, it is avoided for the sake of brevity.

D. Series Converter Control

Series converter control scheme is shown in Fig. 2 (b). This scheme is composed of reference voltage computation and voltage fault detection. The proposed single-phase PLL has been employed for both purpose. A unit vector template is required to determine whether there is a voltage sag or swell in any phase [27] as follows:

$$V_{s+}^{ref} = \sqrt{(V_{ser,as+})^2 + (V_{ser,bs+})^2 + (V_{ser,cs+})^2}, \quad (10)$$

$$u_{ser,xs+} = v_{ser,xs+} / V_{s+}^{ref}, \quad (11)$$

where $x \in \{a, b, c\}$. The unit vector template is computed by sensing the source voltages [15]. The required injection voltage $v_{ser,x}^{inj}$, which can be obtained as follows:

$$v_{ser,x}^{inj}(t) = \left(V_{s+}^{ref} - V_{ser,xs+} \right) \sin(\omega t + \phi_{xs+}), \quad (12)$$

where the reference voltage amplitude is given by V_{s+}^{ref} . The amplitude of the required voltage sag or swell depth ($S_{depth,x}$) can be calculated depending on the grid code requirements (the limit value of $\pm 10\%$) as follows:

$$\begin{aligned} S_{depth,x} &= |V_{s+} - V_{ser,xs+}| \geq 90\%V_{s+} \text{ or} \\ &|V_{s+} - V_{ser,xs+}| \leq 110\%V_{s+} \end{aligned} \quad (13)$$

With the PLL-estimated amplitude, the method detects voltage compliance. If it falls outside the limit, the PWM block activates, and the series converter adjusts it to meet the grid code requirements. The error between the estimated voltage and the sensed source voltage signals for any phase is processed as its input to the PWM controller (see Fig. 2 (b)). According to the sag or swell depth, the extracted component ($V_{ser,xs+}$) is operated in the hysteresis comparator to generate the switching pulses of the series converter.

E. Parallel Converter Control

Parallel converter control scheme is shown in Fig. 2 (d). This converter is responsible for source and load harmonics and unbalance mitigation and also performs the DC-link voltage control. Technical details are given below:

1) DC-Link Voltage Control

Any fault in the grid and/or load will cause a change in the DC-link voltage. As such, fast, accurate, and ripple-free DC-link voltage regulation is essential to ensure high-performance operation of the UPQC, consequently smooth operation of the WEC despite any fault. Conventionally, PI controller is a popular choice for this purpose [7], [8], [10]–[14]. Denote the DC-link voltage error as: $e_{dc}(t) = v_{dc}(t) - V_{dc}^*$ with the instantaneous and the reference voltage being denoted by $v_{dc}(t)$ and V_{dc}^* . In terms of e_{dc} , the PI controller can be written as:

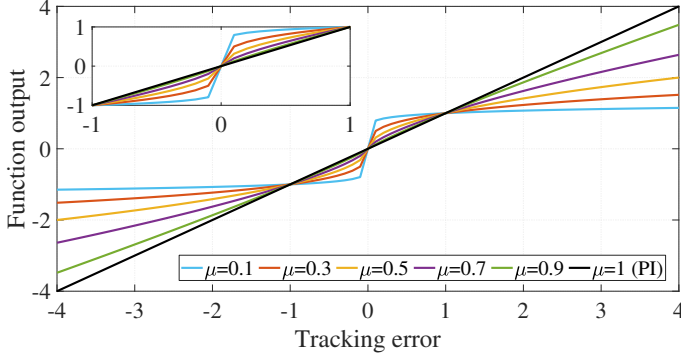


Figure 4. Output of function (16) for varying μ and $\epsilon = 10^{-1}$.

$$u_{dc}(t) = \lambda_{kp}e_{dc}(t) + \lambda_{ki} \int e_{dc}(\tau) d\tau, \quad (14)$$

where the positive tuning gains are denoted by λ_{kp} and λ_{ki} . Controller (14) is popular in practice as it is easy to tune and the relationship between the gains λ_{kp} , λ_{ki} and the dynamics and steady-state performances are well known [4].

The controller in eq. (14) operates as a linear function of the tracking error, leading to slow DC-link voltage adjustment when the grid undergoes sudden changes. Increasing the proportional gain can address this, but it results in higher overshoot and steady-state ripple amplification. To resolve this issue while maintaining the conventional controller structure, a nonlinear PI controller [28] is developed. This controller adjusts gains based on the tracking error: it applies substantial control action for large errors to quickly reach the reference voltage and smaller action for smaller errors, preventing ripple amplification. This nonlinear controller, considered in this work, is defined as follows:

$$u_{npi}(t) = \lambda_{kp}\mathcal{F}(e_{dc}, \mu, \epsilon) + \lambda_{ki}\mathcal{F}\left(\int e_{dc}, \mu, \epsilon\right), \quad (15)$$

where the general form of the nonlinear function is given by for tuning gains $\epsilon, \mu > 0$:

$$\mathcal{F}(\cdot, \mu, \epsilon) = \begin{cases} \text{sign}(\cdot) \cdot |\cdot|^\mu, & |\cdot| > \epsilon \\ \epsilon^{\mu-1} |\cdot|, & |\cdot| \leq \epsilon \end{cases} \quad (16)$$

In (16), the gain μ typically takes value between 0 and 1 and when $\mu = 1$, it represents linear PI case. To reduce control effort and prevent steady-state ripple amplification, a small tracking error zone is defined using ϵ . Fig. 4 shows the output of the nonlinear function (16) with varying μ (while ϵ remains constant), illustrating that $\mu = 1$ yields a linear output, while other μ values result in nonlinear tracking error-dependent gains. This property of the nonlinear PI controller overcomes the trade-off seen in conventional PI controllers. Note that in the case of very noisy measurements of the DC link voltage, a judicious choice must be made when selecting the gain (μ), as smaller values of μ can amplify the noise. This issue can be mitigated by using an additional pre-loop noise rejection filter, which comes with additional design and tuning complexity.

Power balance in the UPQC DC-link can be written as:

$$p_s = p_l + p_{loss}, \quad (17)$$

where the source power, load power and power loss are denoted by p_s , p_l , and p_{loss} , respectively. In the SRF, the power of the UPQC integrated PMSG-based WEC system can be defined by the active component (d) and the different power and loss components are given by, $p_s = v_{sd}i_{sd}$, $p_l = v_{ld}i_{ld}$, and $p_{loss} = v_{sd}i_{loss}$, respectively where the source, load, and loss currents are denoted by i_{sd} , i_{ld} and i_{loss} . Using eq. (17), the loss current can be derived as [29]:

$$i_{loss} = i_{sd} - (v_{ld}/v_{sd}) i_{ld}. \quad (18)$$

Source current is given by $i_{sd} = i_{ld} + i_{pcd}$ and $i_{pcd} = i_{blnc} + i_{loss}$, where i_{pcd} denotes the parallel converter current in the SRF direct axis, i_{blnc} represents the current flowing through the parallel converter to maintain energy balance in the system when there are differences in voltage amplitude between the source voltage (v_s) at the input of the UPQC and the load voltage (v_l) at the output of the UPQC. The balance current can be derived by substituting the above-mentioned source current formula to eq. (18) as:

$$i_{blnc} = i_{sd} (1 - (v_{sd}/v_{ld})). \quad (19)$$

The power flowing through the parallel converter (p_{pc}) (also the DC-bus (p_{bus})) is defined depending on the energy balance (p_{blnc}) and losses (p_{loss}) in the system as follows:

$$p_{pc} = p_{bus} = p_{blnc} + p_{loss} = v_{ld} (i_{blnc} + i_{loss}), \quad (20)$$

where $p_{bus} = v_{dc}i_{bus} = v_{dc}C_{dc} \frac{dv_{dc}}{dt}$ with i_{dc} being the DC-bus current. Then, using eq. (20) and the definition of p_{bus} , i_{dc} can be obtained as:

$$i_{dc} = (i_{blnc} + i_{loss}) (v_{ld}/v_{dc}) = C \dot{v}_{dc}. \quad (21)$$

Additionally, as the losses of the UPQC are closely tied to the voltage variation between v_{sd} and v_{ld} , a ratio of these voltages can be used to estimate the loss through the gain $\Delta p = 1 - v_{sd}/v_{ld}$ to calculate the feedforward current (i_{dc}^{ff}), which is a function of the N-PI-based DC-link controller output denoted by i_{dc} as

$$i_{dc}^{ff} = i_{dc} \Delta p. \quad (22)$$

Under the assumption $i_{dc} = i_{loss}$ and by substituting eq. (18) into eq. (22), it can be found that:

$$i_{dc}^{ff} = (i_{sd} - i_{ld}) (1 - v_{sd}/v_{ld}). \quad (23)$$

As such, $i_{dc}^{ff} = 0$, only when $v_{sd} = v_{ld}$.

2) Load Reactive Power Compensation

Parallel converter offers an interesting solution to meet the reactive power demand of inductive and highly nonlinear loads, which minimizes reactive power drawn from the source, resulting in improved power quality [30]–[32]. After Clarke's transformation is applied to the three-phase load voltage and currents, the reactive power q_l of the load and compensating

reactive power with a parallel converter q_{pc} can be calculated as follows:

$$\begin{aligned} q_{l\alpha\beta} &= \|\vec{q}_{l\alpha\beta}\| = \left\| [v_{l\alpha} \ v_{l\beta}]^T \wedge [i_{l\alpha} \ i_{l\beta}]^T \right\| \\ &= v_{l\alpha} i_{l\beta} - v_{l\beta} i_{l\alpha}, \end{aligned} \quad (24)$$

$$\begin{aligned} q_{pc\alpha\beta} &= \|\vec{q}_{pc\alpha\beta}\| = \left\| [v_{pc\alpha} \ v_{pc\beta}]^T \wedge [i_{pc\alpha} \ i_{pc\beta}]^T \right\| \\ &= v_{l\alpha} i_{l\beta} - v_{l\beta} i_{l\alpha}, \end{aligned} \quad (25)$$

where $\vec{\cdot}$ indicates the power vector and the instantaneous reactive power has been obtained as a cross product of the voltage and currents in the SRF. Then, the compensating current vector for the load and the parallel converter can be calculated as:

$$\vec{i}_{Cl} = \frac{q_{l\alpha\beta}}{v_{l\alpha\beta}^2} \begin{bmatrix} -v_{l\beta} \\ -v_{l\alpha} \end{bmatrix}, \quad \vec{i}_{Cpc} = \frac{q_{pc\alpha\beta}}{v_{pc\alpha\beta}^2} \begin{bmatrix} -v_{pc\beta} \\ -v_{pc\alpha} \end{bmatrix}. \quad (26)$$

The reactive power vector of the load can be considered as a reference power. Thus, it can be formulated as:

$$\vec{I}_q^* = \Gamma_q (\vec{q}_{l\alpha\beta} - \vec{q}_{pc\alpha\beta}), \quad (27)$$

where $\Gamma_q > 0$ represents the reactive current control gain.

3) Determination of Reference Compensation Current

The strategy for computing the current references of the parallel converter aims to determine the overall positive sequence components of source voltages and load currents. A three-phase version of the proposed PLL from Sec. II-C is utilized to separate positive sequence components. The per-phase balanced currents of the load are expressed by [33]–[35]:

$$i_{blncx} = \sum_{h \in H}^N I_x^{2h+1} \sin((2h+1)\gamma_m(t) + \phi_x^{2h+1}), \quad x \in K \quad (28)$$

where $\gamma(t) = \omega t$ and $\gamma_m(t) = \gamma(t) - (2\pi/3)(m-1)$, with $m = \overline{1,3}$, $K = \{a,b,c\}$ represents the three-phases and $H = \overline{0,N}$ with N being the highest harmonics order being considered. The NLLs current comprises of fundamental, harmonic and negative sequence components. Then, after applying Clarke's transformation to three-phase load currents, unbalanced currents of the load are separated as:

$$\begin{aligned} i_{unl\alpha} &= \sum_{h \in H}^N I_{\alpha s^+}^{2h+1} \sin((2h+1)\gamma_m(t) + \phi_{\alpha s^+}^{2h+1}) - \\ &\quad \sum_{h \in H}^N I_{\alpha s^-}^{2h+1} \cos((2h+1)\gamma_m(t) + \phi_{\alpha s^-}^{2h+1}). \end{aligned} \quad (29)$$

$$\begin{aligned} i_{unl\beta} &= \sum_{h \in H}^N I_{\beta s^+}^{2h+1} \cos((2h+1)\gamma_m(t) + \phi_{\beta s^+}^{2h+1}) - \\ &\quad \sum_{h \in H}^N I_{\beta s^-}^{2h+1} \cos((2h+1)\gamma_m(t) + \phi_{\beta s^-}^{2h+1}). \end{aligned} \quad (30)$$

Then, for ($h=0$), the reference compensation currents of the parallel converter are acquired by subtracting the fundamental positive-sequence components of the load, which is extracted by the proposed PLL, from load currents as:

$$i_{pc,x}^C = i_{unlx} - i_{lx s^+}, \quad (31)$$

where $x \in \{\alpha, \beta\}$ and $i_{unlx} - i_{lx s^+}$ defines components of the harmonic and negative sequence. According to the DC-link controller loop (I_{Fd}^*), reference reactive current component (I_q^*) and the load phase voltages, active and reactive currents injected with the parallel converter can be derived as:

$$\begin{bmatrix} i_{pc,\alpha}^{dc} \\ i_{pc,\beta}^{dc} \end{bmatrix} = \frac{1}{v_{l\alpha\beta}^2} \begin{bmatrix} v_{l\alpha s^+} & -v_{l\beta s^+} \\ v_{l\beta s^+} & v_{l\alpha s^+} \end{bmatrix} \begin{bmatrix} I_{Fd}^* \\ I_q^* \end{bmatrix}, \quad (32)$$

where $v_{l\alpha\beta}^2 = (v_{l\alpha s^+})^2 + (v_{l\beta s^+})^2$. Sensed current signals ($i_{pc,\alpha\beta}$) are compared to the reference compensation currents and injecting active and reactive currents to lessen current error ($i_{pc,\alpha\beta}^e$):

$$\begin{bmatrix} i_{pc,\alpha}^e \\ i_{pc,\beta}^e \end{bmatrix} = \begin{bmatrix} i_{pc,\alpha}^C - i_{pc,\alpha}^{dc} - i_{pc,\alpha} \\ i_{pc,\beta}^C - i_{pc,\beta}^{dc} - i_{pc,\beta} \end{bmatrix}. \quad (33)$$

The input of the current control loop is provided by the error between the sensed currents of the parallel converter and the reference compensation currents. Thanks to this error, the controller results in compensating currents that are employed to remove all types of harmonics in the NLL and wave energy applications as well as providing reactive power demand of the load. The output of the current control loop is fed to PWM modules to produce switching signals for the parallel converter.

III. RESULTS AND DISCUSSIONS

The proposed UPQC control scheme for a wave energy-driven PMSG system was implemented in PSCAD/EMTDC. It was validated under various challenging conditions, including nonlinear, highly inductive, unbalanced loads, and voltage faults. Experimentally obtained WEC torque and power data from the AMC's test pool [5] has been utilized to drive the PMSG for realistic validation, and the system and control parameters are listed in Table I.

A. Performance Analysis Under Various Operating Conditions

This subsection presents results for the proposed UPQC-based control scheme in a wave energy-driven PMSG system, both with and without UPQC. It includes scenarios with sudden additions of nonlinear, highly inductive, unbalanced loads, as well as single and double line-to-ground (SLG) and (DLG) faults on the source side.

The case study in Fig. 5 compares control performance of the system connected to a NLL. At 0.15s, an additional highly inductive NLL is added to the point of common coupling (PCC). The parallel converter compensates for load current harmonics and supplies total reactive power without drawing from the PMSG-based WEC. Results demonstrate effective suppression of load voltage and source current harmonics caused by the NLL, regulation of the DC-bus voltage, and

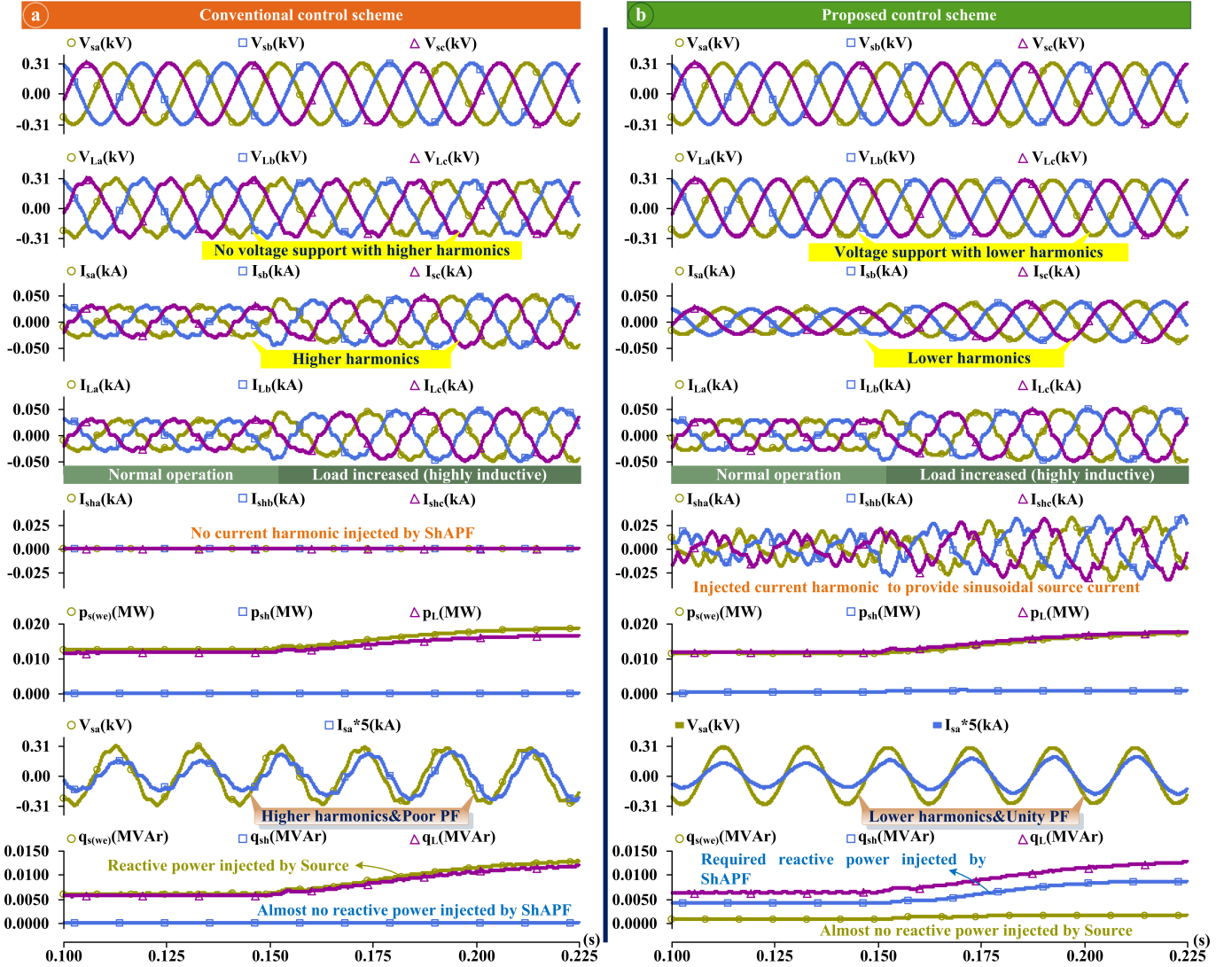


Figure 5. Results of the conventional [14] and proposed control schemes for the wave energy driven PMSG system; a) without UPQC and b) with UPQC.

unity power factor (UPF) assurance. The proposed approach reduces reactive power demand on the parallel converter. Traditional control lacks reactive power control, whereas the proposed control injects 4.1kVAr reactive power for up to 0.15s and then 8.8kVAr to enhance power factor and transient stability, especially under inductive load conditions. Source current (i_{sa}) and load voltage (v_{La}) quality are improved with a THD of 2.01% and 0.7-1.1%, respectively, compared to conventional control with THD values of 13.4% and 7.1%.

The results in Fig. 6 demonstrate substantial improvements in dynamic response and voltage-current harmonic reduction compared to conventional control. A 35% voltage sag SLG fault at 0.1s and the addition of an NLL at 0.15s were used for performance analysis. The proposed N-PI control significantly reduces settling times, fluctuations, and overshoots in DC-bus voltage dynamics, as shown at the bottom of Fig. 6 (b). The contribution of FF current (i_{dc}^{ff}) accelerates system dynamics and helps reduce overshoot and settling time. Large oscillations in DC-bus voltage and unbalanced harmonics in source currents are observed with conventional control,

as depicted in Fig. 6 (a). The proposed N-PI control also improves tracking performance during startup, resulting in a lower voltage error ($\Delta v = 0.3V$), as shown in Fig. 6 (b). The startup time of the DC-bus voltage is reduced from over 40ms in conventional control to around 14ms with the proposed control. Additionally, the proposed control effectively suppresses DC-bus voltage overshoot and deviation during supply fault conditions and load demand changes, enhancing system sustainability and reliability.

In Fig. 7, the system was tested under two common disturbances: DLG fault conditions and additional unbalanced NLL connection. The series converter compensated for a 35% sag in supply voltage, keeping the load voltage constant. The proposed control scheme minimized DC-bus voltage deviation and exhibited negligible steady-state error ($\Delta v = 0.2V$) during unbalanced NLL connection and supply voltage fault conditions. Source currents with the proposed control were nearly sinusoidal, balanced, and had a THD of 1.8%, while the power factor was nearly unity. In contrast, conventional control resulted in source currents with higher harmonics,

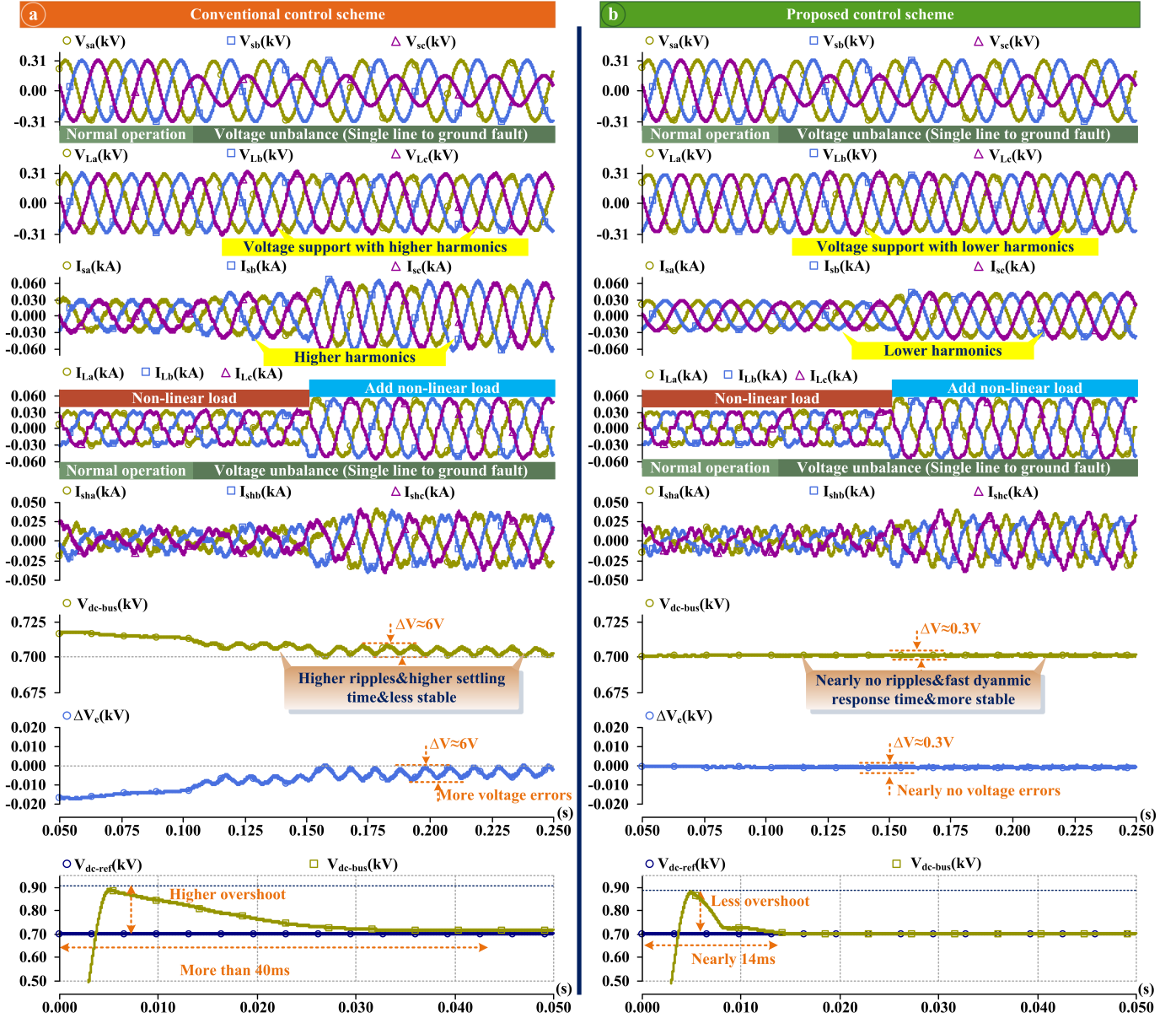


Figure 6. Dynamic response, voltage support and harmonic results of UPQC based wave energy driven PMSG system for a) conventional [14] and b) proposed control schemes under both SLG faults and NLL.

unbalances, and a poor power factor. These results highlight the effectiveness and reliability of the proposed control, and a detailed comparison of source current and load voltage harmonics is provided in Sec. III-B.

B. Comparative Analysis With The Existing Literature

Fig. 8 presents a detailed comparison of A-phase THDs (%) for load voltage and source current under various operating techniques. On the right side of Fig. 8, the proposed control maintains THDs of load voltage and source current below IEEE Std. 519 [16] acceptable limits. Specifically, the THD of source current (around 1.5-2.0%) is significantly lower than the 5% IEEE standard, and the THD of load voltage is below 1.0%, in compliance with IEEE standards. The proposed method employs a harmonically robust PLL along with an adjustable gain controller, which applies substantial

control action for large errors to rapidly reach the reference voltage and smaller action for smaller errors, preventing ripple amplification. These factors distinguish the proposed approach from the conventional counterpart [14].

In Table II, a comparison between the proposed control scheme and recent literature is provided. The UPQC-interfaced wave energy-driven PMSG system with the proposed control outperforms existing methods in terms of reduced THD in source current and load voltage, power factor improvement, accurate fault level tracking, dynamic DC-bus voltage control, and reactive power compensation. The proposed method demonstrates superiority over existing control methods.

IV. CONCLUSION

This study pioneered the use of UPQC in a wave energy-driven PMSG system for power quality improvements. Various

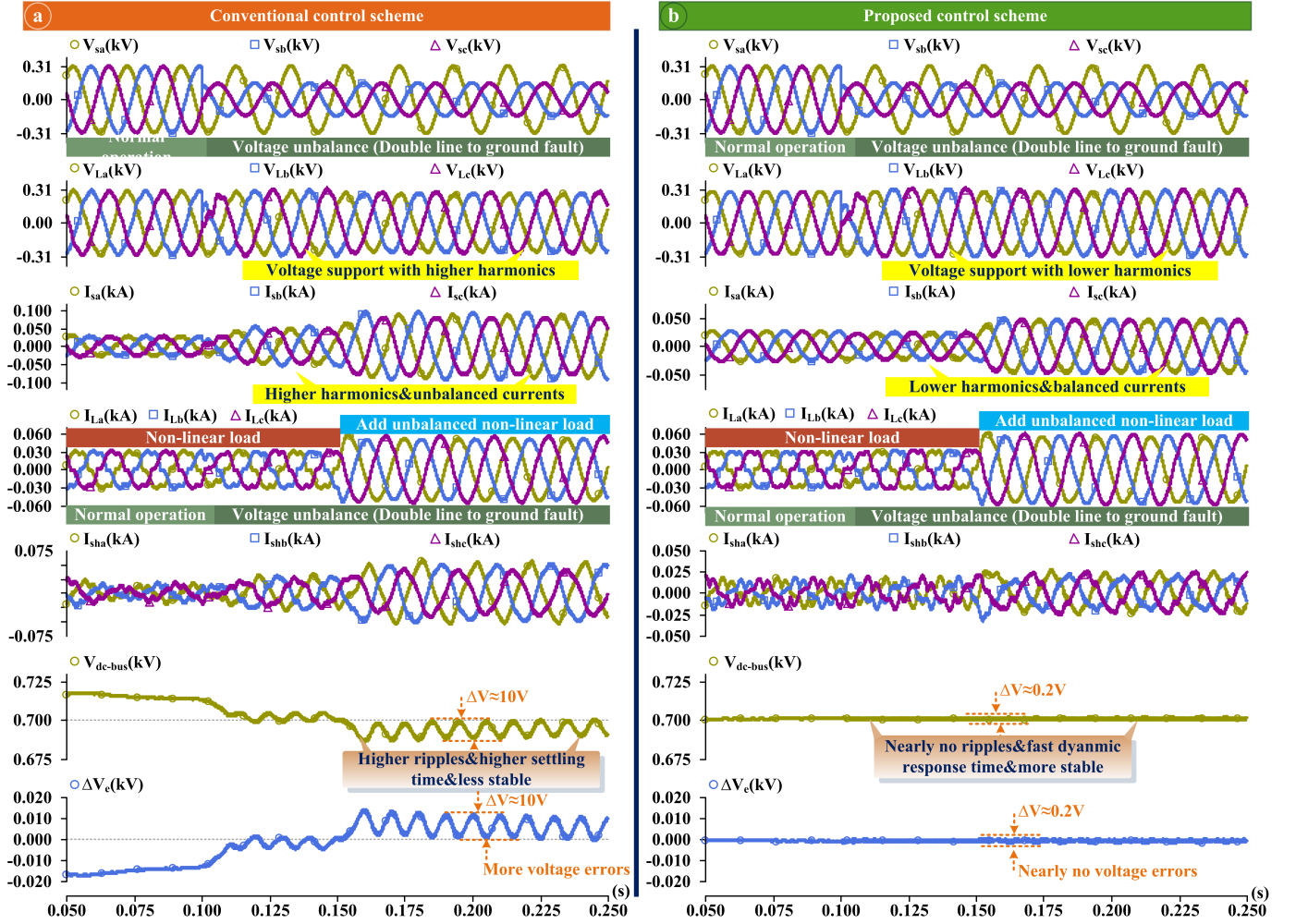


Figure 7. Dynamic response, voltage support and harmonic results of UPQC-based wave energy driven PMSG system for a) conventional [14] and b) proposed control schemes under both DLG faults and unbalanced NLL.

Table I
SYSTEM AND CONTROL PARAMETERS.

System	Description	Specifications
PMSG	AC voltage (L-L)	380V
	Frequency	50Hz
	Power	50kW
	Res. and Ind.	0.005Ω, 0.1mH
Series Converter	Injection transformer	4kVA, 1 : 1 (110V : 110V)
	Damping resistor	0.7Ω
	Filter cap. & ind.	200μF, 1mH
Parallel Converter	Filter inductor	5mH
	Harmonic current	20 – 30A
	Reactive power	10kVar±2kVar
NLLs	Rectifier	15 + j3.15Ω
	Highly inductive NLL	15 + j95Ω
	UNLL	a: 40 – j80Ω, b: 60 – j64Ω, c: 30 – j106Ω
DC-bus	Capacitor (Voltage)	2200μF(800V)
	Switching freq.	10kHz
FFSOGI	$\lambda_s, \tau_m, \lambda_l$	$\sqrt{2}, 5 \times 10^{-3}, 50$
N-PI	$\mu, \epsilon, \lambda_{k_p}, \lambda_{k_i}$	$5 \times 10^{-5}, 15, 50, 10^{-5}$

faults and harmonics causes PQ issues in the proposed system. An enhanced control scheme of the UPQC is proposed to mitigate the PQ issues. A three-phase FFSOGI-QT1-PLL is proposed to fast and accurately extract the fundamental frequency component of the load current for use in the control of parallel converter while single-phase FFSOGI-QT1-PLL has been utilized to identify voltage faults with the series converter control at the generator side. The test results of this method compared to the methods in the literature show that the proposed method stands out better against source voltage faults, unbalanced and highly inductive non-linear various load conditions. In comparison to traditional PI, a new N-PI for the DC-bus voltage control is adopted to provide better tracking performance with lower voltage errors/oscillations, to suppress voltage overshoot and to accelerate the start-up process of the system dynamics. With the proposed control method of the parallel compensator, the DC-bus voltage deviation is kept with $0.2V \sim 0.5V$, the THD of the source current in all cases is kept around $1.5 \sim 2.0\%$, and the THD of the load voltage is less than 1.0% complying with the IEEE standard. Control system presented in this work enhance the dynamic performance of the system under voltage conditions

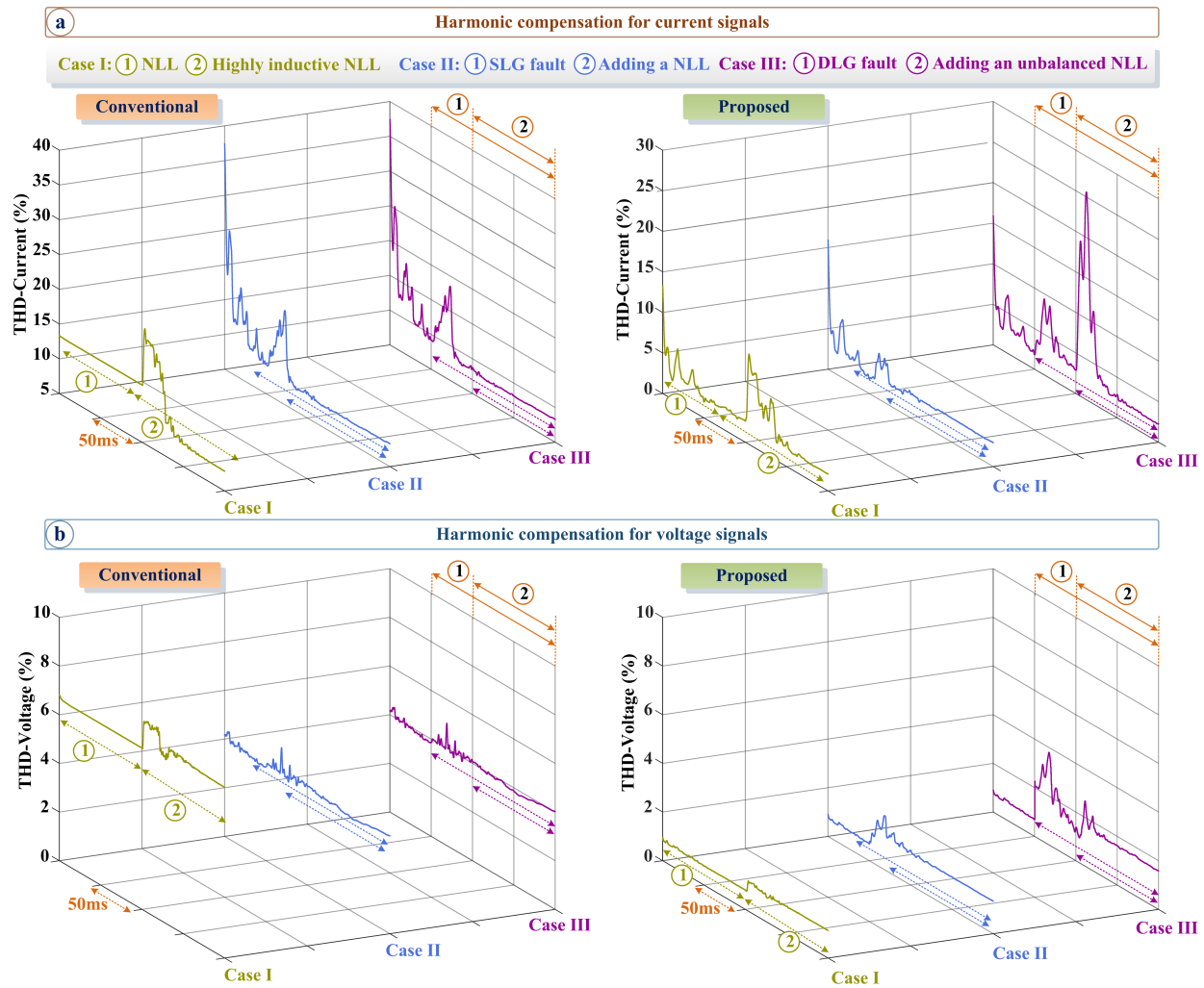


Figure 8. The THD (%) of the load voltage and source current for conventional [14] and proposed control schemes.

Table II
COMPARISON OF THE PROPOSED METHOD WITH THE RECENT LITERATURE.

Method	Energy Source	CVC	APC	RPC	Voltage Harm. Comp. (THD)	Current Harm. Comp. (THD)	Voltage Fault Comp.	IEEE Std. Compliance	CC
[7]	Grid	PI	✗	✓	✗	✓ (~ 1.5%)	✓	✗	Medium
[8]	Grid	PI	✗	✓	✗	✓ (~ 7%)	✗	✗	Low
[9]	Grid	FLPI	✗	✗	✓ (~ 3%)	✓ (~ 3%)	✗	✓	High
[10]	Grid	PI	✗	✓	✓ (~ 2%)	✓ (~ 3%)	✓	✓	Low
[11]	Grid	PI	✓	✗	✗ (> 5%)	✗ (> 2%)	✓	✗	High
[12]	Grid & Wind	PI	✓	✓	✗ (~ 7.7%)	✓ (~ 2%)	✓	✗	High
[13]	Wind	PI	✓	✗	✓	✗	✓	✗	Low
[14]	Hydro	PI	✗	✓	✓ (3.4 – 4.0%)	✓ (4.0 – 5.0%)	✓	✗	Medium
Proposed	Wave	N-PI	✓	✓	✓ (~ 1%)	✓ (1.5 – 2.0%)	✓	✓	High

Capacitor Voltage Control (CVC), Active Power Control (APC), Reactive Power Control (RPC), Computational Complexity (CC)

at the generator side and sudden load change. Comprehensive validation results are provided to demonstrate the advantages of the proposed approach over the conventional counterpart.

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