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A Grid Synchronization PLL with Accurate Extraction Technique of Positive/Negative Sequences and DC-offset under Frequency Drift

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Abstract— **This paper proposes a delayed signal-based demodulation algorithm that enables a fast and accurate extraction of the positive/negative sequences and DC-offset in the grid voltage under a frequency drift. Moreover, a simplified mathematical formalism is proposed to reduce the computational burden for real-time implementation. The algorithm is incorporated with a third-order quasi-type-1 phase-locked loop (TQT1-PLL) to estimate the grid voltage instantaneous phase-angle and frequency. The performance of the proposed PLL referred to as delayed signal demodulation based TQT1-PLL (DSD-TQT1-PLL) is evaluated under highly disturbed grid voltage conditions including DC-offset, fundamental frequency negative sequence (FFNS), characteristic harmonics and frequency variation. The obtained simulation and experimental results show that the proposed PLL can precisely estimate the frequency and the instantaneous phase-angle of the fundamental frequency positive sequence (FFPS) without any ripple. The results showed also its superiority over the conventional and adaptive QT1-PLLs, where a better dynamic response is obtained.**

Index Terms— **DC-offset, distributed power generation, frequency deviation, grid synchronization, moving average filter (MAF), phase-locked loop (PLL), power quality.**

I. Introduction and problem statement

The fast and precise response of the grid side converters (GSC) is becoming increasingly vital especially with the rapid growth in the integration of renewable energy sources (RES) such as wind and photovoltaic power plants. The correct estimation of the grid voltage fundamental parameters such as amplitude, phase and frequency play an important role in the effective operation of the GSC. Indeed, an inaccurate estimation of these parameters may lead to several problems related to the quality of the injected power and the safety of the GSC [1] , [2], [3], [4].

Nowadays, the estimation of grid voltage parameters under ideal condition is very well established where many PLL based synchronization algorithms such as the synchronous reference frame PLL (SRF_PLL) have shown their high performance in terms of accuracy and dynamic response. However, it is still quite challenging to develop a fast synchronization algorithm with a high rejection capability of grid disturbances. The latter are due to characteristic harmonics, the fundamental frequency negative sequence (FFNS), the DC-offset, fundamental frequency deviation, etc. The most severe disturbances remain the DC-offset signals and the FFNS, since they involve the lowest frequency components. Their frequencies in the dq synchronous reference frame are equal to the grid fundamental frequency and twice this frequency, respectively. The aforementioned disturbances give rise to low-frequency ripples in the estimated instantaneous phase and fundamental frequency, which worsens in turn the performance of the GSC in terms of power quality. To overcome this problem, large filters may be used to mitigate the low-frequency ripple. However, these will considerably increase the time response of the synchronization system. Therefore, making a good compromise between the accurate estimation of the grid voltage phase /fundamental frequency and the fast dynamic response is a very important challenge facing the control of GSC and smart grids under disturbed grid voltage conditions.

The appropriate strategy for achieving this objective, widely adopted in recent literature, is to find an optimized filter or processing technique able to eliminate the dominant low-frequency ripples without causing a considerable time delay in the dynamic response [5]. Existing solutions can be grouped as follows:

- The outer loop filtering techniques. For instance, in [6], a moving average filer based prefiltering stage (PMAF) has been used to remove the FFNS and all characteristic harmonics. In [4], the fast delay signal cancellation filter (FDSC) has been used to eliminate the FFSN and /or the DC-offset. Though the aforementioned solutions do not cause a substantial slow-down of the PLL dynamics since they operate outside the loop, however, they are very sensitive to the frequency drift.
- The in-loop filtering techniques: They have been used in the multiple reference frame PLL (MRF-PLL) [7], multiple second-order generalized integrator PLL (MSOGI-PLL) [8] and the multiple complex-coefficient filter PLL (MCCF-PLL) [9] [10] [11]. Though these solutions provide higher performance under disturbed grid conditions, however, their

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implementation is complex and needs a large computation time due to the use of multiple filters and compensators. In this regard, the in-loop MAF was proposed in [12] to reject all low-frequency ripples in the grid voltage. However, it causes a slow dynamic response of the PLL due to its large window-width. To enhance the dynamic performance of the MAF based PLLs, many solutions have been provided in the recent literature. For instance, in [13], a differential MAF (DMAF) that incorporates two special proportional components in the conventional MAF has been proposed to eliminate the FFNS and consequently increase the in-loop filter window width. In [14], a phase-lead compensator has been introduced to compensate the delay caused by the MAF filter. In [15], a QT1-PLL that operates with only a proportional compensator has been proposed to avoid the time delay caused by the integrator. However, the QT1-PLL is vulnerable to the frequency deviation. The problem becomes more adverse under the presence of the DC-offset and the FFNS that generate unwanted low-frequency ripples in the estimated phase and frequency [16], [17]. Many enhanced QT1-PLLs have been developed to achieve a better robustness to frequency deviation such as the QT1-PLL with tunable phase detector [18], the third-order MAF based QT1-PLL [4], the adaptive improved QT1-PLL [19], the cascaded filtering stages based QT1-PLL [20], etc.

- The demodulation techniques (processing techniques): In [21], a Lyapunov demodulator based on an orthogonal signal generation method was proposed. This technique has been incorporated with a MAF filter to enhance the DC-offset and harmonic rejection capability. However, it needs an additional frequency adaptive algorithm to eliminate the errors in the estimated amplitude and phase dues to the frequency deviation. This will inherently be achieved at the cost of additional computational complexity. In [22], a frequency adaptive demodulation technique with a reduced computational burden has been developed to eliminate the FFNS. In [23], the authors proposed a demodulation based open-loop method. However, this method requires a band-pass notch filter to eliminate the FFNS.
- The signal decomposition techniques: In [24], the authors proposed a PLL system that uses Vandermonde matrix to decompose the grid voltage signal. However, the real-time implementation of the method is very complex. Moreover, the proposed decomposition method does not address the removal of DC-offset in the grid voltage.

In view of the above, this paper proposes a new demodulation method based on the delay signal demodulation (DSD) technique, which is able to extract the fundamental frequency positive sequence (FFPS), FFNS, and DC-offset without using any additional filter as opposed to the former research works. The demodulator is incorporated with a third-order quasi-type-1 phase-locked loop (TQT1-PLL); thereafter, the obtained grid synchronization system is named Delayed Signal Demodulation based TQT1-PLL (DSD-TQT1-PLL). Since the FFNS and DC-offset are removed by the DSD, the in-loop filter of the PLL is designed to only reject the harmonics superior or equal to the 5th order. Accordingly, a faster dynamic response of the PLL-loop with robustness against frequency drift is achieved even in presence of the low-frequency ripple caused by the FFNS, DC-offset, and the characteristic harmonics.

II. THE PROPOSED DELAYED SIGNAL BASED DEMODULATION ALGORITHM (DSD)

This section describes the proposed DSD algorithm that allows the extraction of FFPS, FFNS, and DC-offset in the grid voltage. A distorted three-phase grid voltage system with a DC-offset is commonly described using the symmetrical sequence components method as follows:

$$\begin{cases} v_a(t) = \sum_{h=1,7,..,6k+1} V_h^+ \cos\left(h\omega t+\varphi_h^+\right) + \sum_{h=1,5,..,6k-1} V_h^- \cos\left(h\omega t+\varphi_h^-\right) + V_a^{dc} \\ v_b(t) = \sum_{h=1,7,..,6k+1} V_h^+ \cos\left(h\omega t+\varphi_h^+ - \frac{2\pi}{3}\right) + \sum_{h=1,5,..,6k-1} V_h^- \cos\left(h\omega t+\varphi_h^- + \frac{2\pi}{3}\right) + V_b^{dc} \\ v_c(t) = \sum_{h=1,7,..,6k+1} V_h^+ \cos\left(h\omega t+\varphi_h^+ + \frac{2\pi}{3}\right) + \sum_{h=1,5,..,6k-1} V_h^- \cos\left(h\omega t+\varphi_h^- - \frac{2\pi}{3}\right) + V_c^{dc} \end{cases} \quad (1)$$

V_h^+ and V_h^- are the amplitude of the positive and negative sequences, respectively. φ_h^+ and φ_h^- are their initial phases. V_a^{dc}, V_b^{dc}, and V_c^{dc} are the DC-offsets in phases a, b and c, respectively. ω is the grid angular velocity. The voltage system is represented in the α-β stationary reference frame using Clark transformation as follows:

$$\begin{cases} v_\alpha(t) = \sum_{h=1,7,..,6k+1} V_h^+ \cos\left(h\omega t+\varphi_h^+\right) + \sum_{h=1,5,..,6k-1} V_h^- \cos\left(h\omega t+\varphi_h^-\right) + V_\alpha^{dc} \\ v_\beta(t) = \sum_{h=1,7,..,6k+1} V_h^+ \sin\left(h\omega t+\varphi_h^+\right) - \sum_{h=1,5,..,6k-1} V_h^- \sin\left(h\omega t+\varphi_h^-\right) + V_\beta^{dc} \end{cases} \quad (2)$$

With $V_\alpha^{dc} = \frac{2}{3}\left(V_a^{dc} - \frac{1}{2}V_b^{dc} - \frac{1}{2}V_c^{dc}\right)$ and $V_\beta^{dc} = \frac{1}{\sqrt{3}}\left(V_b^{dc} - V_c^{dc}\right)$

Define now $\hat{\omega}$ the angular velocity estimated by the PLL that should be as close as possible to grid velocity ω. The grid voltage could therefore be expressed in a d-q reference frame rotating anti clockwise at $\hat{\omega}$. The dq components of the grid voltage referred to as $v_d(t)$ and $v_q(t)$ are therefore obtained using the following standard transformation:

$$\begin{cases} v_d(t) = v_\alpha(t)\ \cos\left(\hat{\omega}t\right) + v_\beta(t)\ \sin\left(\hat{\omega}t\right) \\ v_q(t) = -v_\alpha(t)\ \sin\left(\hat{\omega}t\right) + v_\beta(t)\ \cos\left(\hat{\omega}t\right) \end{cases} \quad (3)$$

Substituting equation (2) into (3) yields to:

$$\begin{cases} v_d(t) = \left(\begin{array}{l} \sum_{h=1,7,..,6k+1} V_h^+ \cos\left(\left(h\omega-\hat{\omega}\right)t+\varphi_h^+\right) + \sum_{h=1,5,..,6k-1} V_h^- \cos\left(\left(h\omega+\hat{\omega}\right)t+\varphi_h^-\right) \\ \underbrace{+V_\alpha^{dc}\cos\left(\hat{\omega}t\right) + V_\beta^{dc}\sin\left(\hat{\omega}t\right)}_{v_d^{dc}(t)} \end{array} \right) \\ v_q(t) = \left(\begin{array}{l} \sum_{h=1,7,..,6k+1} V_h^+ \sin\left(\left(h\omega-\hat{\omega}\right)t+\varphi_h^+\right) - \sum_{h=1,5,..,6k-1} V_h^- \sin\left(\left(h\omega+\hat{\omega}\right)t+\varphi_h^-\right) \\ \underbrace{+-V_\alpha^{dc}\sin\left(\hat{\omega}t\right) + V_\beta^{dc}\cos\left(\hat{\omega}t\right)}_{v_q^{dc}(t)} \end{array} \right) \end{cases} \quad (4)$$

The αβ components of the grid voltage are now delayed by $N_d T_s$, where T_s is the controller sample period, and N_d is the number of delayed samples. The dq components of the delayed αβ signals referred to as $v_d^{-N_d}(t)$ and $v_q^{-N_d}(t)$ are therefore expressed as follows:

$$\begin{cases} v_d^{-N_d}(t) = \left(\underbrace{\sum_{h=1,7,..6k+1} V_h^+ \cos\left(\left(h\omega - \hat{\omega}\right)t - N_d h\omega T_s + \varphi_h^+\right)}_{v_d^+(t)} + \underbrace{\sum_{h=1,5,..6k-1} V_h^- \cos\left(\left(h\omega + \hat{\omega}\right)t - N_d h\omega T_s + \varphi_h^-\right)}_{v_d^-(t)} + v_d^{dc}(t) \right) \\ v_q^{-N_d}(t) = \left(\underbrace{\sum_{h=1,7,..6k+1} V_h^+ \sin\left(\left(h\omega - \hat{\omega}\right)t - N_d h\omega T_s + \varphi_1^+\right)}_{v_q^+(t)} - \underbrace{\sum_{h=1,5,..6k-1} V_h^- \sin\left(\left(h\omega + \hat{\omega}\right)t - N_d h\omega T_s + \varphi_1^-\right)}_{v_q^-(t)} + v_q^{dc}(t) \right) \end{cases} \quad (5)$$

$v_d^+(t)$, $v_d^-(t)$ and $v_d^{dc}(t)$ are the positive, negative and DC components of $v_d^{-N_d}(t)$. $v_q^+(t)$, $v_q^-(t)$ and $v_q^{dc}(t)$ are the positive, negative and DC components of $v_q^{-N_d}(t)$. Similarly, we define $v_d^{-2N_d}(t)$ and $v_q^{-2N_d}(t)$, the dq components of the grid voltage delayed by $2N_d T_s$ such that:

$$\begin{cases} v_d^{-2N_d}(t) = \left(\sum_{h=1,7,..6k+1} V_h^+ \cos\left(\left(h\omega - \hat{\omega}\right)t - 2N_d h\omega T_s + \varphi_h^+\right) + \sum_{h=1,5,..6k-1} V_h^- \cos\left(\left(h\omega + \hat{\omega}\right)t - 2N_d h\omega T_s + \varphi_h^-\right) + v_d^{dc}(t) \right) \\ v_q^{-2N_d}(t) = \left(\sum_{h=1,7,..6k+1} V_h^+ \sin\left(\left(h\omega - \hat{\omega}\right)t - 2N_d h\omega T_s + \varphi_1^+\right) - \sum_{h=1,5,..6k-1} V_h^- \sin\left(\left(h\omega + \hat{\omega}\right)t - 2N_d h\omega T_s + \varphi_1^-\right) + v_q^{dc}(t) \right) \end{cases} \quad (6)$$

Assume now harmonics of order $h \geq 5$ are filtered outside the DSD block as will be explained in the next section. Therefore, the expressions of $v_d(t), v_q(t)$, $v_d^{-2N_d}(t)$ and $v_q^{-2N_d}(t)$ established in equations (4) and (6) can now be written in terms of $v_d^+(t)$, $v_d^-(t)$, $v_d^{dc}(t)$, $v_q^+(t)$, $v_q^-(t)$ and $v_q^{dc}(t)$ as follows :

$$\begin{cases} v_d(t) = \left(\left[\cos(N_d\omega T_s) v_d^+(t) - \sin(N_d\omega T_s) v_q^+(t) \right] + \left[\cos(N_d\omega T_s) v_d^-(t) - \sin(N_d\omega T_s) v_q^-(t) \right] + v_d^{dc}(t) \right) \\ v_q(t) = \left(\left[\sin(N_d\omega T_s) v_d^+(t) + \cos(N_d\omega T_s) v_q^+(t) \right] - \left[\sin(N_d\omega T_s) v_d^-(t) + \cos(N_d\omega T_s) v_q^-(t) \right] + v_q^{dc}(t) \right) \end{cases} \quad (7)$$

$$\begin{cases} v_d^{-2N_d}(t) = \left(\left[\cos(N_d\omega T_s) v_d^+(t) + \sin(N_d\omega T_s) v_q^+(t) \right] + \left[\cos(N_d\omega T_s) v_d^-(t) + \sin(N_d\omega T_s) v_q^-(t) \right] + v_d^{dc}(t) \right) \\ v_q^{-2N_d}(t) = \left(\left[-\sin(N_d\omega T_s) v_d^+(t) + \cos(N_d\omega T_s) v_q^+(t) \right] - \left[-\sin(N_d\omega T_s) v_d^-(t) + \cos(N_d\omega T_s) v_q^-(t) \right] + v_q^{dc}(t) \right) \end{cases} \quad (8)$$

Equations (5), (7) and (8) can be grouped together, which yields to the following matrix relationship:

$$\left[v_d(t) \quad v_d^{-N_d}(t) \quad v_d^{-2N_d}(t) \quad v_q(t) \quad v_q^{-N_d}(t) \quad v_q^{-N_d}(t) \right]^t = [\boldsymbol{M}] \left[v_d^+(t) \quad v_q^+(t) \quad v_d^-(t) \quad v_q^-(t) \quad v_d^{dc}(t) \quad v_q^{dc}(t) \right]^t \quad (9)$$

And

$$[\boldsymbol{M}] = \begin{bmatrix} \cos(N_d\omega T_s) & -\sin(N_d\omega T_s) & \cos(N_d\omega T_s) & -\sin(N_d\omega T_s) & 1 & 0 \\ 1 & 0 & 1 & 0 & 1 & 0 \\ \cos(N_d\omega T_s) & \sin(N_d\omega T_s) & \cos(N_d\omega T_s) & \sin(N_d\omega T_s) & 1 & 0 \\ \sin(N_d\omega T_s) & \cos(N_d\omega T_s) & -\sin(N_d\omega T_s) & -\cos(N_d\omega T_s) & 0 & 1 \\ 0 & 1 & 0 & -1 & 0 & 1 \\ -\sin(N_d\omega T_s) & \cos(N_d\omega T_s) & \sin(N_d\omega T_s) & -\cos(N_d\omega T_s) & 0 & 1 \end{bmatrix} \quad (10)$$

Considering this, we can theoretically determine the components $v_d^+(t), v_d^-(t), v_d^{dc}(t), v_q^+(t)$, $v_q^-(t)$ and $v_q^{dc}(t)$ by computing the inverse matrix of **[*M*]**. The expression of **[*M*]$^{-1}$** is given in as follows:

$$[\boldsymbol{M}]^{-1} = \frac{-1}{8xy} \begin{bmatrix} x & -2x & x & -2y & 0 & 2y \\ 2y & 0 & -2y & x & -2x & x \\ x & -2x & x & 2y & 0 & -2y \\ 2y & 0 & -2y & -x & 2x & -x \\ -2x & 2z & -2x & 0 & 0 & 0 \\ 0 & 0 & 0 & -2x & 2z & -2x \end{bmatrix} \quad (11)$$

$x = \sin\left(N_d\omega T_s\right)$, $y = \sin^2\left(N_d\omega T_s/2\right)$ and $z = \sin\left(2N_d\omega T_s\right)$

As can be seen, the terms *x*, *y*, and *z* in **[*M*]$^{-1}$** depend on ω. Therefore, to properly estimate these quantities, we shall simply substitute ω by its estimated value $\hat{\omega}$ determined by the PLL system, which yields to:

$$\hat{x} = \sin\left(N_d\hat{\omega}T_s\right), \hat{y} = \sin^2\left(N_d\hat{\omega}T_s/2\right) \text{ and } \hat{z} = \sin\left(N_d 2\hat{\omega}T_s\right) \quad (12)$$

The estimated matrix of **[*M*]$^{-1}$** referred to as $\left[\hat{\boldsymbol{M}}\right]^{-1}$ is therefore computed using (11) and (12), respectively. Considering this, we can estimate $v_d^+(t), v_d^-(t)$, $v_d^{dc}(t)$, $v_q^+(t)$, $v_q^-(t)$ and $v_q^{dc}(t)$ by simply computing $\left[\hat{\boldsymbol{M}}\right]^{-1}$ which yields to equation (13a). This latter is indeed useful to estimate in real-time the FFPS, FFNS and DC-offset of the grid voltage using the updated value of $\hat{\omega}$ and the delayed dq components of the grid voltage. However, it is clear that the main drawback of the relationship provided in equation (13a) is the need for a high computational effort to implement in real-time the trigonometric functions related to the computation of the three variables $\hat{x}$, $\hat{y}$, and $\hat{z}$ defined in equation (12).

$$\begin{cases} \hat{v}_d^+(t) = \dfrac{\hat{x}\left(v_d(t) - 2v_d^{-N_d}(t) + v_d^{-2N_d}(t)\right) - 2\hat{y}\left(v_q(t) - v_q^{-2N_d}(t)\right)}{-8\hat{x}\,\hat{y}} \\ \hat{v}_q^+(t) = \dfrac{2\hat{y}\left(v_d(t) - v_d^{-2N_d}(t)\right) + \hat{x}\left(v_q(t) - 2v_q^{-N_d}(t) + v_q^{-2N_d}(t)\right)}{-8\hat{x}\,\hat{y}} \\ \hat{v}_d^-(t) = \dfrac{\hat{x}\left(v_d(t) - 2v_d^{-N_d}(t) + v_d^{-2N_d}(t)\right) + 2\hat{y}\left(v_q(t) - v_q^{-2N_d}(t)\right)}{-8\hat{x}\,\hat{y}} \\ \hat{v}_q^-(t) = \dfrac{2\hat{y}\left(v_d(t) - v_d^{-2N_d}(t)\right) - 2\hat{x}\left(v_q(t) - 2v_q^{-N_d}(t) + v_q^{-2N_d}(t)\right)}{-8\hat{x}\,\hat{y}} \\ \hat{v}_d^{dc}(t) = \dfrac{-2\hat{x}\left(v_d(t) + v_d^{-2N_d}(t)\right) + 2\hat{z}\left(v_d^{-N_d}(t)\right)}{-8\hat{x}\,\hat{y}} \\ \hat{v}_q^{dc}(t) = \dfrac{-2\hat{x}\left(v_q(t) + v_q^{-2N_d}(t)\right) + 2\hat{z}\left(v_q^{-N_d}(t)\right)}{-8\hat{x}\,\hat{y}} \end{cases} \quad (13a)$$

In this regard, we developed a simplified mathematical relationship that allows a straightforward computation of $\hat{x}$, $\hat{y}$ and $\hat{z}$ without using any time consuming trigonometric function. Indeed, consider the variables $\cos(\hat{\omega}t)$ and $\sin(\hat{\omega}t)$ computed by the PLL system regardless the used demodulation method. Therefore, we can deduce the delayed functions $\cos(\hat{\omega}(t - N_d T_s))$ and $\sin(\hat{\omega}(t - N_d T_s))$ by adding simply N_d delays. This needs only N_d memory addresses to store the past values of $\cos(\hat{\omega}t)$ and $\sin(\hat{\omega}t)$. On the other hand, by making some mathematical developments, we can prove that the trigonometric functions $\cos(N_d\hat{\omega}T_s)$ and $\sin(N_d\hat{\omega}T_s)$ can be deduced from the variables $\cos(\hat{\omega}t)$ and $\sin(\hat{\omega}t)$ determined by the PLL system and their delayed counterparts as follows:

$$\begin{cases} \cos(N_d\hat{\omega}T_s) = \begin{pmatrix} \cos(\hat{\omega}t)\cos(\hat{\omega}(t - N_d T_s)) \\ +\sin(\hat{\omega}t)\sin(\hat{\omega}(t - N_d T_s)) \end{pmatrix} \\ \sin(N_d\hat{\omega}T_s) = \begin{pmatrix} \sin(\hat{\omega}t)\cos(\hat{\omega}(t - N_d T_s)) \\ -\cos(\hat{\omega}t)\sin(\hat{\omega}(t - N_d T_s)) \end{pmatrix} \end{cases} \quad (13b)$$

Considering this, we can use the following relationship enabling the computation of the variables $\hat{x}$, $\hat{y}$ and $\hat{z}$ without using any additional trigonometric function.

$$\begin{cases} \hat{x} = \sin(N_d\hat{\omega}T_s) \\ \hat{y} = \sin^2(N_d\hat{\omega}T_s/2) = \dfrac{1 - \cos(N_d\hat{\omega}T_s)}{2} \\ \hat{z} = \sin(2N_d\hat{\omega}T_s) = 2\sin(N_d\hat{\omega}T_s)\cos(N_d\hat{\omega}T_s) \end{cases} \quad (13c)$$

In view of this, by substituting (13b) and (13c) into (13a), we can estimate the FFPS, FFNS and DC-offset of the grid voltage using only the basic mathematical operators (+, - and /) which practically needs only one clock cycle for their real-time implementation on digital signal processors.

In order to show analytically the accuracy of the estimation equation (13a), the components $v_d(t)$, $v_q(t)$, $v_d^{-2N_d}(t)$ and $v_q^{-2N_d}(t)$ are substituted by their expressions as given in equations (5), (7) and (8) which yields to equation (14). Replacing now the terms $\hat{x}$, $\hat{y}$ and $\hat{z}$ by their respective equivalent expressions as given by equations (12, 13b and 13c) yields to equation (15).

$$\begin{cases} \hat{v}_d^+(t) = \dfrac{\left\{\begin{matrix} 2\hat{x}\left(\cos(N_d\omega T_s) - 1\right)\left(v_d^+(t) + v_d^-(t)\right) \\ -4\hat{y}\sin(N_d\omega T_s)\left(v_d^+(t) - v_d^-(t)\right) \end{matrix}\right\}}{-8\hat{x}\,\hat{y}} \\ \hat{v}_q^+(t) = \dfrac{\left\{\begin{matrix} -4\hat{y}\sin(N_d\omega T_s)\left(v_q^+(t) + v_q^-(t)\right) \\ +2\hat{x}\left(\cos(N_d\omega T_s) - 1\right)\left(v_q^+(t) - v_q^-(t)\right) \end{matrix}\right\}}{-8\hat{x}\,\hat{y}} \\ \hat{v}_d^-(t) = \dfrac{\left\{\begin{matrix} 2\hat{x}\left(\cos(N_d\omega T_s) - 1\right)\left(v_d^+(t) + v_d^-(t)\right) \\ +4\hat{y}\sin(N_d\omega T_s)\left(v_d^+(t) - v_d^-(t)\right) \end{matrix}\right\}}{-8\hat{x}\,\hat{y}} \\ \hat{v}_q^-(t) = \dfrac{\left\{\begin{matrix} -4\hat{y}\sin(N_d\omega T_s)\left(v_q^+(t) + v_q^-(t)\right) \\ -2\hat{x}\left(\cos(N_d\omega T_s) - 1\right)\left(v_q^+(t) - v_q^-(t)\right) \end{matrix}\right\}}{-8\hat{x}\,\hat{y}} \\ \hat{v}_d^{dc}(t) = \dfrac{\left\{\begin{matrix} -4\hat{x}\left(\cos(N_d\omega T_s)\left(v_d^+(t) + v_d^-(t)\right) + v_d^{dc}(t)\right) \\ +2\hat{z}\left(v_d^+(t) + v_d^-(t) + v_d^{dc}(t)\right) \end{matrix}\right\}}{-8\hat{x}\,\hat{y}} \\ \hat{v}_q^{dc}(t) = \dfrac{\left\{\begin{matrix} -4\hat{x}\left(\cos(N_d\omega T_s)\left(v_q^+(t) - v_q^-(t)\right) + v_q^{dc}(t)\right) \\ +2\hat{z}\left(v_q^+(t) - v_q^-(t) + v_q^{dc}(t)\right) \end{matrix}\right\}}{-8\hat{x}\,\hat{y}} \end{cases} \quad (14)$$

When the grid frequency is precisely estimated by the PLL i.e. $\hat{\omega} \cong \omega$, we can verify that the estimated components of the grid voltage are effectively equal to their real values i.e. $\hat{v}_i^+(t) = v_i^+(t)$, $\hat{v}_i^-(t) = v_i^-(t)$ and $\hat{v}_i^{dc}(t) = v_i^{dc}(t)$ ($i = d, q$). This outcome confirms the accuracy of the designed extraction equation (13a) of the proposed DSD algorithm.

From this analysis, we can deduce that the proposed DSD algorithm has the following advantages:

- Compared to the QT1-PLL technique that extracts only the FFPS of the grid voltage, the proposed method enables also the extraction of the DC-offset and FFNS.
- This technique allows the increase of the MAF window width in PLL systems i.e. it enhances its dynamic response. Indeed, the MAF filter will be exempt from the attenuation of the DC-offset and FFNS.
- It does not use any adaptive filter to avoid the problem of frequency variation. Notice that the real-time implementation of adaptive filters increases the computational burden and memory resources due to the implementation of the fractional delay term [4]. As for the proposed method, the adaptive terms in matrix $\left[\hat{\boldsymbol{M}}\right]^{-1}$ ($\hat{x}$, $\hat{y}$ and $\hat{z}$) are implemented in real-time without using any additional resources.

$$
\begin{cases}
\hat{v}_d^+(t) = \dfrac{\left(2\sin\left(N_d\hat{\omega}T_s\right)\left(\cos(N_d\omega T_s)-1\right)-4\sin^2\left(N_d\hat{\omega}T_s/2\right)\sin(\omega N_d T_s)\right)v_d^+(t)+\left(2\sin\left(N_d\hat{\omega}T_s\right)\left(\cos(N_d\omega T_s)-1\right)+4\sin^2\left(N_d\hat{\omega}T_s/2\right)\sin(N_d\omega T_s)\right)v_d^-(t)}{-8\sin\left(N_d\hat{\omega}T_s\right)\sin^2\left(N_d\hat{\omega}T_s/2\right)} \\
\hat{v}_q^+(t) = \dfrac{\left(-4\sin^2\left(N_d\hat{\omega}T_s/2\right)\sin(N_d\omega T_s)+2\sin\left(N_d\hat{\omega}T_s\right)\left(\cos(N_d\omega T_s)-1\right)\right)v_q^+(t)-\left(4\sin^2\left(N_d\hat{\omega}T_s/2\right)\sin(N_d\omega T_s)+2\sin\left(N_d\hat{\omega}T_s\right)\left(\cos(N_d\omega T_s)-1\right)\right)v_q^-(t)}{-8\sin\left(N_d\hat{\omega}T_s\right)\sin^2\left(N_d\hat{\omega}T_s/2\right)} \\
\hat{v}_d^-(t) = \dfrac{\left(2\sin\left(N_d\hat{\omega}T_s\right)\left(\cos(N_d\omega T_s)-1\right)-4\sin^2\left(N_d\hat{\omega}T_s/2\right)\sin(N_d\omega T_s)\right)v_d^-(t)+\left(2\sin\left(N_d\hat{\omega}T_s\right)\left(\cos(N_d\omega T_s)-1\right)+4\sin^2\left(N_d\hat{\omega}T_s/2\right)\sin(N_d\omega T_s)\right)v_d^+(t)}{-8\sin\left(N_d\hat{\omega}T_s\right)\sin^2\left(N_d\hat{\omega}T_s/2\right)} \\
\hat{v}_q^-(t) = \dfrac{\left(-4\sin^2\left(N_d\hat{\omega}T_s/2\right)\sin(N_d\omega T_s)+2\sin\left(N_d\hat{\omega}T_s\right)\left(\cos(N_d\omega T_s)-1\right)\right)v_q^-(t)-\left(4\sin^2\left(N_d\hat{\omega}T_s/2\right)\sin(N_d\omega T_s)+2\sin\left(N_d\hat{\omega}T_s\right)\left(\cos(N_d\omega T_s)-1\right)\right)v_q^+(t)}{-8\sin\left(N_d\hat{\omega}T_s\right)\sin^2\left(N_d\hat{\omega}T_s/2\right)} \\
\hat{v}_d^{dc}(t) = \dfrac{\left(-4\sin\left(N_d\hat{\omega}T_s\right)+2\sin\left(2N_d\hat{\omega}T_s\right)\right)v_d^{dc}(t)+\left(-4\sin\left(N_d\hat{\omega}T_s\right)\cos(N_d\omega T_s)+2\sin\left(2N_d\hat{\omega}T_s\right)\right)\left(v_d^+(t)+v_d^-(t)\right)}{-8\sin\left(N_d\hat{\omega}T_s\right)\sin^2\left(N_d\hat{\omega}T_s/2\right)} \\
\hat{v}_q^{dc}(t) = \dfrac{\left(-4\sin\left(N_d\hat{\omega}T_s\right)+2\sin\left(2N_d\hat{\omega}T_s\right)\right)v_q^{dc}(t)+\left(-4\sin\left(N_d\hat{\omega}T_s\right)\cos(N_d\omega T_s)+2\sin\left(2N_d\hat{\omega}T_s\right)\right)\left(v_q^+(t)-v_q^-(t)\right)}{-8\sin\left(N_d\hat{\omega}T_s\right)\sin^2\left(N_d\hat{\omega}T_s/2\right)}
\end{cases}
\tag{15}
$$

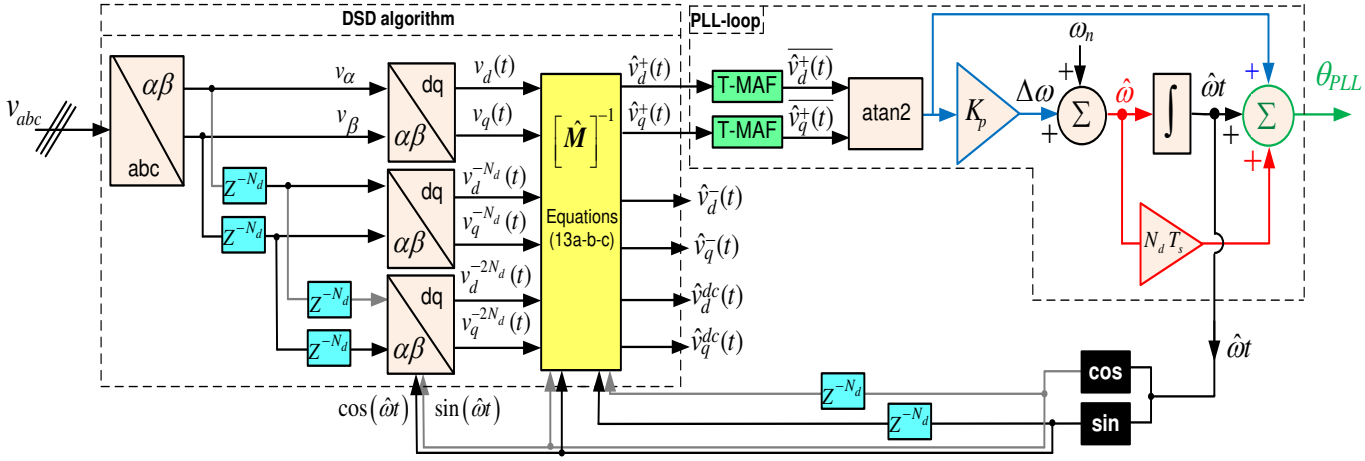

Fig. 1 Structure of the proposed DSD-TQT1-PLL.

III. Implementation with a PLL System: The Proposed DSD-TQT1-PLL

The proposed DSD algorithm can be used with any type of PLL system. In this paper, it is incorporated with a TQT1-PLL as depicted in the block diagram of Fig.1. The obtained PLL is therefore, referred to as DSD-TQT1-PLL. The dq components of the FFPS, FFNS and DC-offset of the grid voltage are extracted using equations (13a-b-c). This implies that the estimated components $\hat{v}_d^+(t)$ and $\hat{v}_q^+(t)$ are free of the FFNS and DC-offset that may exist in the grid voltage. The latter ($\hat{v}_d^+(t)$ and $\hat{v}_q^+(t)$) are thereafter fed to the input of the PLL loop. A third-order MAF (T-MAF) is used to filter out the remaining harmonics that may be involved in these extracted components. This filter enables a high filtering capability even under a frequency drift without the need of any adaptive algorithm. The T-MAF is implemented in a similar manner as done in [2] using three cascaded MAF blocks with a window width equal to 100/3 as shown in the block diagram of Fig.2.

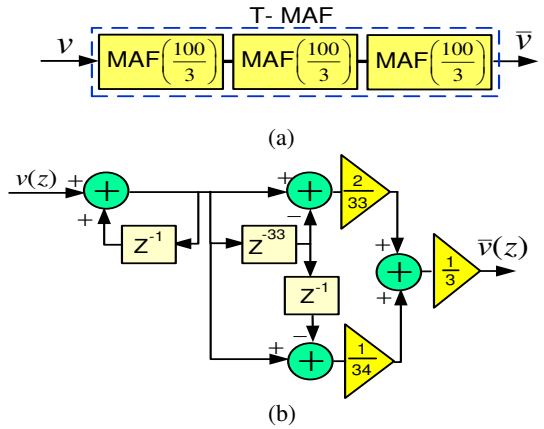

Fig. 2 (a) Implementation of the TMAF using three cascaded MAF (100/3) (b) discrete implementation of a MAF (100/3).

The filtered dq components of the positive sequence $\overline{\hat{v}_d^+(t)}$ and $\overline{\hat{v}_q^+(t)}$ are used to estimate the grid frequency or velocity $\hat{\omega}$ and the instantaneous phase $\hat{\omega}t$ which are needed to implement equations (13a-b-c) and the Park transformation. Moreover, an offset phase-angle equal to (N_d T_s) is added to the output of the PLL to compensate the effect of the delay blocks (z^{-N_d}) used by the extraction algorithm. It is worth mentioning that only the dq components of the FFPS extracted by the DSD algorithm are useful for the PLL-loop. This implies that we can considerably reduce the computational burden of the extraction method since only the first two relationships of equation (13a) are implemented. The extraction of the dq components of the FFNS ($\hat{v}_d^-(t)$ and $\hat{v}_q^-(t)$) are useful for the control of grid-connected inverters under unbalanced grid voltage in a double synchronous reference frame (DSRF-PLL). Moreover, the extracted last 4 components in equation (13a) i.e. $\hat{v}_d^-(t)$, $\hat{v}_q^-(t)$, $\hat{v}_d^{dc}(t)$ and $\hat{v}_q^-(t)$ are useful for other applications such as the active filters, which are beyond the scope of this paper. In this case, we can identify the maximum amplitude and instantaneous phase of the negative sequence ($\hat{V}_1^-$ and $\hat{\theta}_1^-$) as well as the DC-offsets ($\hat{v}_a^{dc}$, $\hat{v}_b^{dc}$ and $\hat{v}_c^{dc}$) using a simple algorithm as illustrated in the block diagram of Fig.3. Once more, we use the T-MAF filer is to enable a high filtering of the remaining harmonics (5th, 7th, etc) under a frequency drift without the need for any adaptive algorithm.

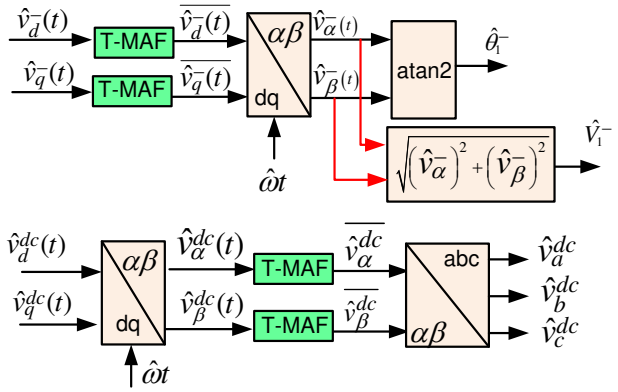

Fig. 3 Extraction of $\hat{V}_1^-$ and $\hat{\theta}^-$ of the FFNS and the DC-offsets $\hat{v}_a^{dc}$, $\hat{v}_b^{dc}$ and $\hat{v}_c^{dc}$.

IV. Numerical Simulation and Real-Time Implementation

A. N_d delay selection

The choice of the delay N_d for real-time implementation was determined based on simulation results to optimize the PLL accuracy, settling time, and overshoot in the transient regime. In order to integrate the proposed algorithm into any PLL system without altering its parameters and performance, we keep both the sampling time T_s and the compensator parameters constant. To illustrate the impact of the term N_dT_s on the PLL dynamic performance, we first provided an equivalent expression of equation (15) as given in (16a), which reveals four specific gains of the DSD namely GSD_1, $GDSD_0$, $GDSD\_{1DC}$ and $GDSD\_{0DC}$, respectively.

$$\begin{cases} \hat{v}_d^+(t) = G_{DSD1}\, v_d^+(t) + G_{DSD0}\, v_d^-(t) \\ \hat{v}_q^+(t) = G_{DSD1}\, v_q^+(t) - G_{DSD0}\, v_q^-(t) \\ \hat{v}_d^-(t) = G_{DSD1}\, v_d^-(t) + G_{DSD0}\, v_d^+(t) \\ \hat{v}_q^-(t) = G_{DSD1}\, v_q^-(t) - G_{DSD0}\, v_q^+(t) \\ \hat{v}_d^{dc}(t) = G_{DSD\_1DC}\, v_d^{dc}(t) + G_{DSD\_0DC}\left(v_d^+(t) + v_d^-(t)\right) \\ \hat{v}_q^{dc}(t) = G_{DSD_{1\_DC}}\, v_q^{dc}(t) + G_{DSD\_0DC}\left(v_q^+(t) - v_q^-(t)\right) \end{cases} \quad (16a)$$

Their analytical expressions are given in equation (16b).

$$\begin{cases} G_{DSD_1} = \dfrac{2\sin\left(N_d\hat{\omega}T_s\right)\left(\cos(N_d\omega T_s)-1\right) - 4\sin^2\left(N_d\hat{\omega}T_s/2\right)\sin(\omega N_dT_s)}{-8\sin\left(N_d\hat{\omega}T_s\right)\sin^2\left(N_d\hat{\omega}T_s/2\right)} \\ G_{DSD_0} = \dfrac{2\sin\left(N_d\hat{\omega}T_s\right)\left(\cos(N_d\omega T_s)-1\right) + 4\sin^2\left(N_d\hat{\omega}T_s/2\right)\sin(N_d\omega T_s)}{-8\sin\left(N_d\hat{\omega}T_s\right)\sin^2\left(N_d\hat{\omega}T_s/2\right)} \\ G_{DSD_{1\_DC}} = \dfrac{-4\sin\left(N_d\hat{\omega}T_s\right) + 2\sin\left(2N_d\hat{\omega}T_s\right)}{-8\sin\left(N_d\hat{\omega}T_s\right)\sin^2\left(N_d\hat{\omega}T_s/2\right)} \\ G_{DSD_{0\_DC}} = \dfrac{-4\sin\left(N_d\hat{\omega}T_s\right)\cos(N_d\omega T_s) + 2\sin\left(2N_d\hat{\omega}T_s\right)}{-8\sin\left(N_d\hat{\omega}T_s\right)\sin^2\left(N_d\hat{\omega}T_s/2\right)} \end{cases} \quad (16b)$$

It is clear that GSD_1 and $GDSD\_{1DC}$ should be equal to 1, while the remaining two gains $GDSD_0$ and $GDSD\_{0DC}$ must be zero to obtain a perfect extraction of the FFPS, FFNS, and DC-offset of the grid voltage. Substituting now the relationships defined in equation (13c) into (16b), yields:

$$\begin{cases} G_{DSD1} = \dfrac{\sin\left(N_d\hat{\omega}T_s\right)\sin^2\left(N_d\omega T_s/2\right) + \sin(N_d\omega T_s)\sin^2\left(N_d\hat{\omega}T_s/2\right)}{2\sin\left(N_d\hat{\omega}T_s\right)\sin^2\left(N_d\hat{\omega}T_s/2\right)} \\ G_{DSD0} = \dfrac{\sin\left(N_d\hat{\omega}T_s\right)\sin^2\left(N_d\omega T_s/2\right) - \sin(N_d\omega T_s)\sin^2\left(N_d\hat{\omega}T_s/2\right)}{2\sin\left(N_d\hat{\omega}T_s\right)\sin^2\left(N_d\hat{\omega}T_s/2\right)} \\ G_{DSD\_1DC} = 1 \\ G_{DSD\_0DC} = \dfrac{\cos(N_d\omega T_s) - \cos\left(N_d\hat{\omega}T_s\right)}{2\sin^2\left(N_d\hat{\omega}T_s/2\right)} \end{cases} \quad (16c)$$

Equation (16c) reveals that GDS_{1_DC} is always equal to 1, while the remaining three gains of the DSD algorithm may slightly vary only in transient regime. Their deviation from the exact values depends only on the term N_dT_s and the frequency estimation error $\Delta f_{PLL} = \dfrac{(\omega - \hat{\omega})}{2\pi}$. Indeed, after the convergence of the PLL to the steady state regime i.e. $\hat{\omega} \approx \omega$ implying also $N_d\hat{\omega}T_s = N_d\omega T_s$, we can verify from (16.c) that G_{DSD1} =1, while G_{DSD0} = G_{DSD_DC0} = 0. However, under grid frequency variation, the PLL will experience a transient regime before the convergence to the new grid frequency. During the settling time, the deviation of the estimated frequency from the real grid frequency is not negligible particularly if the transient overshoot is important. To evaluate the accuracy of the proposed DSD gains in transient regime, we computed the gains versus N_dT_s for different values of the frequency error. The obtained curves computed for a nominal grid frequency equal to 50 Hz are displayed in Figs. 4a-b-c. It is clear, when

N_dT_s varies from 6 ms to 7 ms, the deviation of the three gains from their exact values is less than 2% even for Δf_{PLL} = ±2 Hz, confirming the accuracy of the obtained gains in transient regime and for important deviations from the nominal grid frequency.

To determine the appropriate value of N_dT_s within the interval [6ms, 7ms] and considering additional performance criteria such as the overshoot and the settling time of the PLL during the transient regime, three numerical simulations are carried out with : N_dT_s = 6.0 ms, N_dT_s = 6.3 ms and N_dT_s = 6.6 ms, respectively. The obtained results reveal that N_dT_s = *6.3 ms* provides the best dynamic performance among the other values.

On the other hand, since the PLL algorithm is basically used in the control loop of grid-connected power converters, therefore the sampling time of the PLL algorithm is commonly chosen equal to the switching period of the power devices. Considering a value of T_s = 100 µs, basically used for IGBT based power converters with a rated power of several *kW*, it becomes that the appropriate value of N_d is 63.

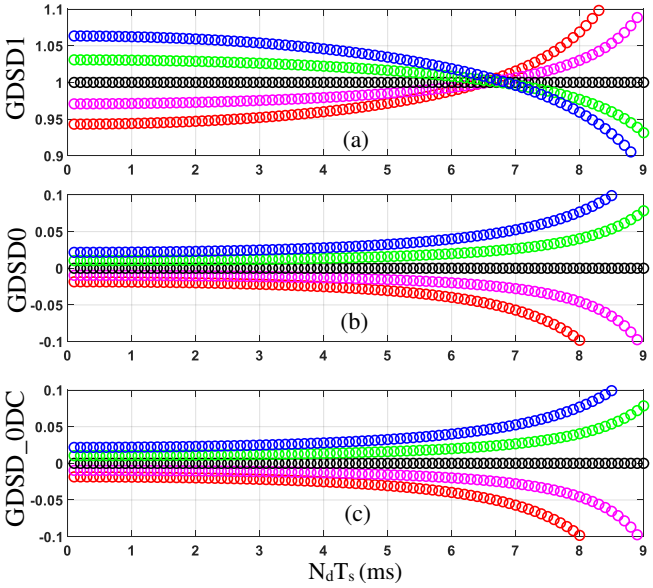

Fig. 4 : Variation of the DSD algorithm Gains versus N_dT_s for different values of Δf_{PLL} and a nominal grid frequency equal to 50 Hz. (red) Δf_{PLL}= -2 Hz, (magenta), Δf_{PLL} = -1 Hz, (black) Δf_{PLL} = 0 Hz, (green) Δf_{PLL} = +1Hz, and (blue) Δf_{PLL} = +2Hz.

B. Numerical simulation

A simulation test of the proposed DSD-TQT1-PLL is carried out with a highly disturbed grid voltage that includes DC-offsets, voltage unbalance and harmonic components. A frequency step change is also applied at the same time. The grid parameters in disturbed condition are listed in Table 1. The grid fault is enabled within the time interval [0.2s, 0.36s] as shown in Fig.5. The proportional gain of the DSD-TQT1-PLL (K_p) is equal to 79.5 and the gain of the conventional QT1-PLL is set to its optimal value (K_p = 50) as designed in [22]. The delay N_d in the DSD algorithm is set to 63.

Fig.6 shows the instantaneous amplitude of the FFPS extracted with the DSD-TQT1-PLL, the conventional QT1-PLL and the adaptive QT1-PLL, respectively. The results show that the performance of the DSD-TQT1-PLL and the adaptive QT1-PLL are stable and the extracted FFPS accurately matches its true value. As for the conventional QT1-PLL, it performs poorly, where the low-frequency ripple is not perfectly filtered. It is because of its vulnerability to the frequency deviation.

Table 1 Grid voltage parameters

Grid voltage parameters	Value
Amplitude and initial phase of FFPS	0.6 p.u*, π/3
Amplitude and initial phase of FFNS	0.2 p.u, π/6
Amplitude and initial phase of -5th harmonic	0.07 p.u,- π/12
Amplitude and initial phase of +7th harmonic	0.05 p.u,- π/20
Amplitude and initial phase of -11th harmonic	0.05 p.u,- π/24
Amplitude and initial phase of +13th harmonic	0.03 p.u, π/30
DC-offset in phases a,b and c	0.1, 0.05and -0.04 p.u
Frequency step change	+ 2 Hz

* p.u. values are computed with reference to the nominal grid voltage amplitude

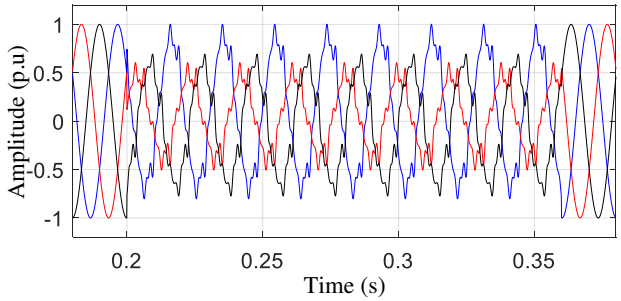

Fig. 5 Grid voltage waveforms considering the parameters of table 1.

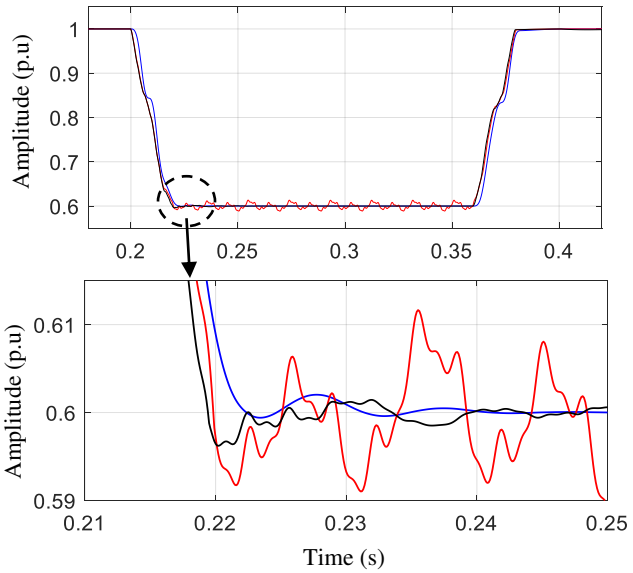

Fig. 6 Extraction of the FFPS instantaneous amplitude in p.u., (blue) proposed DSD-TQT1 (red) conventional (QT1) (black) adaptive QT1.

Moreover, in transient operation, the time needed by the DSD-TQT1-PLL to mitigate the ripple is lower than that of the adaptive QT1-PLL. Fig.7 and Fig.8 display the instantaneous amplitudes of the FFNS and the DC-offsets extracted by the DSD-TQT1-PLL. These waveforms converge precisely to their appropriate references though different DC-offsets are added to the three-phases of the grid voltage. The adaptability of the proposed DSD method to extract the FFPS, FFNS and the DC-offset components of the grid voltage is therefore proved.

Fig.9a illustrates the frequency error response obtained with the proposed DSD-TQT1-PLL and the conventional QT1-PLL [15], respectively. The frequency error curve of the DSD-TQT1-PLL reaches favorably the ±2% band within a 2% settling time about 39ms. As for the QT1-PLL, the ripple amplitude in steady state remains outside the ±2% band's limit, that is, ± 0.04Hz for a step change equal to 2Hz. This low-frequency ripple in steady-state is due to the frequency deviation from its nominal value that worsens the performance of the QT1-PLL. The DSD-TQT1-PLL has favorably mitigated this ripple owing to the use of the DSD algorithm that enables an efficient removal of the DC-offset and the FFNS. Besides, the removal of the DC-offset and FFNS allowed the use of in-loop TMAF filters with a reduced window width, which justifies the fast dynamic response of the DSD-TQT1-PLL. Notice also that the implemented TMAF filter is almost insensitive to the frequency variation in the waveforms of the remaining harmonics (5, 7, 11 and 13), which justifies the absence of any ripple caused by these characteristic harmonics. The superiority of the proposed technique to the conventional QT1-PLL is therefore, confirmed.

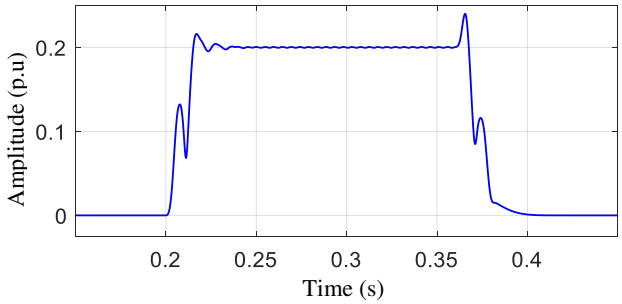

Fig. 7 Extraction of the FFNS amplitude in p.u. with the proposed DSD-TQT1.

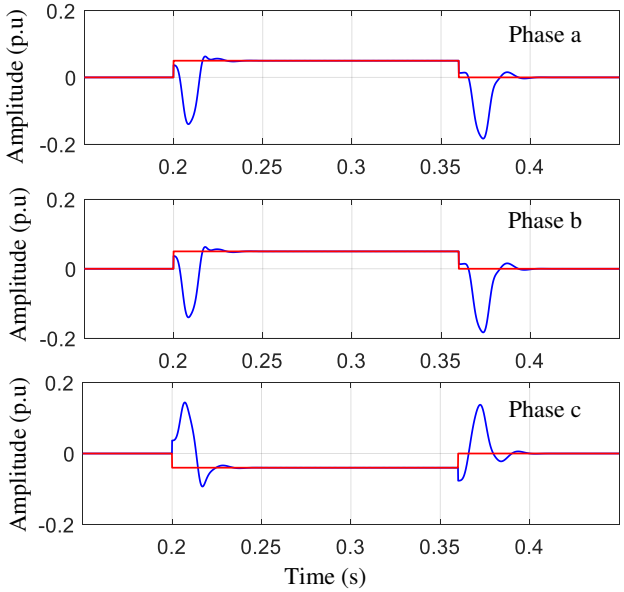

Fig. 8 Extraction of the amplitudes of the DC-offsets in p.u., (blue) extracted sequences by DSD-TQT1 (red) real DC-offsets as reported in table 1.

A second comparative study is carried out with the adaptive QT1-PLL. The results displayed in Fig.9b show that the 2% settling time of the adaptive QT1-PLL is obtained as 97.3ms. The same observations apply for the estimation of the instantaneous phase as displayed in Figs.10a-b.

To better evaluate the performance of the proposed DSD-TQT1-PLL in terms of harmonic distortion under frequency jump and DC-offset disturbances, we performed a harmonic analysis. For this purpose, we computed the cosine value of the estimated instantaneous phase and used the FFT tool to determine the main harmonic components. The same procedure is used with the QT1 and adaptive QT1-PLLs. The obtained harmonic spectra are depicted in Fig.11. It is clear that the proposed PLL shows the best mitigation capability of the dominant low-order harmonics, particularly sub- and inter-harmonics. Consequently, it provides the lower THD, which is equal to 0.07%.

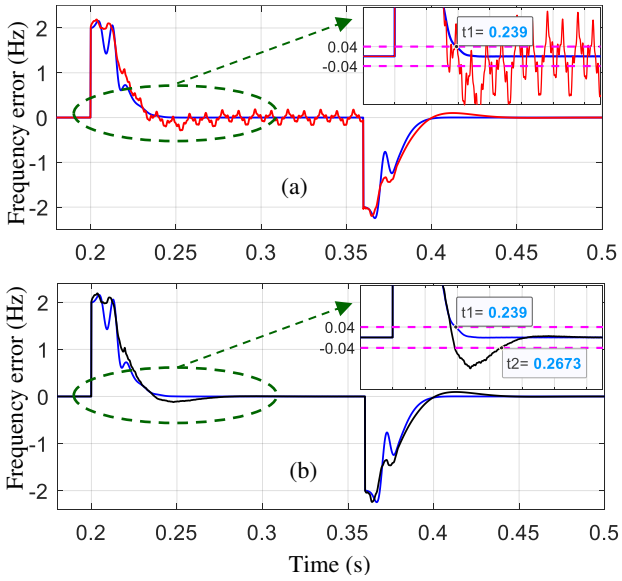

Fig. 9 Frequency error response in (Hz), (blue) proposed DSD-TQT1 (red) conventional (QT1) (black) adaptive QT1.

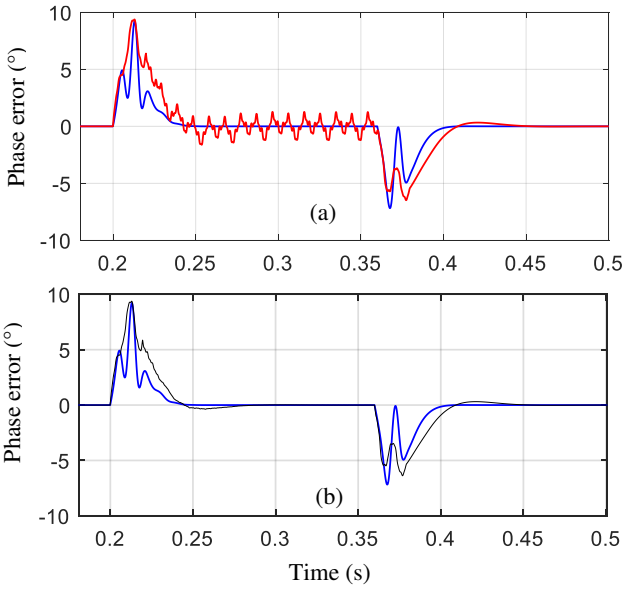

Fig. 10 Phase error response in (°) (blue) proposed DSD-TQT1 (red) conventional (QT1) (black) adaptive QT1.

Table 2 summarizes the performances obtained with the three PLLs (QT1, adaptive QT1 and DSD-TQT1). Besides the

fast dynamic response, the DSD-TQT1-PLL provides a ripple free response without using an adaptive in-loop filter. The high performance of the DSD-TQT1-PLL is, therefore, proved.

Table 2 Performance of the three simulated PLLs

	QT1-PLL	Adaptive QT1-PLL	DSD-TQT1-PLL
Use of adaptive in-loop filters	No	Yes	No
Steady state ripple	Yes	No	No
2% settling time	-----	67.3ms	39ms

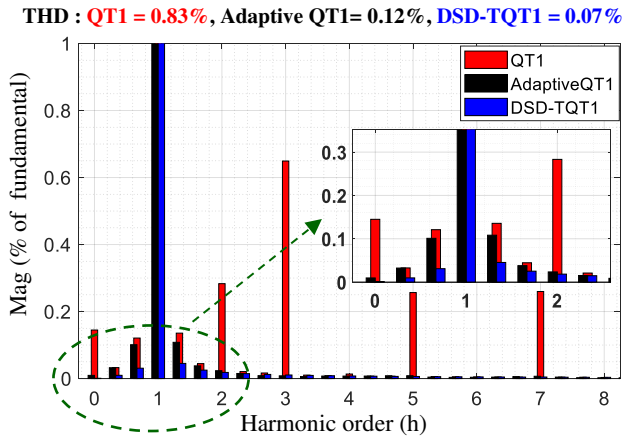

Fig. 11 Comparative THD Analysis (blue) proposed DSD-TQT1 (red) conventional (QT1) (black) adaptive QT1.

C. *OPAL-RT platform based experimental validation*

This section reports the experimental implementation study using the OPAL-RT OP5707XG real-time digital simulator. The experimental setup is shown in Fig.12.

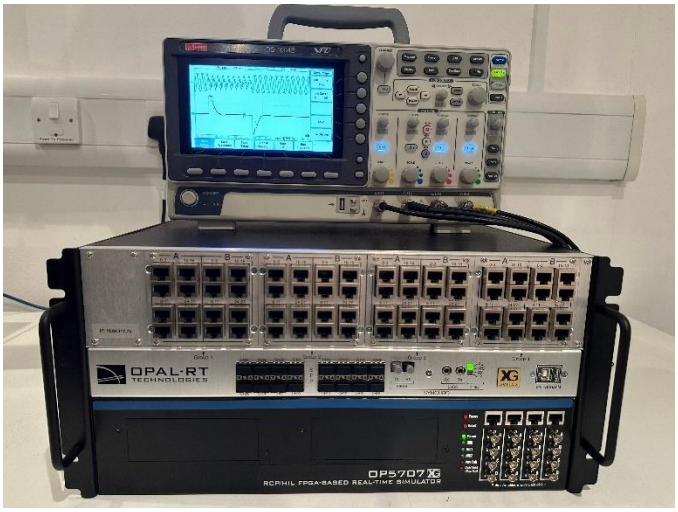

Fig. 12 Experimental setup for real-time implementation.

The proposed DSD-TQT1-PLL and the adaptive QT1-PLL are implemented in real-time on the OP5707XG simulator with a sampling frequency of 10 kHz. For the experimental implementation, we emulate based on MATLAB Simulink the same grid conditions specified in the simulation section for $v_\alpha(t)$ and $v_\beta(t)$. The emulated digital grid voltage signals are converted into analog (physical) signals through the OP5330-3 digital to analog converter module. The physicals signals are then sampled through OP5342 analog to digital converter module for loop back study. Experimental results are plotted in the RS-Pro IDS-1054B digital storage oscilloscope.

Fig.13 displays the real-time waveforms of the grid voltage α-β components and frequency errors obtained with the adaptive QT1-PLL and DSD-TQT1-PLL, respectively. As can be seen, the experimental results are quite consistent with the simulation findings, where the proposed PLL outperforms the adaptive QT1-PLL in terms of dynamic performance and exhibits similar behavior in steady state, making it a more effective solution. Fig.14 displays the real-time waveforms of estimated instantaneous phase. The results show that the proposed PLL remains stable, which confirms the appropriate operation of the DSD extraction method over a large time interval of the grid disturbance.

In summary, the experimental results and real-time waveforms provide compelling evidence of the superiority and effectiveness of the proposed PLL. It not only outperforms the adaptive QT1-PLL in terms of dynamic performance, but also demonstrates similar behavior in steady state and precise phase estimation. As a result, the proposed PLL presents a highly promising option for grid-connected converter control and other related applications.

Grid voltage 1v/div and frequency 1 Hz/div, 50 ms/div

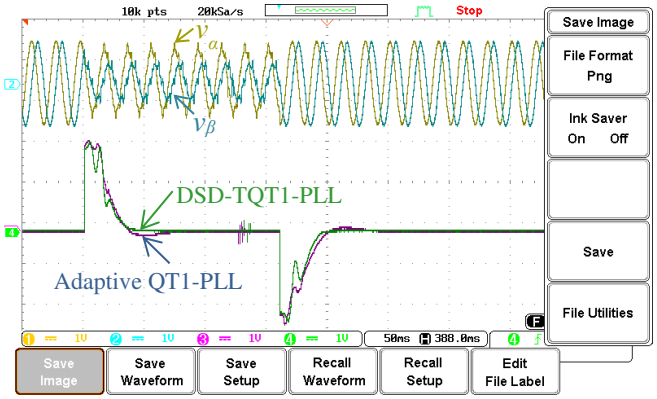

Fig. 13 Real-time waveform of $v_\alpha(t)$, $v_\beta(t)$ and the frequency error response in (Hz).

Grid voltage 1v/div and phase 180 °/div, 50 ms/div

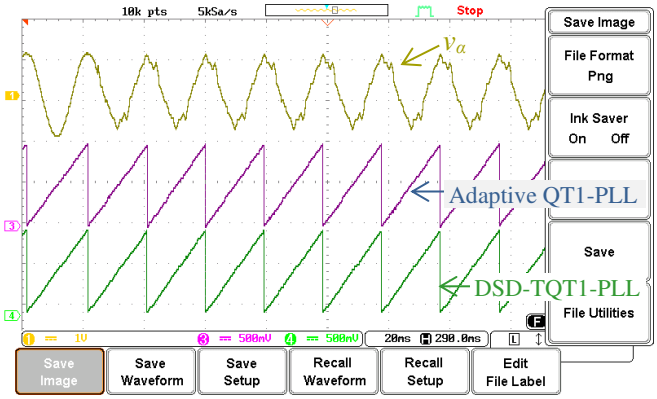

Fig. 14 Real-time waveform of $v_\alpha(t)$ and the phase response in (°).

V. Conclusion

This paper presented the design and implementation of a novel DSD-TQT1-PLL achieved by integrating the DSD algorithm into the TQT1-PLL. The DSD algorithm acts as a preprocessing block for various FFPS extraction techniques, making it easy to integrate into any PLL and thereby enhancing its performance by effectively eliminating the FFNS and DC-offset. The proposed DSD-TQT1-PLL demonstrates high performance in achieving accurate and rapid synchronization with the grid voltage even in presence of the FFNS, DC-offset, the characteristic harmonics, and a frequency variation.

The comparative analysis demonstrated the superiority of the proposed DSD-TQT1-PLL over both conventional and adaptive QT1-PLL algorithms, particularly under highly disturbed grid voltage conditions. Remarkably, these achievements have been attained without the need for any frequency adaptive algorithms and time consuming extra computationally intensive trigonometric functions, making the proposed PLL a more straightforward solution and easily implementable on real-time digital platforms. The successful real-time implementation of the DSD algorithm empowers the proposed PLL with the ability to operate effectively in distributed power generation systems and active filters connected to a weak grid. This is of paramount importance in modern energy landscapes, where non-polluting renewable energy sources and distributed generation play a crucial role.

VI. References

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