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Differential Power Processing Based Control Framework for Multiple Battery Energy Storage Systems in DC Microgrids

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***Abstract*—Multiple battery energy storage systems (BESSs) have been widely used in the DC microgrids to balance generation and demand. To achieve this, the BESS converters need to deliver the full required input/output power imposed on BESSs under the conventional BESS-DC bus configuration, which often demands high power ratings for the converters, hence leads to high installation cost as well as high power losses. To reduce the power ratings for BESS converters while delivering the same power from BESSs, this paper proposes a new differential power processing (DPP) based control framework where the DPP techniques and BESSs are firstly combined without losing the following control objectives, namely, the accurate current-sharing and state of charge (SoC) balance of BESSs as well as DC bus voltage regulation. This is achieved first by introducing inverted bidirectional buck converters to function as a front-end converter and DPP converters. Then, a virtual state variable combining BESS output current and its SoC is proposed, based on which a consensus control strategy is proposed. The stability of the proposed DPP-based control framework is also analyzed. Finally, the real-time hardware-in-loop (HIL) tests confirm the effectiveness of the proposed control framework, showing that the proposed DPP-based control framework reduces the power ratings of the converters to less than 20 $\%$ of BESS converters used in conventional BESS-DC bus configuration even in the worst operating scenario, while delivering the same required power from BESSs, paving a way for an innovative BESS DC microgrid design with much down-sized converters for BESSs.**

***Index Terms*—Differential power processing, Multiple BESSs, DC microgrids, Consensus Control, SoC balancing.**

I. Introduction

WORLDWIDE commitments to reduce both carbon and pollutant emissions from burning fossil fuels have led to the rapid development of power generation technologies from renewable energy sources (RESs) [1], [2]. The battery energy storage systems (BESSs) are often introduced into the DC microgrids to balance the power generation from RESs and the loads [3]. The control objectives usually include accurate current-sharing and state-of-charge (SoC) balance among different BESSs together with DC bus voltage regulation [4].

In the conventional BESS-DC bus configuration as illustrated in Fig.1, the BESSs are connected to the DC bus through BESS converters. They are controlled by different control strategies, which enable the power flow adjustment between BESSs and DC bus to achieve the aforementioned control objectives. For example, the droop control is the most widely used control strategy for BESS converters, it works in the decentralized way and only the local information is used [5]–[8]. Lu et al proposed a droop control where the droop coefficient is proportional to the n-th order of SoC in the charging process, while it is inversely proportional to the n-th order of SoC in the discharging process [5], [6]. Lin et al proposed an integral droop control for transient power allocation of hybrid energy storage systems in the DC microgrids [7]. An adaptive droop control for distributed BESSs in the DC microgrids is proposed, the battery state and model parameters are estimated simultaneously online by dual extended Kalman filter algorithm [8]. Distributed secondary control strategies are also proposed for BESS converters [9]–[13], where Lu et al developed a distributed secondary control, which uses local controllers and the low-bandwidth communication network to exchange information between converters. Average voltage and current controllers are used for each converter to simultaneously enhance the current-sharing accuracy and restore the average DC bus voltage [9]. Zeng et al proposed a distributed secondary control strategy for BESSs in the DC shipboard microgrid, where the consensus algorithm is introduced and only the neighbour-to-neighbour information is necessary [10], [11]. A distributed cooperative control for multiple DC electric springs is proposed in [12], where the average DC-bus voltage regulation and SoC balance are achieved. A novel distributed multiagent finite-time control strategy with time delays for the SoC balance and average voltage restoration is proposed for multiple BESSs in the DC microgrids, where a feedback linearisation technique is used to obtain a second-order consensus strategy for SoC [13]. Besides the droop control and secondary control, DC-bus-signaling-based control strategies are proposed, where the BESSs are selected as master units and coordinate slave units like RESs and loads by adjusting the DC bus voltage [14], [15].

In the conventional BESS-DC bus configuration, the BESS converters adopting the aforementioned control strategies have to deliver the full required input/output power imposed on the BESSs, which is referred as full power processing (FPP). Considering full power is delivered by the converter for each BESS, the power flow through the converters will inevitably lead to a high power loss, let alone the full power rating is required for the BESS converters, leading to high converter installation costs [16]. The concept of differential power processing (DPP) was introduced in [17] for PV systems, unlike the FPP techniques, only the power differences between PV and adjacent PVs/DC bus are processed by the DPP techniques. The inverted buck converters, flyback and single-ended primary-inductor converter (SEPIC) converters are usually introduced to function as DPP converters [18].

The DPP techniques developed so far for the PV system

can be grouped into two categories, namely, the series DPP techniques and the parallel DPP techniques [18], [19]. The PV elements are series connected in the series DPP techniques and the DPP converters are supposed to provide the power differences between adjacent PV elements. Shimizu et al proposed a novel circuit which enables maximum power to be obtained from all of the PV modules even if some of the modules are prevented from receiving light [20]. Series PV string architectures with the DPP converters are proposed, which extracts the maximum power from PV systems by using distributed MPPT method [21], [22]. Shenoy et al introduced an energy conversion approach that enables PV work at MPPT while only processing a small fraction of the total power produced. The overall efficiency is increased and the challenges associated with unmatched maximum power points are addressed [23]. Kim et al detailed the computational methods to determine the operation of PV-to-bus and PV-to-PV DPP architectures with rating-limited converters [24]. Uno et al introduced two series DPP architectures, they are two-switch voltage equalizer using an LLC resonant inverter with voltage multiplier [25] and single-switch SEPIC-based voltage equalizer, respectively [26]. In [27], the segmented DPP structure is introduced as a modular approach that utilizes the bidirectional DPP flyback converters to maximize PV power generation while minimizing converter power loss. In parallel DPP techniques, the PV elements are parallel connected and the voltage differences between PV elements and DC bus is processed. Zhou et al used the flyback converters as the DPP converters [28], the input of which is connected to the DC bus directly. While the front-end converter is introduced as the input of DPP converters in the [29], the former steps down the DC bus voltage to an intermediate level. Liu et al proposed a PV-to-PV method for the modular DPP, which permits PV panels to be added to or removed from either series strings or paralleled connections [30].

In summary, BESS converters have to deliver the full required power imposed on the BESS in the conventional BESS-DC bus configuration, which inevitably imposes high specifications on the power ratings of converters, the installation cost and power losses are consequently high. Inspired by the parallel DPP techniques for the PV systems, a DPP-based control framework for BESSs in DC microgrids is proposed, where the DPP techniques and BESSs are firstly combined without losing the following control objectives, namely, the accurate current-sharing and SoC balance of BESSs as well as DC bus voltage regulation. The main contributions of this paper are summarized below

1) Different from the PV systems, inverted bidirectional buck converters are introduced as the front-end and DPP converters to allow bidirectional power flow from BESSs, the power ratings of the converters in the proposed DPP-based control framework are significantly reduced compared with BESS converters used in the conventional BESS-DC bus configuration.

2) A virtual state variable combining the BESS output current and its SoC is proposed, based on which a consensus based control strategy is proposed. All the key control objectives, i.e., accurate current-sharing, SoC balance, and DC bus voltage regulation are achieved.

3) Considering the DC bus voltage is regulated by the BESSs, the stability of the proposed DPP-based control framework is analyzed.

The remainder of this paper is organized as follows. Section II presents the conventional BESS-DC bus configuration and battery cell model. The proposed DPP-based control framework is demonstrated in Section III while its stability analysis is presented in Section IV. The hardware-in-loop (HIL) test results of the proposed control framework are given in Section V. Section II presents the comparison between the proposed control framework and conventional configuration. Finally, Section VII concludes the paper.

II. Preliminaries

A. Conventional BESS-DC bus configuration

The conventional BESS-DC bus configuration is illustrated in Fig.1, where n BESSs are parallel connected to the DC bus through their respective bidirectional BESS converters. Besides, the PV panel is connected to the DC bus through a boost converter while the load modeled by a resistor is connected to DC bus directly.

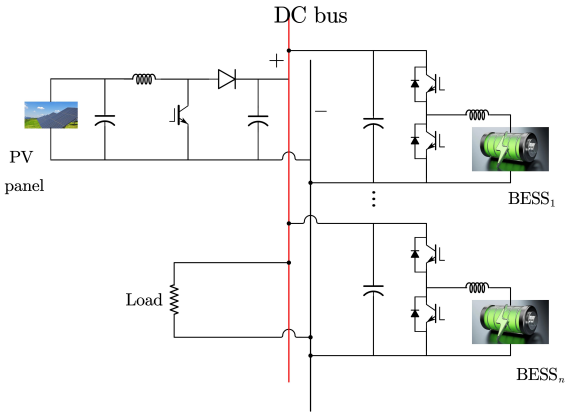

Fig. 1. Conventional BESS-DC bus configuration

B. Battery Cell Model

To model the output characteristics of BESSs, different kinds of battery cell models have been proposed like the electrochemical model, the electric circuit model and the neural networks model [31], [32]. The first-order electric circuit model illustrated in the Fig.2 (a) is one of the most widely used battery cell models, where ocv and r_0 are the open circuit voltage and internal resistance of the battery cell, respectively, while r_1c_1 network is used to capture the battery relax process. v_b and i_b represent the output voltage and current of the battery cell, respectively.

Based on the electric circuit in the Fig.2 (a), v_b is expressed by

$$v_b = \text{ocv} - i_b r_0 - i_b r_1 \left(1 - e^{\frac{-t}{r_1 c_1}}\right) \tag{1}$$

The ocv changes with SoC of battery cell, and the latter is usually updated with the Coulomb Counting method

$$\text{SoC} = \text{SoC}_{init} - \frac{1}{3600 c_b} \int i_b dt \tag{2}$$

where SoC_{init} and c_b are the initial SoC and capacity of battery cell, respectively.

For different kinds of batteries, an approximate linear relationship exists between SoC and ocv, although it is not exactly same for all types of batteries. A typical LiFeO_4 battery cell is used for demonstration in this paper. Based on our experimental results, the ocv at different SoC is illustrated in Fig.2 (b) [33]. It can be observed that ocv increases as battery SoC increases.

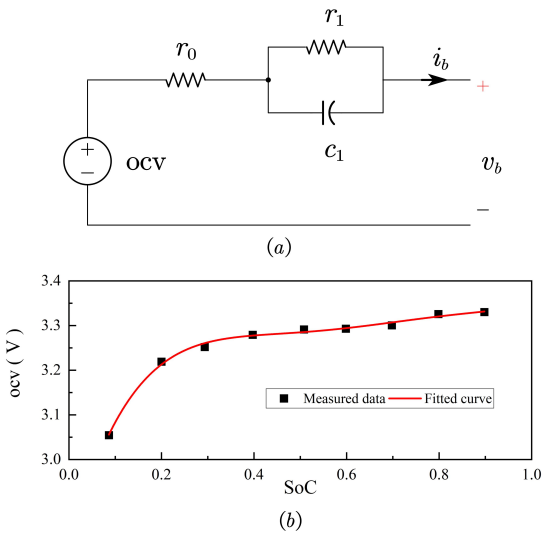

Fig. 2. Battery model (a) Equivalent circuit model (b) ocv versus SoC of LiFeO_4 battery

The relationship between ocv and SoC can be modeled by the m-order polynomial function based on the experimental data, it is expressed by

$$\mathrm{ocv} = \alpha_m \mathrm{SoC}^m + \alpha_{m-1}\mathrm{SoC}^{m-1} + \cdots + \alpha_1 \mathrm{SoC} + \alpha_0 \quad (3)$$

where $a_m, ..., a_0$ is the constant value obtained from curve fitting. With Eq (1) and (3), the relationship between v_b and i_b can be obtained. The BESS usually consists of $N_p \times N_s$ identical battery cells, where the N_p is the number of parallel connected battery cell strings and N_s is the number of battery cells in each battery string. Therefore, the output voltage of BESSs (V_b) is expressed by

$$V_b = \mathrm{OCV} - IR_0 - IR_1\left(1 - e^{\frac{-t}{R_1 C_1}}\right) \quad (4)$$

where I is the BESS output current, $\mathrm{OCV} = N_s\mathrm{ocv}$ is the open circuit voltage of BESS and $R_0 = N_s/N_p r_0$ is the internal resistance of BESS, $R_1 = N_s/N_p r_1$ and $C_1 = N_p/N_s c_1$ are used to capture the BESS relax process. The SoC of the BESS can be updated by

$$\mathrm{SoC} = \mathrm{SoC}_{init} - \frac{1}{3600 C_b}\int I dt \quad (5)$$

where C_b is the capacity of the BESS. The parameters of the battery cell used in this paper are given in the Table I.

TABLE I
PARAMETERS OF BATTERY CELL

r_0	r_1	c_1	N_s	N_p	c_b
0.016 Ω	0.0177 Ω	470 F	260	10	5Ah
α_4	α_3	α_2	α_1	α_0	SoC range
-2.436	6.093	-5.353	2.021	3.001	0.2-0.8

III. The Proposed DPP-based Control Framework

A. The DPP Techniques for BESSs

In the conventional BESS-DC bus configuration like Fig.1, the power interaction between BESSs and the DC microgrids is controlled by the bidirectional BESS converters, however, the full BESS power is processed by the BESS converters, which inevitably imposes high requirements on the power ratings of the converters. Considering the power losses and installation cost of the converters are proportional to the power flow goes through them, the conventional BESS-DC bus configuration will inevitably cause high power losses and installation cost.

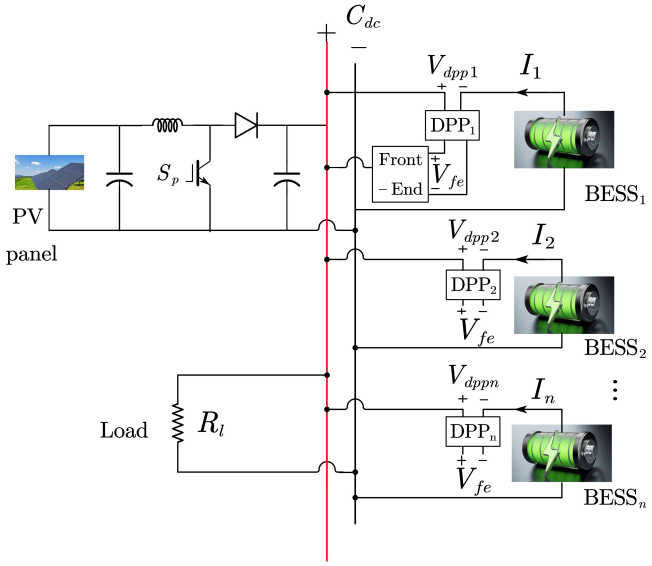

Fig. 3. The configuration of the DC microgrid in the proposed DPP-based control framework

Inspired by the parallel DPP techniques for PV systems, a new DPP-based control framework is proposed in this paper to address the aforementioned issues. As illustrated in the Fig.3, the DPP converters are introduced between the BESSs and DC bus, they enable the power flow adjustment between the BESSs and DC bus by controlling their output voltage V_{dpp}. To step down the the DC bus voltage to an intermediate voltage level for the input power supply of DPP converters, a front-end converter is introduced. The input of the front-end converter is connected to the DC bus while its output terminal is connected to **all DPP converters**, each of which is connected to a BESS, where C_{dc} is the capacitance of DC bus, R_l is the load resistance, and V_{fe} denotes the output voltage of the front-end converter. L_p, C_p, S_p denote the inductor, capacitor, and switch of PV converter, respectively.

B. Inverted Bidirectional Buck Converters for DPP Implementation

Different converters are selected to function as the DPP converters in the PV systems, like the flyback and SEPIC converters [18], [26], [28]. Besides, the inverted buck converters (also being named flipped buck converters) are used and they require less components than flyback and SEPIC converters [28], [29]. The reason using inverted buck converters rather than conventional buck converters is that the output of all DPP converters should be connected with the common DC bus, the positive output of PV systems would be grounded when using conventional buck converters [28]. The DPP techniques with PV systems are well researched, however, combing DPP techniques with BESSs while developing control strategies for SoC balance and DC bus voltage regulation has not been studied.

Considering the aforementioned advantages of inverted buck converters, they are introduced as the front-end converter and DPP converters in this study as illustrated in the Fig.4. The principle of front-end converter and DPP converters in the proposed control framework will be presented in the following, the readers also can refer DPP techniques in PV systems for better understanding.

Unlike the PV panels that only provides unidirectional power support to the DC bus, two switches are used in the front-end and i-th DPP converter for bidirectional power flow regulation between BESS_i and DC bus, where S_{d1} and S_{d2} denote two switches for all DPP converters, S_{f1} and S_{f2} are switches for the front-end converter, L_d and C_d denote the inductor and the capacitor in all DPP converters, respectively. L_f and C_f are the inductor and the capacitor in the front-end converter, respectively. V_{dppi} and I_{dppi} are the voltage and current of the i-th DPP converter, respectively. $I_{fe,\alpha}$ $I_{fe,\beta}$ are current of the front-end converter at the DC bus side and C_f side, V_{dc} is the DC bus voltage.

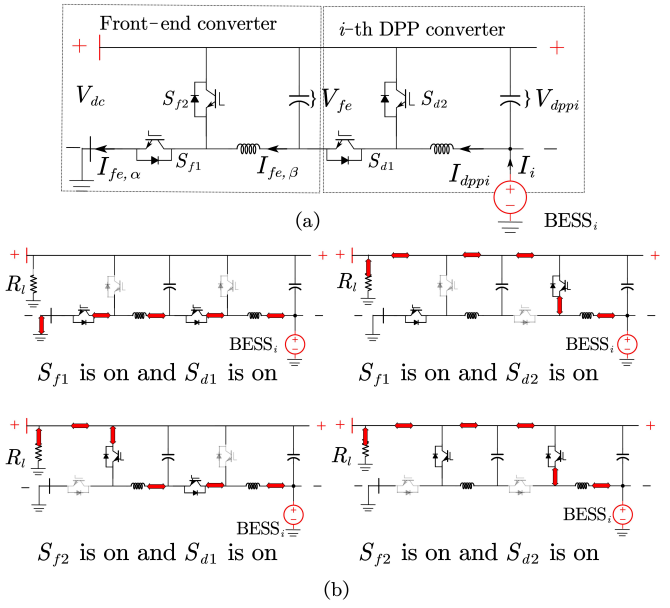

Fig. 4. Inverted bidirectional buck converters (a) topology (b) power flow analysis

Fig.4 (b) illustrates the power flow between the BESS_i and DC bus when the front-end and the i-th DPP converter work at different operating modes. They are detailed as below:

S_{f1} and S_{d1} are on: $\mathrm{BESS}_i \leftrightarrow L_d \leftrightarrow S_{d1} \leftrightarrow L_f \leftrightarrow S_{f1} \leftrightarrow$ ground.

S_{f1} and S_{d2} are on /S_{f2} and S_{d2} are on: $\mathrm{BESS}_i \leftrightarrow L_d \leftrightarrow S_{d2} \leftrightarrow$ DC bus $\leftrightarrow$ load.

S_{f2} and S_{d1} are on: $\mathrm{BESS}_i \leftrightarrow L_d \leftrightarrow S_{d1} \leftrightarrow L_f \leftrightarrow S_{f2} \leftrightarrow$ DC bus $\leftrightarrow$ load.

In summary, the bidirectional power flow between BESS_i and DC bus are allowed with the proposed control framework. BESS_i works in the discharging mode when there is a power deficit on the DC bus, part of the BESS_i power is injected to the DC bus through i-th DPP converter directly, and the left power is either injected to the DC bus through the front-end converter or flow back to BESS_i from the ground. The only difference between BESS working in charging mode and discharging mode is the power flow direction.

When the system operates in the steady state, the voltage on the capacitor and current on the inductor are at a stable value. It is easy to infer that

$$I_i = I_{dppi} \tag{6a}$$

$$I_{fe,\alpha} = \sum_{i=1}^{n} I_i - \frac{V_{dc}}{R_l} + I_{pv} \tag{6b}$$

where I_{pv} is the output current from PV array.

With Eq (6), the power of i-th DPP converter, i-th BESS, and the front-end converter can be calculated by

$$P_{dppi} = V_{dppi} I_i \tag{7a}$$

$$P_{bi} = V_{bi} I_i \tag{7b}$$

$$P_{fe} = V_{dc} I_{fe,\alpha} \tag{7c}$$

Since V_{dppi} is designed much smaller than V_{bi}, the power rating of i-th DPP converter will be highly reduced compared with BESS converter in the conventional BESS-DC bus configuration. The power ratings for different converters will be discussed in Section V.

C. The Proposed Control Strategy

In the proposed DPP-based control framework, the front-end converter is used to step down the DC bus voltage to an intermediate voltage level, thus, the control algorithm for the front-end converter is straightforward. As illustrated in Fig. 5 (a), the dual voltage and current loop is used to track the reference of the front-end converter output voltage V_{fe}^*, and pulse width modulation (PWM) is generated to drive switches of converters.

For the control of DPP converters, their output voltage should be adjusted to achieve the following control objectives, i.e., accurate current-sharing and SoC balance among BESSs, and DC bus voltage restoration.

$$\lim_{t\to\infty} (I_i/C_{bi} - I_j/C_{bj}) = 0 \ \forall i, j \tag{8a}$$

$$\lim_{t\to\infty} (\mathrm{SoC}_i - \mathrm{SoC}_j) = 0 \ \forall i, j \tag{8b}$$

$$\lim_{t\to\infty} V_{dc} - V_{dc}^{*} = 0 \tag{8c}$$

where V_{dc}^{*} is the reference of DC bus voltage. To achieve accurate current-sharing and SoC balance between different BESSs, a virtual state variable ρ_i combing i-th BESS output current and SoC information is proposed, which is expressed as

$$\rho_i = I_i/C_{bi} - k\mathrm{SoC}_i \tag{9}$$

where k is an index for SoC balance speed regulation.

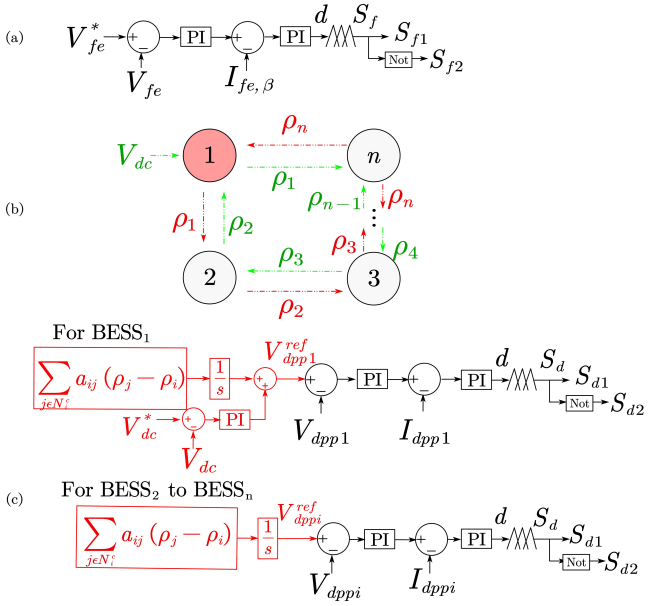

Fig. 5. The proposed control strategy (a) the front-end converter control algorithm (b) communication links (c) i-th DPP converter control algorithm

Further, the communication links illustrated in Fig. 5 (b) are introduced in the controller design. In the communication network, BESS_1 to BESS_n are modeled as node 1 to n, each node only communicates with its neighbours. The connections between node 1 to n can be represented by an adjacency matrix $\boldsymbol{a} = [a_{ij}] \in R^{n\times n}$, where the communication weights are given by:

$$a_{ij} = \begin{cases} a & \text{if } j \in \mathrm{N}_i^c \\ 0 & \text{otherwise} \end{cases} \tag{10}$$

N_i^c denotes the set of nodes that have communication links with i-th node. a is a constant value. The incoming cyber information matrix can be denoted by $\boldsymbol{Z_{in}} = \mathrm{diag}\{z_i\}$, $z_i = \sum_{j\epsilon \mathrm{N}_i^c} a_{ij}$, In this paper, all communication links are bidirectional and the Laplacian matrix $\boldsymbol{L} = \boldsymbol{Z_{in}} - \boldsymbol{a}$ is defined. Further, in this paper, we assume that the all the nodes in the communication links are accessible, the associated graph has a spanning tree.

Based on the communication links, the consensus protocol is used in the controller design, where BESS_i compares its local ρ_i and neighbours' ρ_j, and the leader node also collects V_{dc}, then the reference of i-th DPP converter output voltage V_{dppi}^{ref} is adjusted according to

$$V_{dppi}^{ref} = \frac{1}{s}\sum_{j\epsilon \mathrm{N}_i^c} a_{ij}(\rho_j - \rho_i) + g_i\left(V_{dc}^{*} - V_{dc}\right)\left(k_p + k_i/s\right) \tag{11}$$

where g_i is the index for the leader node, $g_i = 1$ if i is selected as the leader node, otherwise $g_i = 0$. k_p and k_i are proportional gain and integral gain for DC bus voltage regulation, respectively. In this paper, node 1 is the leader node. Similar with the front-end converter control, the dual voltage and current loop is introduced to track V_{dppi}^{ref} in the i-th DPP controller.

As demonstrated in Eq (11), the difference between virtual state variables is sent to an integrator and the voltage deviation between the DC bus and its reference value is sent to a PI controller, therefore, the DC bus voltage can be restored to V_{dc}^{*} and all virtual state variables will converge to the same value. It is easy to obtain Eq (12) when all virtual state variables are at the same value.

$$\rho_i = \rho_j \rightarrow I_i/C_{bi} - I_j/C_{bj} = k \triangle \mathrm{SoC}_{ij} \quad \forall i,j \tag{12}$$

where $\triangle\mathrm{SoC}_{ij} = \mathrm{SoC}_i - \mathrm{SoC}_j$. Combing Eq (5) and Eq (12), it yields

$$\frac{d\mathrm{SoC}_j}{dt} - \frac{d\mathrm{SoC}_i}{dt} = 3600k \triangle \mathrm{SoC}_{ij} \tag{13}$$

Eq (13) shows SoC will be gradually balanced with the proposed control strategy no matter in BESS charging or discharging.

1) If BESS_i and BESS_j are discharging and $\mathrm{SoC}_i > \mathrm{SoC}_j$, $\frac{d\mathrm{SoC}}{dt} < 0$ and $|\frac{d\mathrm{SoC}_i}{dt}| > |\frac{d\mathrm{SoC}_j}{dt}|$, which indicates that SoC decrease speed of BESS_i is quicker than BESS_j, thus BESS_i and BESS_j will be gradually balanced.

2) If BESS_i and BESS_j are charging and $\mathrm{SoC}_i > \mathrm{SoC}_j$, $\frac{d\mathrm{SoC}}{dt} > 0$ and $|\frac{d\mathrm{SoC}_i}{dt}| < |\frac{d\mathrm{SoC}_j}{dt}|$, which indicates that SoC increase speed of BESS_i is lower than BESS_j, thus BESS_i and BESS_j will be gradually balanced.

3) If one BESS is charging and the other one is discharging, SoC balance will be achieved.

After SoCs are balanced, $\rho_i = \rho_j \rightarrow I_i/C_{bi} = I_j/C_{bj}\ \forall i,j$, the proposed controller works as current controller and voltage regulation controller, the accurate current-sharing among BESSs can be achieved.

D. Practical Implementation

In the proposed DPP-based control framework, the inverted bidirectional buck converters are introduced as DPP converters, it is worth noting that their output voltages can not be negative values. Therefore, the two following aspects should be considered in designing V_{dc}^{*} and V_{bi}. Firstly, V_{dc}^{*} should be designed higher than the maximum output voltage of any BESS to make sure the DPP converters work properly. V_{bi} reaches its maximum value V_{bi}^{max} when BESS_i is at its highest SoC value and charged with maximum current I_i^{max}

$$V_{bi}^{max} = \mathrm{OCV}_i\left(\mathrm{SoC}_i = 0.8\right) + I_i^{max}R_0 + I_i^{max}R_1\left(1 - e^{\frac{-t}{R_1C_1}}\right) \tag{14}$$

Considering the SoC operation range is usually between 0.2 to 0.8 for the microgrid application, the highest SoC is 0.8 in this paper.

Secondly, V_{dc}^{*} should not be designed too much higher than the minimum output voltage of any BESS. The power of the i-th DPP converter is $P_{dppi} = V_{dppi} I_{dppi} = (V_{dc} - V_{bi})\, I_{dppi}$, it has the largest value when $V_{bi} = V_{bi}^{min}$. If V_{dc}^{*} is much higher than V_{bi}^{min}, it will put a high power rating requirement on i-th DPP converter. Similarly, V_{bi} reaches its minimum value when BESS_i is at the lowest SoC value and discharged with maximum current I_i^{max}

$$V_{bi}^{min} = \mathrm{OCV}_i\left(\mathrm{SoC}_i = 0.2\right) - I_i^{max} R_0 - I_i^{max} R_1 \left(1 - e^{\frac{-t}{R_1 C_1}}\right) \tag{15}$$

IV. Stability Analysis

The stability analysis is conducted to verify the proposed DPP-based control framework. In the BESS model, the R_1C_1 network is used to represent the long time relax process, and the voltage on the R_1C_1 network changes slowly due to the large C_1, hence, it is neglected in the following analysis. Based on Kirchhoff's voltage law (KVL), I_i can be expressed as

$$I_i = \frac{\mathrm{OCV}_i + V_{dppi} - V_{dc}}{R_{0i}} \tag{16}$$

The DC bus is modeled as a large capacitor, assuming the responses of the front-end and DPP converters are fast enough, the output power of the BESSs can be delivered to DC bus immediately, the response of DC bus voltage is expressed by

$$C_{dc}\dot{V_{dc}} = \sum_{i=1}^{n} (\mathrm{OCV}_i - I_i R_{0i}) I_i / V_{dc} - \frac{V_{dc}}{R_l} + I_{pv} \tag{17}$$

where $\dot{x}$ represents the derivative of state variable x. Linearzing Eq (16) and Eq (17) at equilibrium point, it yields

$$\Delta I_i = \frac{\Delta V_{dppi} - \Delta V_{dc}}{R_{0i}} \tag{18a}$$

$$C_{dc}\Delta\dot{V_{dc}} = \frac{-\bar{I_i}\sum_{i=1}^{n}\mathrm{OCV}_i \Delta V_{dc}}{\bar{V_{dc}}^{2}} + \frac{\sum_{i=1}^{n}(\mathrm{OCV}_i \Delta I_i)}{\bar{V_{dc}}} - \frac{\Delta V_{dc}}{R_l} \tag{18b}$$

where Δx and $\bar{x}$ represent small perturbations and equilibrium points of state variable x, respectively. Note the voltage drop on the R_0 is also neglected when linearzing Eq (17) for similicity.

The state variable vector $\Delta\boldsymbol{\varphi} = \left[\Delta \boldsymbol{V_{dpp}}^{\mathrm{T}}, \Delta\boldsymbol{\rho}^{\mathrm{T}}, \Delta V_{dc}\right]^{\mathrm{T}}$ is selected for stability analysis, where $\Delta \boldsymbol{V_{dpp}} = [\Delta V_{dpp1}, \Delta V_{dpp2}, \cdots \Delta V_{dppn}]^{\mathrm{T}}$, $\Delta\boldsymbol{\rho} = [\Delta\rho_1, \Delta\rho_2, \cdots, \Delta\rho_n]^{\mathrm{T}}$. The other state variables can be expressed by $\Delta\boldsymbol{\varphi}$, for example, the BESS output current vector $\Delta\boldsymbol{I} = [\Delta I_1, \Delta I_2, \cdots \Delta I_n]^{\mathrm{T}}$ can be expressed by

$$\Delta\boldsymbol{I} = [\mathbf{A}_1, \mathbf{0}_{n\times n}, \mathbf{A}_2]\, \Delta\boldsymbol{\varphi} \tag{19}$$

where $\mathbf{A}_1 = \mathrm{diag}\,(1/R_{01}, 1/R_{02}, \cdots, 1/R_{0n})$, and $\mathbf{A}_2 = [-1/R_{01}, -1/R_{02}, \cdots, -1/R_{0n}]^{\mathrm{T}}$. $\mathbf{0}_{\boldsymbol{n}\times\boldsymbol{n}}$ is $n\times n$ matrix with all elements equal to 0.

It is worth noting that the bandwidth of dual voltage and current loop is usually much higher than outer loop for effective reference voltage tracking, it is reasonable to assume dual voltage and current loop equal to '1', i.e., $V_{dppi}^{ref} = V_{dppi}$ [34]. Combing the DPP control algorithm defined by Eq (11) and Eq (18b), it yields

$$\Delta\dot{\boldsymbol{\varphi}}_1 = \mathbf{A}_3 \Delta\boldsymbol{\varphi} \tag{20a}$$

$$\Delta\dot{\boldsymbol{I}} = [\mathbf{A}_1, \mathbf{A}_2]\, \Delta\dot{\boldsymbol{\varphi}}_1 \tag{20b}$$

where $\Delta\boldsymbol{\varphi}_1 = \left[\Delta \boldsymbol{V_{dpp}}^{\mathrm{T}}, \Delta V_{dc}\right]^{\mathrm{T}}$,

$$\mathbf{A}_3 = \left[\begin{array}{ccc} k_p\mathbf{A}_4 & -\boldsymbol{L} & -k_i - k_p l \\ \mathbf{0}_{(\boldsymbol{n}-1)\times\boldsymbol{n}} & & \mathbf{0}_{\boldsymbol{n}-1} \\ \hline \mathbf{A}_4 & \mathbf{0}_n^{\mathrm{T}} & l \end{array}\right]$$

$$\mathbf{A}_4 = \left[\mathrm{OCV}_1 / \left(\bar{V_{dc}} R_{01} C_{dc}\right), \cdots, \mathrm{OCV}_n / \left(\bar{V_{dc}} R_{0n} C_{dc}\right)\right]$$

$$l = -1/\left(C_{dc} R_l\right) - \frac{1}{C_{dc}}\left(\sum_{i=1}^{n} \mathrm{OCV}_i \bar{I_i} / \bar{V_{dc}}^{2} + \sum_{i=1}^{n} \frac{\mathrm{OCV}_i}{R_{0i}} / \bar{V_{dc}}\right)$$

$\mathbf{0}_{\boldsymbol{n}}$ is n-th order vector with all elements equal to 0.

Combing Eq (5) and Eq (9), it yields

$$\Delta\dot{\boldsymbol{\rho}} = k/3600 \boldsymbol{C_b}^{-1} \Delta\boldsymbol{I} + \boldsymbol{C_b}^{-1} \Delta\dot{\boldsymbol{I}} \tag{21}$$

where $\boldsymbol{C_b} = \mathrm{diag}\,(C_{b1}, C_{b2}, \cdots, C_{bn})$. With Eq (18) to Eq (21), the system dynamic can be expressed by

$$\Delta\dot{\boldsymbol{\varphi}} = \mathbf{A}\Delta\boldsymbol{\varphi} \tag{22}$$

where

$$\mathbf{A} = \left[\begin{array}{ccc} k_p\mathbf{A}_4 & -\boldsymbol{L} & -k_i - k_p l \\ \mathbf{0}_{(\boldsymbol{n}-1)\times\boldsymbol{n}} & & \mathbf{0}_{\boldsymbol{n}-1} \\ \hline k/3600\boldsymbol{C_b}^{-1}[\mathbf{A}_1, \mathbf{0}_{n\times n}, \mathbf{A}_2] + \boldsymbol{C_b}^{-1}[\mathbf{A}_1, \mathbf{A}_2]\,\mathbf{A}_3 & & \\ \mathbf{A}_4 & \mathbf{0}_n^{\mathrm{T}} & l \end{array}\right]$$

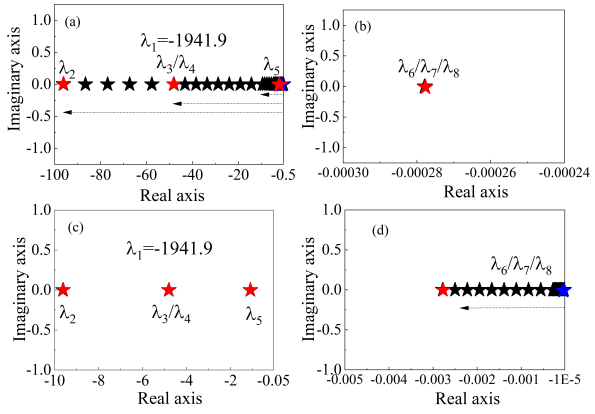

Fig. 6. Eigenvalue movement (a) λ_1 to λ_5 as a increases (b)λ_6 to λ_8 as a increases (c) λ_1 to λ_5 as k increases (d) λ_6 to λ_8 as k increases

Based on Eq (22), a four-BESSs-system is used to analyze the impact of control parameters communication weight a and SoC balance index k on the system response. The movement of eigenvalues as control parameters changing is illustrated in Fig.6. The blue stars represent where the eigenvalues move from and red stars represent where the eigenvalues stop, and

the arrows represent the movement of eigenvalues as these parameters vary. λ_2 to λ_5 reflect the ρ convergence speed. λ_6 to λ_8 are BESS SoCs related eigenvalues.

Fig.6 (a) and (b) show the movement of λ_1 to λ_5 and λ_6 to λ_8 as a increases, respectively. All eigenvalues are located in the left panel, which demonstrates that the whole system is stable. λ_2 to λ_5 move left which shows that the increase of a accelerates the ρ convergence speed, while λ_6 to λ_8 are kept unchanged, thus, the change of a does not have impact on BESS SoC balance speed.

The movement of λ_1 to λ_5 as k increases is illustrated in Fig.6 (c) and the movement of λ_6 to λ_8 as k increases is illustrated in Fig.6 (d). λ_1 to λ_5 are kept unchanged while λ_6 to λ_8 move left, thus, the increase of k achieves a quicker BESS SoC balance speed but does not impact the response of ρ.

V. Hardware-in-loop Test Results and Discussions

To validate the proposed DPP-based control framework, the HIL real-time tests are conducted at the Typhoon HIL-604 platform. As illustrated in Fig.7, the whole system (converters, BESSs, etc) is emulated by Typhoon HIL-604, while the controller for the real-time emulated system is implemented using a Texas Instruments TI LaunchPad (LAUNCHXL-F28069M), which is interfaced with the Typhoon HIL device through a Launchpad interface.

A four-BESSs-system is used to validate the proposed DPP-based control framework. The parameters for the battery modeling are presented in the Table I, where four batteries have identical parameters, while the parameters for the converter circuit and controller are listed in Table II. where P_{pv} is the output power of PV panel.

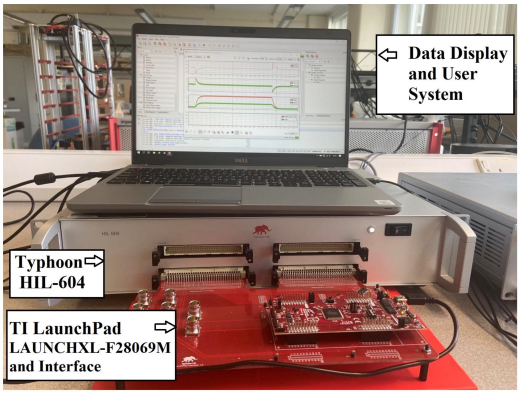

Fig. 7. HIL tests

A. Test Results Under Load and PV Disturbances

The performance of the proposed DPP-based control framework under load and PV disturbances is illustrated in Fig.8, the load is connected at about 6 s and the PV is connected at about 16 s. BESSs work at discharging mode after 6 s to support the load, and the proposed controller forces the BESSs to supply same output current. Then BESSs switch to the charging mode when PV is connected at 16 s. Similarly, the BESS charging currents also converge to the same value.

TABLE II
System and Control Parameters Used in HIL Tests

Parameters	Value	Parameters	Value
V_{dc}^*	900V	V_{fe}^*	300V
C_{dc}	0.01 F	SoC range	0.2-0.8
k	1	a	50
k_p	1	k_i	10
L_d/L_f	5e-3H	C_d/C_f	1e-3F
R_l	10 Ω	P_{pv}	14.4kW

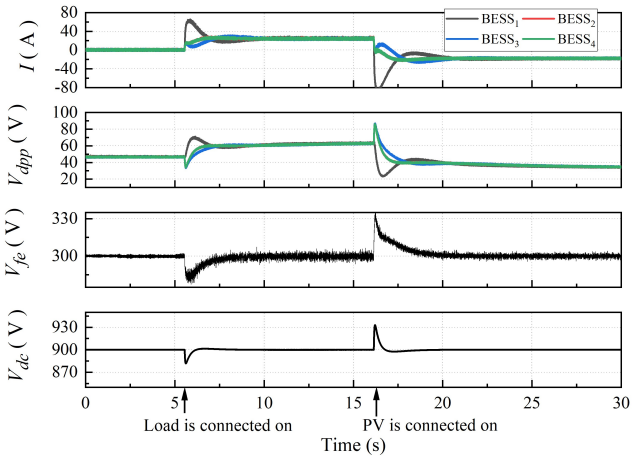

Fig. 8. Test results under load and PV disturbances

Fig.8 also illustrates the response of V_{fe} and V_{dc} under load and PV disturbances, it can be observed that they are regulated to their reference values 300V and 900V, respectively. V_{dpp} is dynamically changed to achieve the accurate current-sharing and DC bus voltage regulation.

B. SoC Balance Tests

The BESS SoC balance with different k is studied in this test. Fig.9 and Fig.10 illustrate the SoC balance when $k = 0.2$ and $k = 2$, respectively. The initial SoCs of BESS_1, BESS_2, BESS_3, BESS_4 are set to 0.7, 0.6, 0.5, 0.4, respectively. The SoC balance is activated at 6 s and PV is connected at about 27 s. After SoC balance is activated, the SoC difference gradually decreases, and BESSs with higher SoC discharge more current in the discharging mode, while they absorb less current in the charging mode.

It can be observed from Fig.9 and Fig.10 that a greater k leads to a quicker SoC balance speed, which verifies the conclusion in the stability analysis. And V_{dc} is regulated at 900 V.

C. Virtual State Variables Convergence Speed Tests

In this test, the response speed of ρ with different a is researched. Fig.11 (a) and (b) illustrate the test results with different $a = 10$ and $a = 100$, respectively. Load and PV are

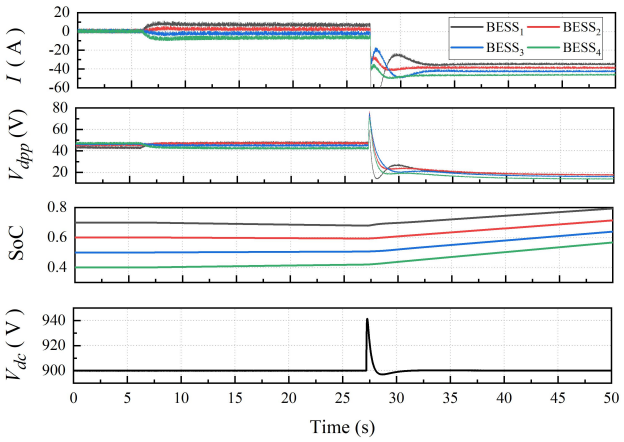

Fig. 9. BESSs SoC balance test when k=0.2

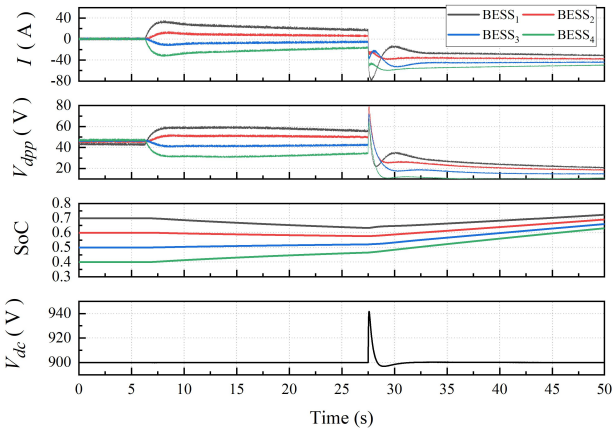

Fig. 10. BESSs SoC balance test when k=2

connected at about 7 s and 17 s, respectively. SoC balance index k is set to 0 in this test, thus, the response of ρ can be represented by the response of I. It can be observed that a greater a lead to a faster current convergence speed, which validates the conclusion in the stability analysis.

D. Power Requirements of Different Converters

As aforementioned, the proposed DPP-based control framework requires low converter power ratings compared with conventional BESS-DC bus configuration. The power of DPP and front-end converters under four different BESS operating scenarios are researched. V_{dpp}, I, $I_{fe,\alpha}$ with high BESS SoCs (SoC of four BESSs is 0.8) and low BESS SoCs (SoC of four BESSs is 0.2) are demonstrated in the Fig.12 and Fig.13, respectively. As shown in the Table III, the power of front-end converter and DPP converters together with BESS output power can be calculated based on the Eq (7) with the steady-state values marked in Fig.12 and Fig.13.

The power requirements under four following operating scenarios are summarized below

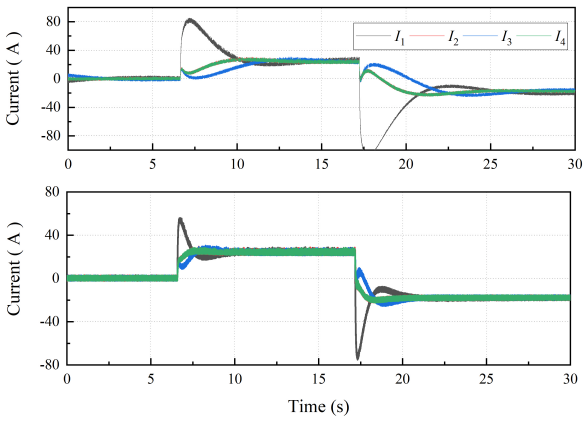

Fig. 11. Virtual state variables convergence speed tests when (a) a=10 (b) a=100

SoC is high and BESS is in charging mode. In this operating scenario, BESSs have the highest output voltage and the differences between DC bus and BESS output voltage are smallest. Therefore, the power of DPP converters and front-end converter is the lowest among the four operating scenarios.

SoC is low and BESS is in discharging mode. In this operating scenario, BESSs have the lowest output voltage and the differences between the DC bus and BESS output voltage are largest. Therefore, the power flowing through the DPP converters and the front-end converter is at its maximum.

SoC is high and BESS is in discharging mode/SoC is low and BESS is in charging mode. In these two operating scenarios, the differences between DC bus and BESS output voltage is medium. Therefore, the power of DPP converters and front-end converter is between aforementioned operating scenarios.

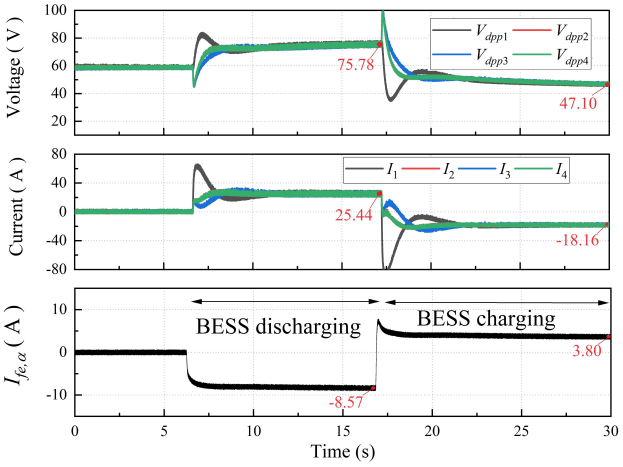

Fig. 12. Performance of the front-end and the DPP converters under low SoC condition

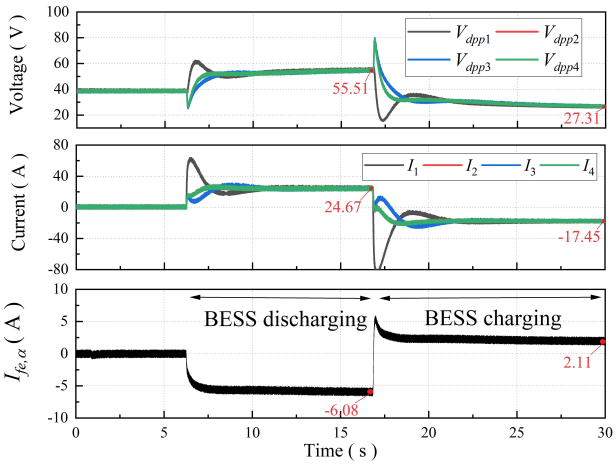

Fig. 13. Performance of the front-end and the DPP converters under high SoC condition

TABLE III
POWER OF BESS AND DIFFERENT CONVERTERS

Low SoC	BESS discharging	BESS charging
Front-end converter	7713 W	3420W
DPP converter	1928W	855W
BESS converter(conventional)	20500W	15900W
BESS	20500W	15900W
High SoC	**BESS discharging**	**BESS charging**
Front-end converter	5472 W	1908 W
DPP converter	1368W	477W
BESS converter(conventional)	20500W	15900W
BESS	20500W	15900W

The power of BESS converter used in the conventional BESS-DC bus configuration is also demonstrated in the Table III. It can be seen that the power of the front-end converter is n times of the DPP converter, n is the number of the DPP converters. Additionally, the power of DPP converter is 1928/20500=9.40% of the power of BESS converter used in the conventional BESS-DC bus configuration in the worst operating scenario (low SoC and BESS discharging), and that value for the front-end converter is 37.62%. The power of all converters in the proposed control framework is 1928×4+7713=15425W, while the power for all BESS converters in the conventional BESS-DC bus configuration is 20500×4=82000W. Thus, the total power requirement of all converters is reduced to 15425/82000=18.81 % in the worst operating scenario.

In the best operating scenario (high SoC and BESS charging), the power of the DPP converter and the front-end converter are further reduced to 3.00 % and 11.94 % of the power of BESS converter, respectively. The power of all converters is reduced to 5.97 % .

In summary, the power requirement of the converters are reduced to less than 20 % in the worst operating scenario with the proposed DPP-based control framework, and that value will be even smaller for all other operating scenarios. Considering the power losses and installation cost of converters are proportional to their power ratings, the installation cost and power losses will be significantly reduced with the proposed DPP-based control framework.

VI. COMPARISONS WITH CONVENTIONAL CONFIGURATION

The performance of the conventional BESS-DC bus configuration is presented as a comparison to further validate the proposed control framework. Note that the step-down converters are used, the output voltages of BESSs are raised to around 1500V in the conventional configuration. The other parameters of controllers and converters are kept as identical with that in Table II. To reduce the impact of external noise and the signal detecting error, the tests are conducted in the Matlab/Simulink environment. As illustrated in Fig.14, two topologies present similar DC bus voltage regulation and current-sharing performance. However, the proposed control framework significantly mitigates noise resulting from switching. Notably, the current ripple is reduced to 1 A, compared to approximately 10 A in the conventional configuration.

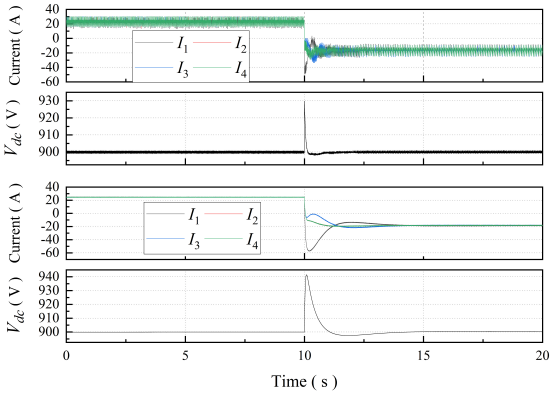

Fig. 14. The test results with the conventional configuration (first two figures) and the proposed control framework (last two figures)

We have further investigated the changes in the power requirement for the all converters with the proposed control framework as the efficiency of these converters and output voltage of DPP converters vary. For simplicity, the efficiencies of all converters are set to an identical value η. Similarly, the output voltage of all DPP converters and output current of all batteries are set to V_{dpp} and I, respectively. Note that the power of front-end converter equals to the power of all DPP converters if neglecting the power losses, the total power of all converters with the proposed control framework (P_1) can be calculated by

$$P_1 = P_{fe} + 4P_{dpp} = 4V_{dpp}I/\eta^2 + 4V_{dpp}I/\eta \qquad (23)$$

Assuming the power mismatch between loads and PV panels is P_0, BESSs are then used to compensate the power mismatch, it is easy to derive Eq (24) by neglecting the losses

$$I = \frac{P_0}{4V_b} = \frac{P_0}{4\left(V_{dc} - V_{dpp}\right)} \qquad (24)$$

Combing Eq (23) and Eq (24), it yields Eq (25a). And the total power of all converters with conventional configuration (P_2) is expressed by Eq (25b).

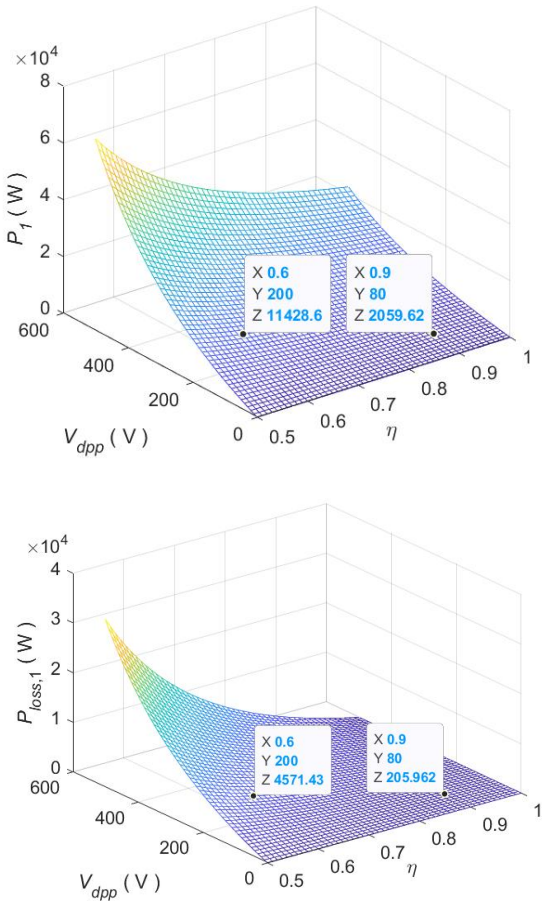

Fig. 15. The total power requirement and power loss of all converters with the proposed control framework.

$$P_1 = \frac{V_{dpp} P_0}{(V_{dc} - V_{dpp})\,\eta^2} + \frac{V_{dpp} P_0}{(V_{dc} - V_{dpp})\,\eta} \tag{25a}$$

$$P_2 = P_0/\eta \tag{25b}$$

Similarly, the power losses of all converters with the proposed control framework $P_{loss,1}$ and conventional configuration $P_{loss,2}$ are expressed by

$$P_{loss,1} = \frac{V_{dpp} P_0}{(V_{dc} - V_{dpp})} \left(1/\eta^2 - 1\right) \tag{26a}$$

$$P_{loss,2} = P_0 \left(1/\eta - 1\right) \tag{26b}$$

With Eq (25) and Eq (26), the total power requirement and power loss of all converters with the proposed control framework as a function of the efficiency and the DPP voltage are illustrated in Fig.15, while Fig.16 illustrates the results for the conventional configuration. It can be observed that both the power requirement and power loss increase as V_{dpp} increases and η decreases, those values for the proposed control framework are much lower than that for the conventional configuration when η is about 0.9. The power requirements and power loss of converters for the two topologies are about the same level when η is about 0.6 and V_{dpp} is more than 200V. However, generally speaking, the converters do not work at that low efficiency and V_{dpp} is not designed that high.

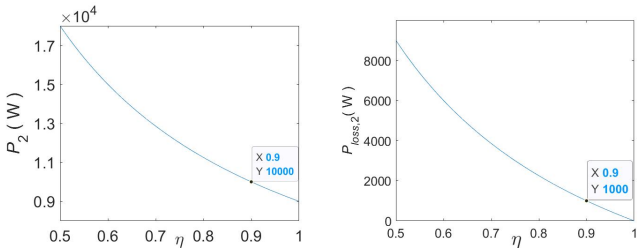

Fig. 16. The total power requirement and power loss of all converters with conventional configuration.

VII. Conclusions

This paper has proposed a new DPP-based control framework to reduce the power ratings for BESS converters while delivering the same power from BESSs. This is achieved first by introducing inverted bidirectional buck converters to function as a front-end converter and DPP converters. Then, a virtual state variable combining BESS output current and its SoC is proposed, based on which a consensus control strategy is proposed to simultaneously achieve multiple control objectives, namely accurate current sharing, SoC balancing, and and DC bus voltage regulation. The stability of the proposed DPP-based control framework is also analyzed. Finally, the real-time HIL tests confirm the effectiveness of the proposed control framework, showing that the proposed DPP-based control framework reduces the power ratings of the converters to less than 20 % of BESS converters used in conventional BESS-DC bus configuration even in the worst operating scenario, while delivering the same required power from BESSs, paving a way for an innovative BESS DC microgrid design with much down-sized converters for BESSs.

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