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Analytical modelling of SiC MOSFET based on datasheet parameters considering the dynamic transfer characteristics and channel resistance dependency on the drain voltage

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***Abstract*—Silicon Carbide devices enable high power density power electronic converters due to their lower junction capacitances and higher thermal conductivity. Analytical models of these devices help in estimating the switching dynamics, losses and current/voltage stresses on the devices. The dynamics of SiC MOSFET current during turn ON is impacted by the drain voltage it is switched at, due to the drain induced barrier lowering (DIBL) effect. This is however ignored in the existing analytical models available in the literature. This paper thus proposes and develops a new analytical modelling approach that models this effect by relying only on the datasheet parameters, thereby avoiding the need for expensive and time-consuming experimental methods. Dynamic channel resistance is also modelled as a function of drain voltage. The analysis reveals the impact of drain voltage on damping time of high frequency drain current oscillations during turn ON. An experimental double pulse test (DPT) setup using 1.2kV SiC MOSFET (C3M0010602K) and Schottky diode (C4D40120D) is built to verify the findings. Further, the accuracy of the proposed model is compared against the most detailed existing model in the literature.**

Keywords—Drain induced barrier lowering, SiC MOSFET, double pulse test, switching loss, analytical model.

I. INTRODUCTION

Analytical models for high voltage SiC MOSFETS (1.2 kV) with discrete packages (TO – 247) were done in [1] – [3]. While [1] included the discharging currents into the output capacitance of the MOSFET, [2] modelled the dynamic parasitic capacitances with drain voltage. These models used linear transconductance fitting for analysis. Various other modelling approaches of transconductance were done by authors in [4] – [7]. Each of these demonstrated an improvement in accuracy of loss estimation over linear fitting of transconductance curve. The transconductance data used for modelling the SiC MOSFET current transition in all the above analytical modelling approaches is derived from the datasheet, that corresponds to the drain voltage of 20V. This is insufficient for modelling the behaviour of SiC MOSFETs switching at higher voltages, as there exists a significant change in the transconductance at higher drain voltages due to the drain induced barrier lowering (DIBL) and short channelling effect [8]. If not considered, it results in slower current rise estimates. Though the approach in [9] further improved the accuracy in estimating the current rise of SiC MOSFET by considering DIBL effect, it involved an experimental procedure that is both uneconomical and time consuming. In this paper, a novel mathematical methodology to estimate transconductance characteristics at higher drain voltages, by extrapolating the limited data from the output characteristics given in datasheet and choosing a suitable mathematical fit by considering the statistical measures is proposed. It eliminates the need for any additional experimental effort for modelling DIBL effect. Furthermore, dependency of channel resistance on drain voltage is modelled based only on datasheet information which is not considered in existing model [2].

In the following sections, the impact of dynamic transconductance on the accurate estimation of current is explained. The procedure to obtain the information needed to model these effects from datasheet is demonstrated. Also, the influence of dynamic channel resistance on modelling the oscillatory behavior of drain current during voltage fall is discussed. An experimental double pulse test circuit is used to validate the proposed mathematical modelling and the corresponding results at a wide range of operating points are presented. Finally, a comparative analysis of the improvement in accuracy of turn ON loss estimation due to the proposed model over the existing approaches is shown.

II. DEPENDENCY OF CURRENT RISE ON DRAIN VOLTAGE DURING MOSFET TURN ON

Fig. 1 shows the experimental double pulse test (DPT) circuit comprising of a SiC MOSFET along with a complementary Schottky diode in parallel with an inductive load. The corresponding circuit with the equivalent circuit models of the MOSFET, Schottky diode and the inductive load comprising of their parasitic elements and the respective voltages and currents are as indicated in Fig. 2.

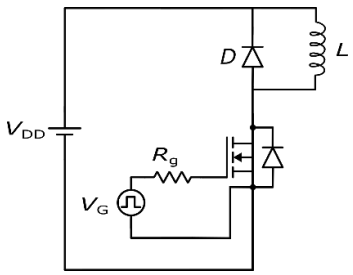


Fig. 1: Experimental double – pulse test setup

A. Analytical modelling of turn ON

The turn ON of SiC MOSFET is sub – divided into four separate stages as shown in Fig. 3. It consists of the delay

stage followed by the current rise, voltage fall and the oscillatory stages. The corresponding mathematical equations of each stage are given in Appendix for brevity.

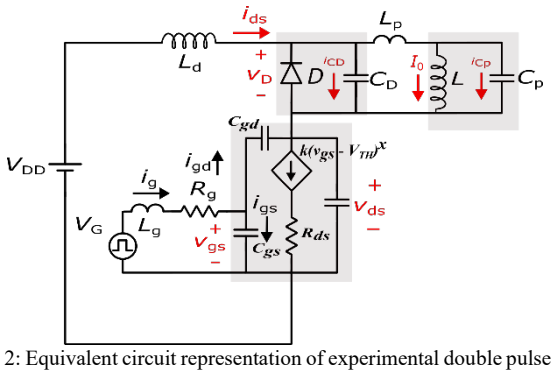


Fig. 2: Equivalent circuit representation of experimental double pulse test setup.

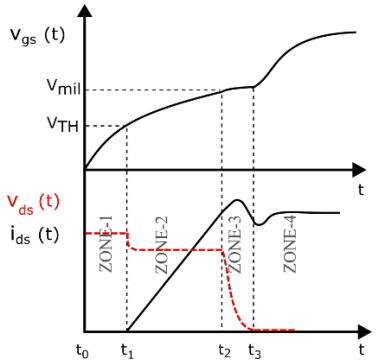


Fig. 3: Turn ON of SiC MOSFET – stage wise representation

B. *Current rise of SiC MOSFET – Impact of drain voltage*

With the gate source voltage crossing the threshold level $v_{gs} > V_{TH}$, the MOSFET channel starts to conduct. The current starts to rise during this time with a corresponding fall in the freewheeling diode current. Since $(v_{gs} > V_{TH})$ and $v_{ds} > (v_{ds} - V_{TH})$, the MOSFET is in saturation region. Considering the non – linearity of transfer characteristics, the channel current during this time interval is expressed as a function of gate – source and drain- source voltage according to Shichman – Hodges' physical model in saturation region as shown in (1) and (2).

$$i_{ds}(v_{gs}, v_{ds\_p}) = k'_{v_{ds\_p}}(v_{gs} - V_{th})^x \quad (1)$$

$$k'_{v_{ds\_p}} = k_{v_{ds\_p}}\left(1 + \lambda_{v_{ds\_p}} v_{ds\_p}\right) \quad (2)$$

As can be observed from the above equations, the channel current in saturation region depends on the drain voltage. This is due to the drain induced barrier lowering phenomenon and can be seen from the varying slope of the transfer characteristics with drain voltage in Fig. 4. This phenomenon needs to be included in the analytical model for accurate estimation of device characteristics. Ignoring it would result in slower current rise estimations which leads to over estimation of switching loss. This is illustrated in Fig. 5 where conventional analytical models that do not consider this phenomenon is compared with the experimental results.

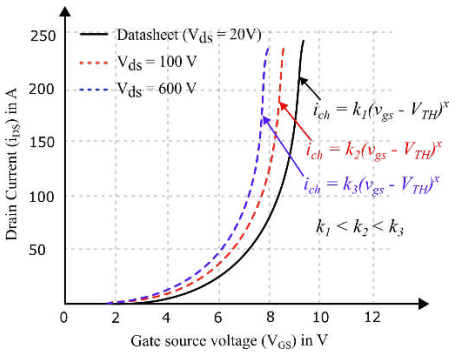


Fig. 4: Impact of drain voltage on transfer characteristics

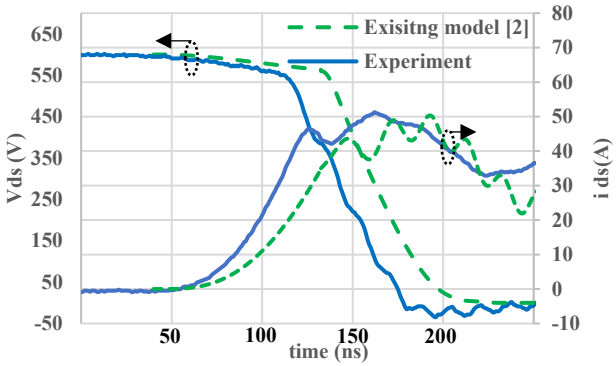
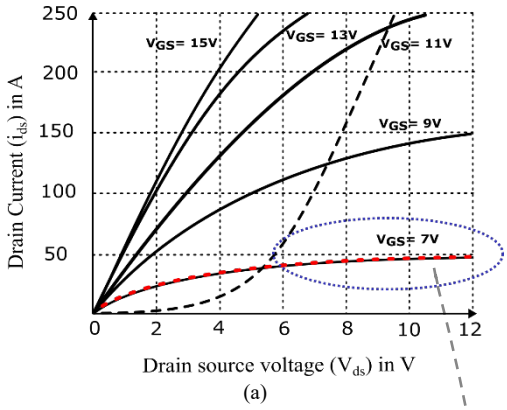
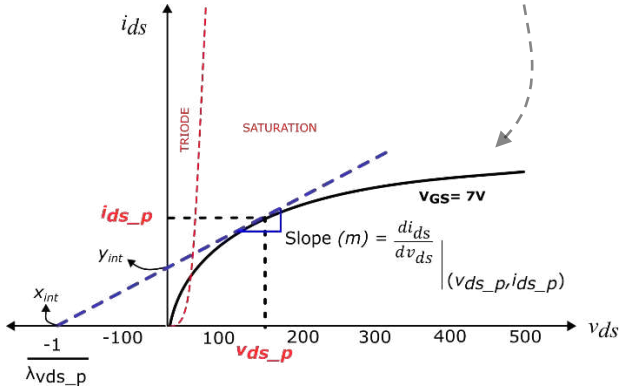


Fig. 5: Comparison of conventional analytical model and experimental turn ON waveforms at 600V/40A

C. *Modelling of v_{ds} dependent transfer characteristics*



(a)



(b)

Fig. 6(a): Output characteristics of C3M0016120K. (b): Extrapolated output characteristics at $V_{GS} = 7V$ and the corresponding intercepts of the tangent at (v_{ds_p}, i_{ds_p})

The output characteristics of the SiC MOSFET provides the basis for extracting the information related to the dependency of channel current on drain voltage. Since the MOSFET is in saturation during current rise, the corresponding section of the output characteristics at a given V_{GS} is curve fitted into an n^{th} order polynomial equation as in (3).

$$v_{ds} = a_0 i_{ds}^{n} + a_1 i_{ds}^{n-1} \dots + a_k i_{ds}^{n-k} \dots + a_n \tag{3}$$

The extracted data is denoted by the dotted red line in Fig. 6(a), while the extrapolated version is shown in Fig. 6(b). The choice of order of the polynomial is based on the accuracy of the curve fit determined using statistical measures such as R^2. As shown in Fig. 6(b) , the slope of the tangent to the curve at an operating point (v_{ds_p}), and the intercepts it makes on the drain voltage and drain current axes are used to obtain the values of $k_{v_{ds\_p}}$ and $\lambda_{v_{ds\_p}}$ at a particular drain voltage v_{ds_p}. While the slope is defined as in (4), the value of i_{ds_p} is evaluated using (3). The expressions for the corresponding values of intercepts (i.e., x_{int} and y_{int} as shown in Fig. 6(b)) are shown in (5) and (6) respectively.

$$m = \frac{di_{ds}}{dv_{ds}}|(v_{ds\_p}, i_{ds\_p}) = \frac{1}{na_0 i_{ds}^{n-1} \dots + (n-k)a_k i_{ds}^{n-k-1} \dots + a_{n-1}} \tag{4}$$

$$x_{int} = \frac{mv_{ds\_p} - i_{ds\_p}}{m} \tag{5}$$

$$y_{int} = i_{ds\_p} - mv_{ds\_p} \tag{6}$$

Using the intercept values in (5) and (6), $\lambda_{v_{ds\_p}}$ and $k_{v_{ds\_p}}$ are calculated as in (7) and (8).

$$\lambda_{v_{ds\_p}} = \frac{-1}{x_{int}} = \frac{m}{mv_{ds\_p} - i_{ds\_p}} \tag{7}$$

$$k_{v_{ds\_p}} = \frac{y_{int}}{(V_{GS} - V_{TH})^x} = \frac{i_{ds\_p} - mv_{ds\_p}}{(V_{GS} - V_{TH})^x} \tag{8}$$

Transfer characteristics given in the datasheet are used to obtain x and V_{TH} through curve fitting. Using (2), (7) and (8), $k'_{v_{ds\_p}}$ is derived. The variation of $\lambda_{v_{ds\_p}}$, with the drain voltage operating point is shown in Fig. 7, while Fig. 8 shows the variation of $\lambda_{v_{ds\_p}}$ and $k_{v_{ds\_p}}\left(1 + \lambda_{v_{ds\_p}}\right)$ with drain voltage explicitly for C3M0016120K MOSFET.

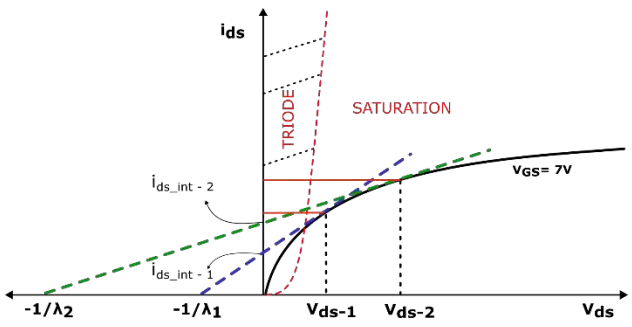


Fig. 7: Variation of $\lambda_{v_{ds\_p}}$ and i_{ds} intercept with v_{ds}.

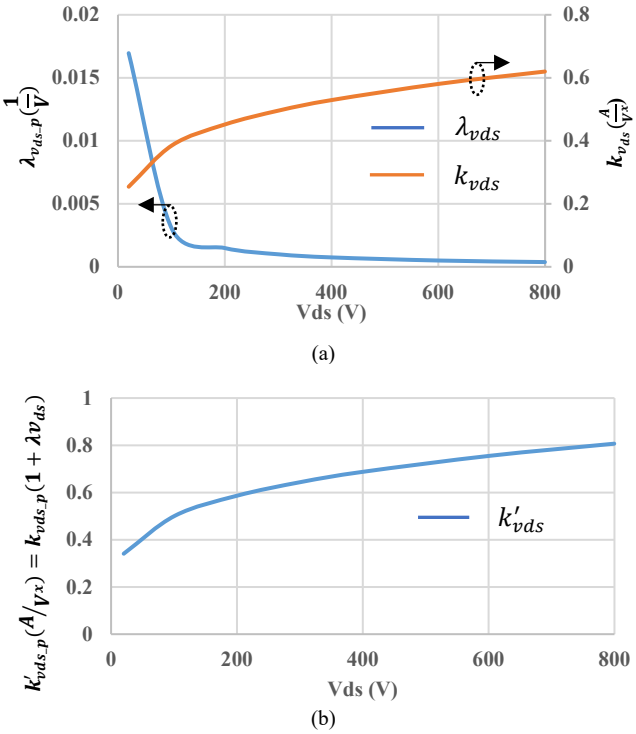


Fig. 8: C3M0016120K (a): Variation of $\lambda_{v_{ds\_p}}$ and $k_{v_{ds\_p}}$ with drain voltage. (b) Variation of $k'_{v_{ds\_p}}$ with drain voltage.

D. Modelling of v_{ds} dependent channel resistance

In contrast with the conventional model where a constant resistance is used to model the channel during the voltage fall, the proposed model considers this resistance as a variable quantity as the MOSFET transits through the saturation region into the ohmic region. The slope of the output characteristics is used for computing this dynamic resistance of the channel during voltage fall of the MOSFET turn ON. It is modelled as a function of drain source voltage until v_{ds} falls to the saturation level, $(v_{ds} = v_{gs})$ and is defined as a ratio of change in v_{ds} to i_{ds} and expressed as in (9).

$$R_{ds}(v_{ds}) = \frac{\partial v_{ds}}{\partial i_D}(V_{GS} = constant) \tag{9}$$

The variation R_{ds} with v_{ds} impacts the damping of the high frequency oscillations in drain current during voltage fall interval of the MOSFET turn ON.

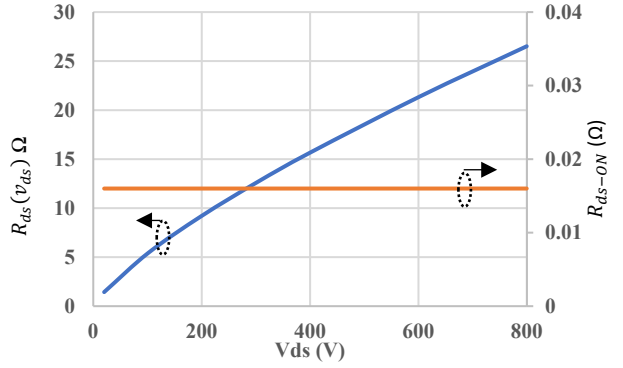


Fig. 9: Comparison of fixed channel resistance in triode region (R_{ds-ON}) to variable resistance in saturation region ($R_{ds}(v_{ds})$) of C3M0016120K

III. EXPERIMENTAL VS NEW MODEL COMPARISON

A. Turn ON waveforms comparison

With the mentioned improvements in modelling the SiC MOSFET, a comparison of experimental and analytical models (existing and improved) is done in this section. The experimental results are obtained from the double pulse test setup, with a 1.2 kV SiC MOSFET and 1.2kV SiC Schottky diode complementary to it. The test setup is shown in Fig. 10. The measurements are recorded on a 200 MHz, 4GS/s, digital signal oscilloscope DSOX3024A using a 100 MHz differential voltage probe (TA042) and 30 MHz Rogowski coil (T3RC0300 – UM).

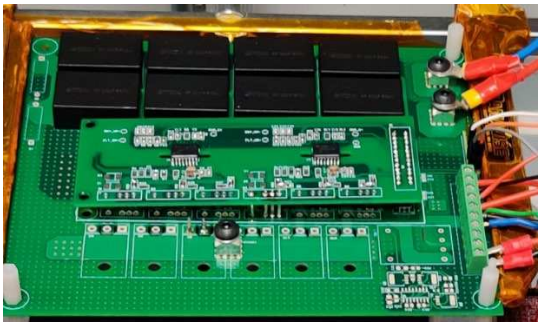
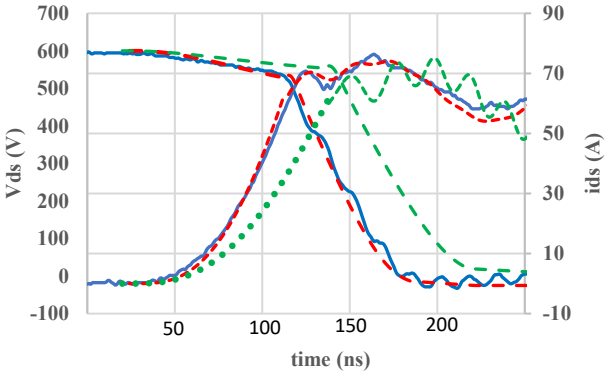
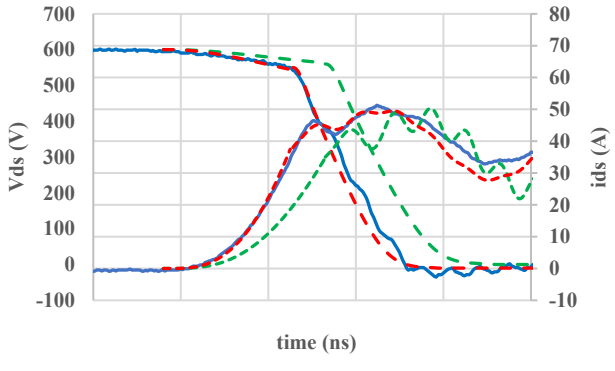


Fig. 10: Double pulse test (DPT) setup.

Experimental waveforms were obtained over a wide range of voltage and current operating points: V_{ds}: 200V – 600V and i_{ds}: 20A – 60A. A turn ON gate resistance of 20Ω was used in the double – pulse tests.



(a)

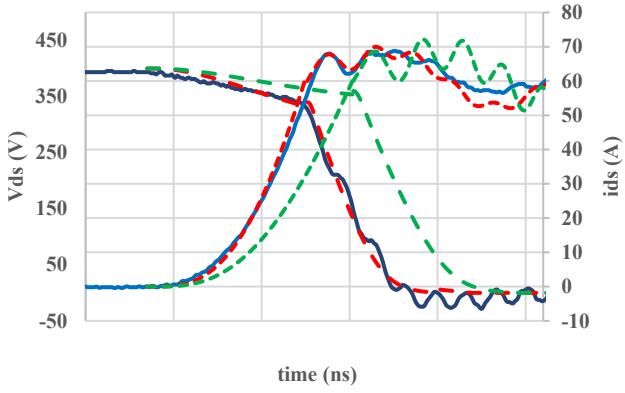


(b)

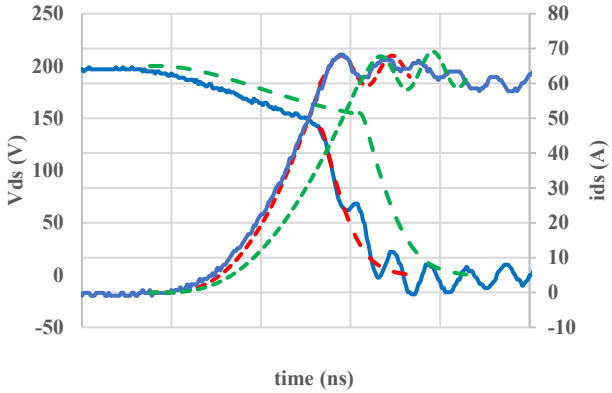
Experiment Existing model New model

Fig. 11: Comparison of turn ON at 600V – (a): 60A (b) 40A

Analytical model with $(k_{v_{ds\_p}}, \lambda_{v_{ds\_p}})$ obtained by fitting the output characteristics of datasheet to a 4th order polynomial is compared with the experimental waveforms and existing model. Fig. 11 shows the comparison at 600V and at different currents, while Fig. 12 shows the comparison at 60A, at different voltages.



(a)



(b)

Experiment Existing model New model

Fig. 12: Comparison of turn ON at 60A – (a): 400V (b) 200V

B. Impact of dynamic channel resistance modelling

The impact of modelling dynamic channel resistance $(R_{ds}(v_{ds}))$ is demonstrated in Fig. 13. As shown, if a constant resistance (R_{ds-ON}) is considered as in conventional models, the i_{ds} estimated deviates from the experimental waveforms. It exhibits oscillation that are not damped as much as in the case of experimental or the proposed model and results in additional error in loss estimation.

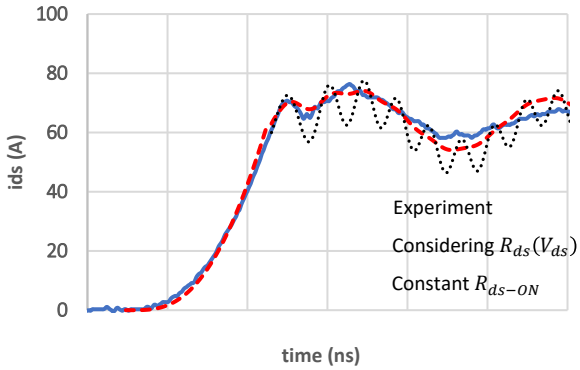


Fig. 13: Comparison of experimental and model drain current oscillations with and without considering $R_{ds}(v_{ds})$

C. *Turn ON loss estimation – comparison*

From the waveforms obtained from both the improved and the existing models, turn ON switching loss estimations were done and compared with the experimental results at each test point. Fig. 14 (a) gives a comparison of turn ON switching loss at 600V, while the test current was varied from 20A to 60A. In Fig. 14 (b), turn ON switching loss at 60A was compared, while the DC voltage was varied from 200V to 600V.

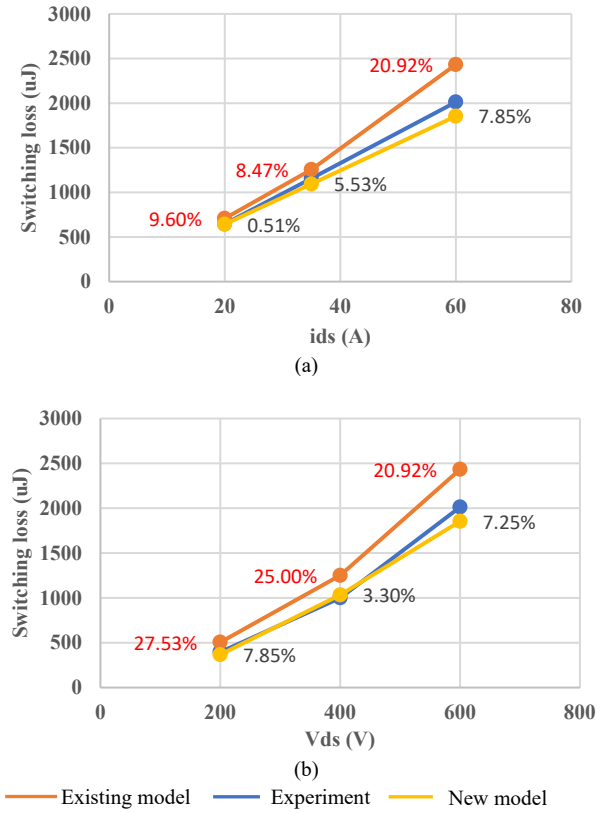


Fig. 14: Comparison of turn ON switching loss (a): at 600V (b) at 60A

As can be observed from the loss comparison in Fig. 14, there is a considerable improvement in accuracy due to the proposed model over the conventional model across the wide operating range.

IV. CONCLUSION

This research study proposes an improved analytical model of SiC MOSFET to predict its turn ON waveforms and associated losses considering the DIBL phenomenon. It proposes a mathematical methodology to account for the DIBL effect that influences the transfer characteristics with drain voltage. This is accomplished by relying on the output characteristics that is a part of datasheet parameters and eliminates the need for elaborate test procedure. It also proposes a dynamic channel resistance that impacts the damping time of the high frequency drain current oscillations during turn ON. The proposed analytical model's waveforms show a better match with the experimental results as compared to the existing model, with a reduction in maximum switching loss estimation error from 27% to 7.8%.

APPENDIX

The equations describing the turn ON of SiC MOSFET depicted in a stage wise approach as in Fig. 3 are given in this section:

Zone 1: Delay time *($t_0 - t_1$):*

Equations representing this stage are as shown in (1) and (2).

$$v_{GG} = v_{gs} + R_g i_g + L_g \frac{di_g}{dt} \tag{1}$$

$$i_g = (C_{gs} + C_{gd}) \frac{dv_{gs}}{dt} \tag{2}$$

Zone 2 : Current rise *($t_1 - t_2$):*

Equations (1) and (2) continue to be valid in describing v_{gs}. Channel current and voltage across drain – source of MOSFET are described using (3) and (4). Equivalent circuit of this stage is as shown in Fig. 15

$$i_{ds} = f(v_{gs}, v_{ds}) = k(v_{gs} - V_{TH})^x \tag{3}$$

$$v_{ds} = V_{DD} - L_d \frac{di_{ds}}{dt} \tag{4}$$

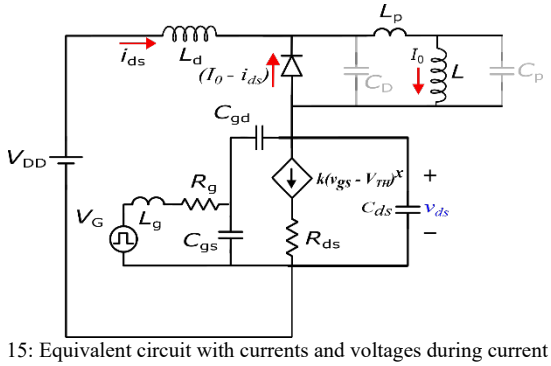


Fig. 15: Equivalent circuit with currents and voltages during current rise

Zone 3: Voltage fall *($t_2 - t_3$):*

The state of the DPT circuit in this stage is as shown in Fig. 16. In addition to the load current, diode's parasitic capacitance current i_{C_D} along with the current i_{C_p} to charge the parasitic capacitance C_p across the load inductor constitutes drain current as in (5).

$$i_{ds} = i_{C_D} + i_{C_p} + I_0 \tag{5}$$

Gate – Kelvin side in this stage is defined as in (6) and (7).

$$i_g = i_{gs} + i_{gd} \tag{6}$$

$$v_{GG} = L_g C_{iss} \frac{d^2 v_{gs}}{dt^2} + R_g C_{iss} \frac{dv_{gs}}{dt} + v_{gs} - R_g C_{gd} \frac{dv_{ds}}{dt} \tag{7}$$

The parasitic components of the load and devices are considered to describe the voltage across the diode and MOSFET as in (8) and (9)

$$V_{DD} = v_{ds} + L_d \frac{di_{ds}}{dt} + L_p \frac{d}{dt}\left(i_{ds} - i_{C_D}\right) + v_{C_p} + R_{ds} i_{ds} \quad (8)$$

$$L_p \frac{di_{C_p}}{dt} + v_{C_p} - v_{C_D} = 0 \quad (9)$$

The parasitic capacitances of the SiC MOSFET and Schottky diode are dependent on v_{ds} and are modelled as shown in (10).

$$C_D(v_{ds})/C_{ds}(v_{ds})/C_{gd}(v_{ds}) = \frac{c_0}{\left(1 + c_1 v_{ds}^{c_2}\right)} + c_3 \quad (10)$$

where, c_0 , c_1 , c_2 and c_3 are curve fitting parameters.

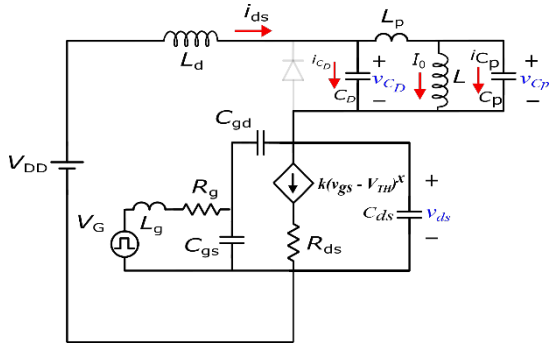


Fig. 16: Equivalent circuit with currents and voltages during voltage fall.

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