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A new back-to-back graded AlGaIn barrier for complementary integration technique based on GaN/AlGaIn/GaN platform

Jinggui Zhou¹, Huy-Binh Do², and Maria Merlyne De Souza¹

¹The University of Sheffield, UK, ²Ho Chi Minh City University of Technology and Education, Vietnam

Abstract

A novel composite barrier layer with back-to-back graded AlGaIn in a GaN/AlGaIn/GaN epitaxial structure for high performance n- and p-channel devices on the same platform is proposed. By adjusting the relative thicknesses of the two graded layers, we obtain a spread in the width and concentration of carriers in the 3D slabs. The best barrier amongst those studied, enhances the on-current (I_{ON}) by 24.4% in low voltage n-channel devices, 32.2% the p-channel devices whereas the figure of merit of the power device is higher by 3 times, in comparison to the conventional platform. (Keywords: GaN/AlGaIn/GaN, back-to-back graded AlGaIn, complementary integration, n-channel, p-channel, and breakdown voltage)

Introduction

The p-GaN/AlGaIn/GaN based epitaxial structure is a well-known platform for n-off operation of commercially available power devices [1]–[3]. Such p-GaN gated HEMTs with source field plates and breakdown voltage (V_{BV}) > 1 KV have been monolithically integrated with gate drivers in high voltage (HV) modules, to reduce parasitic loop inductance during switching, resulting in enhanced reliability, and fast switching capability [3][4]. By growing the AlGaIn/GaN on an AlN buffer, a high V_{BV} of 2154V and figure of merit (FOM) of $1.8 \text{ GV}^2/\Omega \cdot \text{cm}^2$ was demonstrated in [5]. p-GaN HEMTs have shown leakage current suppressed to $1 \mu\text{A}/\text{mm}$ for 1100V blocking capability through gate stack design [6]. However, the p-GaN/AlGaIn/GaN platform results in low hole mobility, high on-resistance for Enhancement-mode (E-mode) p-channel devices that reduces the voltage gain for related CMOS [4][7]. On the other hand, a graded AlGaIn barrier layer improves channel transconductance and carrier conductivity due to polarization “doping” in a three-dimensional (3D) carrier slab [8][9]. Thus, to eliminate the mutual limitation in n-and p-channel devices in GaN/AlGaIn/GaN based double heterostructures a new composite AlGaIn barrier with back-to-back graded layer is examined in this work.

Methodology

Our p-GaN/u-GaN/AlGaIn/GaN simulation platform is benchmarked for both n-and p-channel devices against the experimental data that was presented by Palacios et al in Fig.1 [10]. This structure consists of 20nm p^{++}GaN with Mg doping ($[\text{Mg}]$) of $6 \times 10^{19}/\text{cm}^3$, 70nm p^+GaN with $[\text{Mg}] = 1 \times 10^{19}/\text{cm}^3$, 20nm u-GaN channel and $\text{Al}_{0.2}\text{Ga}_{0.8}\text{N}$, and 150nm GaN buffer. The mobility of holes is kept at $10 \text{ cm}^2/\text{Vs}$ [10]. In addition, an interface fixed charge and trap density at the oxide/GaN interface of $6.4 \times 10^{12} \text{ cm}^{-2}$ and $3 \times 10^{12} \text{ cm}^{-2}$, respectively, are introduced in the model to match the reported experimental $I_D - V_{GS}$ curves in Fig.1(b). The main change from the structure in [10] proposed in this work is replacement of the conventional AlGaIn barrier with graded counterpart. A positive graded AlGaIn in this work, is one with Al mole fraction higher at the top and lower at the bottom, resulting in $\Delta x_{b,p} = x_{b,top} - x_{b,bottom} > 0$. The negative graded AlGaIn is the opposite, ie $\Delta x_{b,n} = x_{b,bottom} - x_{b,top} > 0$. Their respective thicknesses are referred to as $t_{b,n}$ and $t_{b,p}$ in Fig.2 (a). By keeping $\Delta x_{b,n} = \Delta x_{b,p}$, several barriers examined are listed in Table 1. The negative graded layer is considered as a part of the p-GaN gate stack in n-channel devices as shown in Fig.2(b). Moreover, the ideal thickness of the u-GaN channel layer t_{ch} in a p-GaN/u-GaN/AlGaIn/GaN structure has been shown to be $\leq 5 \text{ nm}$ [11]. Hence a 5nm u-GaN layer is considered in this work.

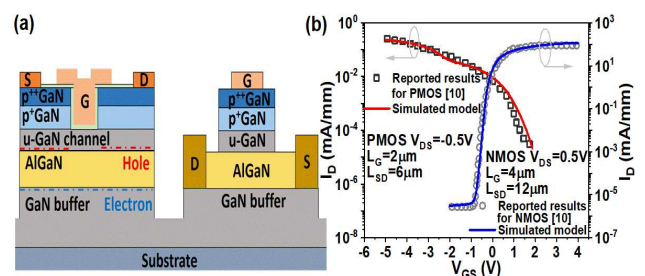


Fig.1: (a) Schematic of the benchmarked platform for integration of n- and p-channel device [10]. (b) The $I_D - V_{GS}$ curves of n- and p-channel devices for benchmarking our simulations against experimental results reported in [10].

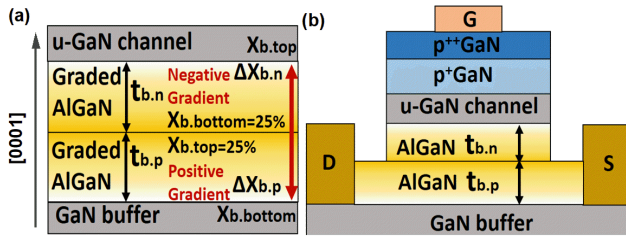


Fig.2: (a) Schematic of the new composite AlGaIn barrier layer with back-to-back graded layers. (b) The gate stack for n-channel devices.

Table 1: List of composite AlGaIn barriers

ID	Barrier parameter	
BarrierA	$Al_{0.25}Ga_{0.75}N$, $t_b = 20nm$	
ID	Upper negative graded layer	Lower positive graded layer
BarrierB	$x_{b,bottom} = 25\%$, $\Delta x_{b,n} = 25\%$, $t_{b,n} = 15nm$	$x_{b,top} = 25\%$, $\Delta x_{b,p} = 25\%$, $t_{b,p} = 5nm$
BarrierC	$x_{b,bottom} = 25\%$, $\Delta x_{b,n} = 15\%$, $t_{b,n} = 15nm$	$x_{b,top} = 25\%$, $\Delta x_{b,p} = 15\%$, $t_{b,p} = 5nm$
BarrierD	$x_{b,bottom} = 25\%$, $\Delta x_{b,n} = 25\%$, $t_{b,n} = 10nm$	$x_{b,top} = 25\%$, $\Delta x_{b,p} = 25\%$, $t_{b,p} = 10nm$

Results and discussion

Fig.3(a) reveals $I_D - V_{GS}$ characteristics of p-GaN gated n-channel devices, shown in Fig.2(b), as a function of barrier type. The on-state current densities increase by $\sim 8-24.4\%$ when barrier A is replaced by barriers B, C, and D, due to the contribution of the positive graded AlGaIn layer. In addition, a positive shift of V_{th} is observed with increase of the thickness $t_{b,n}$ of the negative graded layers in the gate stack, because the negative graded layers suppress the leakage across the 3DEG slab in positive graded AlGaIn. The operation mode is changed from depletion-mode (D-mode) to E-mode when barrier A is replaced by barriers B, C, and D, reaching $V_{th} = +0.5V$ in device with barrier B. According to the $I_D - V_{DS}$ characteristics in Fig.3(b), I_D is lower in Barrier B at low gate voltage (V_{GS}) but surpasses that in Barrier A at higher V_{GS} with the help of positive barrier AlGaIn. The reduced on-resistance (R_{ON}) is due to the 3DEG as the polarization “doping” distributed in positive graded layers. It is seen in Fig.3(c) that the electron density (n_e) distribution of Barrier B is lowest, whereas its hole density (n_h) at the u-GaN/AlGaIn interface is widest, across the u-GaN channel and AlGaIn barrier. Therefore, besides the enhancement of V_{th} , the negative graded AlGaIn suppresses the n_e below the gate, which contributes

to improved electrostatics for n-channel devices. Fig.3(d) illustrates that the concentration peak of carriers at both u-GaN/AlGaIn and AlGaIn/GaN interfaces are reduced, widened at large $\Delta x_{b,n}$ and $\Delta x_{b,p}$. As $t_{b,n} = 15nm$, the maximum $\Delta x_{b,n}$ makes the conduction band at the AlGaIn/GaN interface shift upward, which means Barrier B can deplete the electron gas under the gate. Based on Barrier D, the hole distribution width is limited by the increased $t_{b,p}$. At maximum $\Delta x_{b,p}$, the conduction band at the AlGaIn/GaN interface is expanded and shifted downwards, resulting in enlargement of the width and peak of the electron distribution. As a result, V_{th} is negative, leading to the LV n-channel device operating in D-mode.

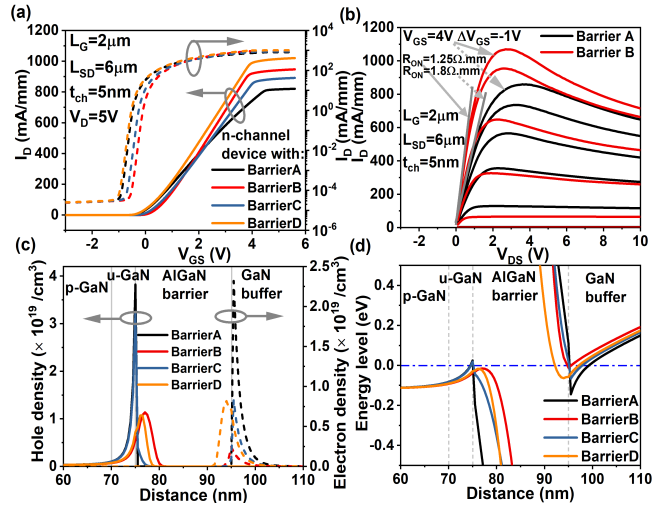


Fig.3: (a) I_D vs. V_{GS} in linear and log scale for scaled LV n-channel devices with different types of barriers at $V_D = 5V$. (b) Comparison of $I_D - V_{DS}$ curves between LV n-channel devices with Barrier A&B. (c) Hole and electron density distribution for different barriers. (d) Band diagram under p-GaN gate region for various barriers.

Fig. 4(a) shows the $I_D - V_{DS}$ characteristics of HV power devices. The gate to drain length (L_{GD}) of $10\mu m$ and the gate field plate (L_{fp}) of $5\mu m$ are used and shown in the inset of Fig.4(a). It is seen that V_{BV} increases by 32.5% when replacing Barrier A by Barriers B, C, and D. The larger $\Delta x_{b,p}$ and thicker $t_{b,p}$ contribute to higher V_{BV} , which means that the positive graded AlGaIn has a good prospect to improve the breakdown characteristics of GaN based power devices. Fig.4(b) shows the benchmark of V_{BV} as a function of specific on-resistance ($R_{ON,SP}$) of devices with barrier described in Table1. The figure

of merit (FOM) ($FOM = V_{BR}^2/R_{on,sp}$) is found to increase more than 3 times when Barrier A is replaced by Barrier D, reaching $2.33GV^2/\Omega.cm^2$ that is the best-in-class FOM predicted for the GaN/AlGaIn/GaN based epitaxial structure [12]. In addition, the breakdown electric field (E_C) is significantly improved in the device with Barrier D owing to the larger $t_{b,p}$ and maximum $\Delta x_{b,p}$ shown in the inset of Fig. 4(b).

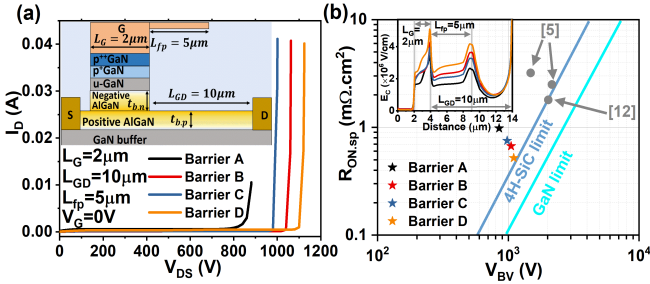


Fig.4: (a) V_{BS} in HV n-channel devices with different barrier layers at $L_{GD} = 10\mu m$, $L_{fp} = 5\mu m$ and $V_G = 0V$. (b) The $V_{BV} - R_{ON,SP}$ for HV power devices with different barriers compared with latest results [5][12]. The inset shows the comparison of critical electric field between various kinds of barriers.

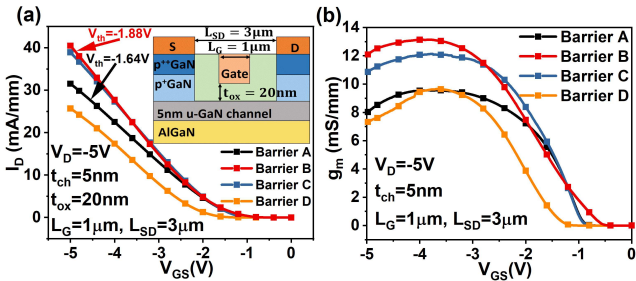


Fig.5: (a) $I_D - V_{GS}$ of p-channel devices with different barrier layers at $L_G = 1\mu m$, $L_{SD} = 3\mu m$ and $V_D = -5V$. (b) The related $g_m - V_{GS}$ curves.

Fig.5(a) reveals the transfer characteristics of p-channel devices with $L_G = 1\mu m$, $L_{SD} = 3\mu m$ and the gate oxide (t_{ox} , between gate and u-GaN channel) of 20nm shown in the inset of Fig.5(a). I_{ON} of Barriers B and C increases as compared to Barrier A owing to the widened 3DHG slab width in a negative graded AlGaIn displayed in Fig.3 (d). $|V_{th}|$ of Barrier B increases 14.6% as compared to Barrier A, due to the positive graded AlGaIn. A degradation of I_{ON} in p-channel device is observed with Barrier D, due to the limited spread of hole distribution shown

in Fig. 3(c). Fig.5 (b) illustrates that the negative graded AlGaIn can improve the transconductance (g_m) for p-channel devices due to the 3DHG across the channel and barrier layer as polarization “doping”.

Conclusion

We introduce a novel back-to-back graded AlGaIn, where the upper layer is negative graded AlGaIn whereas the lower is positive graded AlGaIn. For the n-channel device based on the p-GaN gate structure, the increase of I_{ON} and reduction of R_{ON} are realized by the positive graded AlGaIn. Moreover, n_e under the gate region is depleted and V_{th} is shifted to E-mode direction by Barriers B and C with thicker $t_{b,n}$ as the negatively graded AlGaIn is etched beyond the gate region. In addition, the positive AlGaIn leads to enhanced V_{BV} and critical electric field, which achieves a very high FOM of $2.33GV^2/\Omega.cm^2$ and makes the composite graded AlGaIn promising in high power applications. Furthermore, I_{ON} and g_m are both improved by the negative graded AlGaIn in p-channel devices without degradation to $|V_{th}|$.

References

- [1] Z. Zheng, W. Song, L. Zhang, S. Yang, J. Wei, and K. J. Chen, “Monolithically Integrated GaN Ring Oscillator Based on High-Performance Complementary Logic Inverters,” *IEEE Electron Device Lett.*, vol. 42, no. 1, pp. 26–29, Jan. 2021.
- [2] Z. Zheng *et al.*, “Gallium nitride-based complementary logic integrated circuits,” *Nat. Electron.*, vol. 4, no. 8, pp. 595–603, Aug. 2021.
- [3] J. Wei, G. Tang, R. Xie, and K. J. Chen, “GaN power IC technology on p-GaN gate HEMT platform,” *Japanese Journal of Applied Physics*, vol. 59, no. SG. Institute of Physics Publishing, 01-Apr-2020.
- [4] Z. Zheng *et al.*, “Enhancement-Mode GaN p-Channel MOSFETs for Power Integration,” in *Proceedings of the International Symposium on Power Semiconductor Devices and ICs*, 2020, vol. 2020-Sept, pp. 525–528.
- [5] J. G. Kim, C. Cho, E. Kim, J. S. Hwang, K. H. Park, and J. H. Lee, “High Breakdown Voltage and Low-Current Dispersion in AlGaIn/GaN HEMTs with High-Quality AlN Buffer Layer,” *IEEE Trans. Electron Devices*, vol. 68, no. 4, pp. 1513–1517, Apr. 2021.
- [6] H. Jiang, R. Zhu, Q. Lyu, and K. M. Lau, “High-Voltage p-GaN HEMTs with OFF-State Blocking Capability after Gate Breakdown,” *IEEE Electron Device Lett.*, vol. 40, no. 4, pp. 530–533, Apr. 2019.
- [7] J. Chen *et al.*, “A GaN Complementary FET Inverter with Excellent Noise Margins Monolithically Integrated with Power Gate-Injection HEMTs,” *IEEE Trans. Electron Devices*, vol. 69, no. 1, pp. 51–56, Jan. 2022.
- [8] N. Venkatesan, J. S. Moon, and P. Fay, “Electric Field Engineering in Graded-Channel GaN-Based HEMTs,” in *2021 IEEE BiCMOS and Compound Semiconductor Integrated Circuits and Technology Symposium, BCICTS 2021*, 2021.
- [9] P. M. Lytvyn *et al.*, “Polarization Effects in Graded AlGaIn Nanolayers Revealed by Current-Sensing and Kelvin Probe Microscopy,” *ACS Appl. Mater. Interfaces*, vol. 10, no. 7, pp. 6755–6763, Feb. 2018.
- [10] N. Chowdhury, Q. Xie, M. Yuan, K. Cheng, H. W. Then, and T. Palacios, “Regrowth-Free GaN-Based Complementary Logic on a Si Substrate,” *IEEE Electron Device Lett.*, vol. 41, no. 6, pp. 820–823, Jun. 2020.
- [11] H.-B. Do, J. Zhou, and M. M. De Souza, “Origins of the Schottky Barrier to a 2DHG in a Au/Ni/GaN/AlGaIn/GaN Heterostructure,” *ACS Appl. Electron. Mater.*, Sep. 2022.
- [12] J.-H. Lee *et al.*, “High Figure-of-Merit (V_{2BR}/Ron) AlGaIn/GaN Power HEMT With Periodically C-Doped GaN Buffer and AlGaIn Back Barrier,” *IEEE J. Electron Devices Soc.*, vol. 6, pp. 1179–1186, Oct. 2018.