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# Quantized conductance in hybrid split-gate arrays of superconducting quantum point contacts with semiconducting two-dimensional electron systems

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A quantum point contact (QPC)—a constriction in a semiconducting two-dimensional electron system with a quantized conductance—is a building block of novel spintronic and topological electronic circuits. QPCs can also be used as readout electronics, charge sensors, or switches in quantum nanocircuits. A short and impurity-free constriction with superconducting contacts is a Cooper-pair QPC analogue known as a superconducting quantum point contact (SQPC). The technological development of such quantum devices has been prolonged due to the challenges of maintaining their geometrical requirement and near-unity superconductor-semiconductor interface transparency. Here, we develop advanced nanofabrication, material and device engineering techniques and report on an innovative realization of nanoscale hybrid SQPC arrays with split gate technology in semiconducting 2D electron systems. We exploit the special gate tunability of the quantum wells, and demonstrate the first experimental observation of conductance quantization in hybrid InGaAs-Nb SQPCs. We observe reproducible quantized conductance at zero magnetic fields in multiple quantum nanodevices fabricated in a single chip and systematically investigate the quantum transport of SQPCs at low and high magnetic fields for their potential applications in quantum metrology, for extremely accurate voltage standards, and fault-tolerant quantum technologies.

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#### I. INTRODUCTION

A quantum point contact (QPC) is a small constriction defined in a two-dimensional-electron-gas (2DEG) system that exhibits quantized conductance. Generally, the constriction has width and length  $L_c$  both smaller than the mean free path. This particular shape, also known as the Sharvin point contact, was proposed to study the Fermi

Published by the American Physical Society under the terms of the Creative Commons Attribution 4.0 International license. Further distribution of this work must maintain attribution to the author(s) and the published article's title, journal citation, and DOI. surface in a metallic sample and has since been used to study scattering [1,2].

With the advent of 2DEG heterostructures and the need to investigate quantum transport, the QPC in a GaAs/AlGaAs heterostructure was developed, followed by the prediction of quantized conductance as multiples of the conductance quantum  $G = \sum_{n=1}^{N_c} 2e^2/h$  [3–9]. Since then, QPCs have become important tools for studying electron transport in condensed-matter systems and have found a wide range of applications in areas such as quantum nanoelectronics. Ever since investigations of the hybrid semiconductor-superconductor junction were initiated, a plethora of experimental and theoretical efforts have been dedicated to this field [10]. This was followed by the theoretical prediction of quantized conductance in hybrid systems [superconducting QPCs (SQPC)] [11]: the

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conductance of the hybrid field-effect SQPC is quantized, as in normal QPCs; however, the plateau height is different from that for a normal QPC, with a step height of  $2e^2/h$ . In perfect conditions, the conductance step height of SOPCs with a single superconductor-2DEG interface is predicted to be doubled (a value of  $4e^2/h$ ) due to the retroreflective property of the scattering (retro property of Andreev reflection) at the interface [11], and is related to the number of one-dimensional sub-bands in their constrictions. In such a single-interface system, the normal electron excitation incident from the 2DEG is reflected at the interface with a superconductor as hole excitation with identical momentum but opposite velocity. This means that every single reflected quasiparticle initially radiated from the hybrid junction will come back to it, causing the doubling of conductance in a single-interface superconductor-2DEG device [12]. In the case of a smooth and impurity-free superconducting constriction of length shorter than the coherence length  $L_c \ll \xi_0 = (\hbar \nu F / 2\pi \Delta_0)$ , the step height in conductance at zero temperature is dependent only on the bulk superconductor energy gap  $\Delta_0$  and is independent of the junction parameters [12,13]. However, the existence of disorder and roughness in the interfaces of real hybrid junctions, the device geometry, and fabrication errors may result in the suppression and reduction of conductance values [14]. Moreover, the conductance G as a function of contact width or Fermi energy of a single-interface hybrid QPC has also been predicted to have plateaus at half-integer multiples of  $4e^2/h$  if the superconductor is in a topologically nontrivial phase, but to have the usual integer multiples in the topologically trivial phase, sensitive to disorders [15]. Nevertheless, the

experimental exploration of quantized conductance values in hybrid SQPCs is limited to only a few studies on InAs-based 2DEGs with observed step heights that do not exactly follow the predicted theoretical values [12,16].

When a negative gate voltage is applied to a hybrid SQPC, the conductance oscillates due to the Fabry-Perot interference of quasiparticles [17]. By further application of negative gate voltage and increase of the absolute value of the gate voltage, the 2DEG underneath the split gates starts to pinch off. A one-dimensional sub-band will develop in the hybrid field-effect devices when the constriction length  $L_c$  becomes comparable to the 2DEG Fermi wavelength  $\lambda_F$  [18]. The number of sub-bands in a QPC should follow the relation  $2L_c/\lambda_F$  and can be modulated by the gate voltage. In the case of an SQPC or hybrid field-effect device under such conditions, two currents will be running through the constriction: (i) the superconducting current and (ii) the normal current. To observe the quantized supercurrent in hybrid devices, junctions with nanoscale dimensions of high-quality interfaces are needed as the magnitude of the quantized current is predicted to depend on junction parameters and barrier strength [12,18].

Here we report on a realization of quantum nanoelectronics circuit architecture by integration of an array of hybrid split-gate InGaAs-Nb SQPCs in a single chip. Moreover, we show that robust quantized conductance can be formed when the split-gate voltages of the SQPCs are swept to negative values. Finally, we discuss the response of quantized conductance to perpendicular magnetic fields for single-interface and double-interface SQPCs.

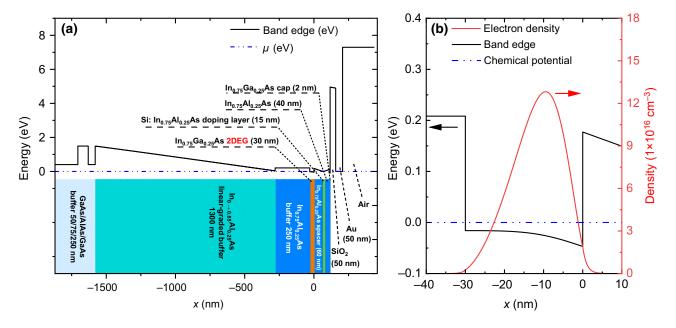


FIG. 1. (a) Band edge of the InGaAs-wafer layered structure calculated with use of NEXTNANO. (b) Enlarged view of the InGaAs/InAlAs quantum well. The red curve represents the electron density.

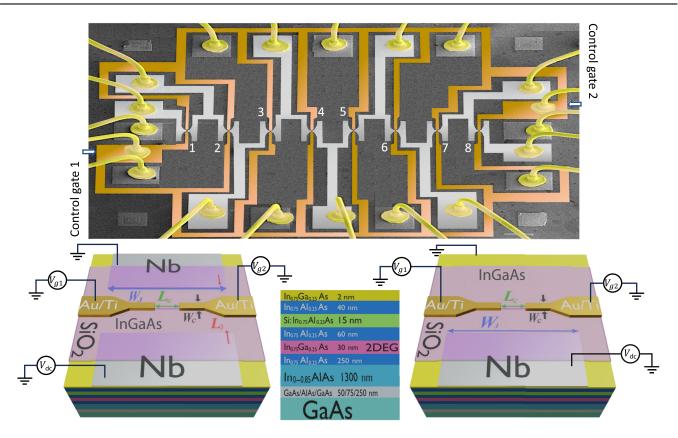


FIG. 2. Top: False-color scanning electron microscope image of the integrated hybrid SQPC chip with eight split-gate devices each controlled by two universal control gates (left and right). The Au leads are bright yellow, the Ti/Au gates are colored copper, and the Nb layer is colored silver. Bottom: Schematic demonstration of the split-gate SQPC double interface formed on an InGaAs heterostructure wafer with the circuit measurement configuration (left) and a single-interface SQPC (right). The SQPC geometrical parameters for a junction with width  $W_J$  (dark blue) and length  $L_J$  (dark red) and constriction width  $W_c$  (black) and length  $L_c$  (dark green) for an array of devices are shown in Table I. The top view of the hybrid split-gate SQPC double interface is shown in Fig. 7. The heterostructure wafer showing that the In<sub>0.75</sub>Ga<sub>0.25</sub>As 2DEG with 30-nm thickness is located approximately 120 nm below the surface is shown in the middle.

# II. WAFER GROWTH AND QUANTUM-WELL SIMULATION

The wafer was grown by molecular-beam epitaxy; the layered structure is shown in the bottom part of Fig. 1(a), in which the *x* direction is the growth direction. The 2DEG was grown on a 500-μm GaAs substrate starting with a GaAs/(50 nm)/AlAs/(70 nm)/GaAs(250 nm) buffer layer. On top of the buffer layer are a 1300-nm linear-graded InAlAs buffer layer, another InAlAs buffer layer (250 nm), and a 30-nm In<sub>0.75</sub>Ga<sub>0.25</sub>As quantum well (QW), which

TABLE I. The designed geometrical parameters of the eight hybrid split-gate SQPCs integrated into a single quantum chip.

SQPC parameter	1	2	3	4	5	6	7	8
$L_c$ (nm)	400	400	400	400	400	400	400	400
$W_c$ (nm)	400	300	200	100	100	100	100	100
$L_J (\mu m)$	1.4	1.4	1.4	1.4	1.4	1.4	1.4	3.2
$W_J$ ( $\mu$ m)	5	5	5	5	5	5	5	5

is a 2DEG with mobility  $\mu_e = 2.5 \times 10^5 \mathrm{cm}^2 \ \mathrm{V}^{-1} \ \mathrm{s}^{-1}$  and electron density  $n_s = 2.24 \times 10^{11} \mathrm{cm}^{-2}$  in the dark. The 2DEG is buried under a 60-nm  $\mathrm{In}_{0.75}\mathrm{Al}_{0.25}\mathrm{As}$  spacer, 15-nm  $\mathrm{In}_{0.75}\mathrm{Al}_{0.25}\mathrm{As}$  with n-type doped modulation, and another  $\mathrm{In}_{0.75}\mathrm{Al}_{0.25}\mathrm{As}$  spacer (45 nm), with a final 2-nm InGaAs cap to prevent oxidization. Figure 1 shows the wafer's conduction-band edge simulated with use of NEXTNANO (a self-consistent Poisson-Schrödinger solver) [19]. The band edge is calculated from the self-consistent Poisson equation.

The electrostatic potential is evaluated through the Poisson equation, and is subsequently fed into the Schrödinger equation. The resulting redistribution of electron density will further alter the potential. This iterative process is repeated until the convergency requirements are met and self-consistency is achieved. The final output is the band edges considering strain and quantum mechanics. Figure 1(b) shows an enlarged view of the 2DEG region, which is the band edge under the Fermi level. The InGaAs 2DEG layer is sandwiched between two InAlAs layers

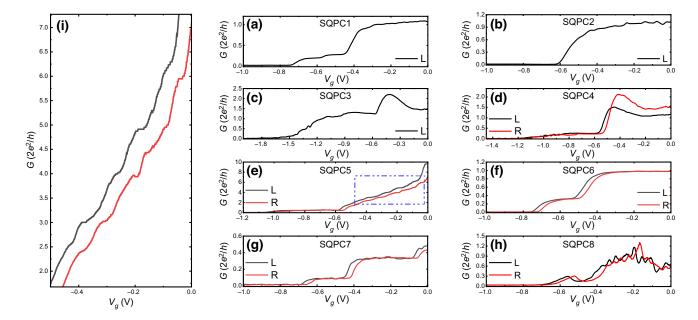


FIG. 3. Conductance as a function of electric field on the split gates for eight hybrid SQPCs integrated into a single chip measured at T = 280 mK, and B = 0 T: (a) SQPC1, (b) SQPC2, (c) SQPC3, (d) SQPC4, (e) SQPC5, (f) SQPC6, (g) SQPC7, and (h) SQPC8. (i) Enlarged view of the dashed-line area in (e), showing multiple plateaus. Here L and R correspond to gate-voltage sweep directions from 0 to negative voltages and back to 0 V, respectively.

with a greater band gap. Hence, a quantum well is formed in the InGaAs layer. Furthermore, the n-type silicon-doped modulation layer mentioned in the wafer description will tile the band gap towards a lower energy and bring the conduction-band edge down so that the quantum-well bottom is lower than the Fermi level. A triangular quantum well is formed below the Fermi level. In this sense, the 2DEG is formed with several sub-bands filled with electrons. The red curve in Fig. 1(b) represents the electron density calculated with NEXTNANO. The integrated electron density is around  $2.1 \times 10^{11}$  cm<sup>-3</sup>, which is consistent with a previously reported result [20].

# III. HYBRID SQPC CHIP FABRICATION AND SUBKELVIN CRYOGENIC MEASUREMENTS

Figure 2 (top) shows a false-color and scaled scanning-electron-microscope image of the integrated SQPC chip with eight split-gate devices (see Table I for their specific dimensions), each controlled by two universal control gates (gate 1 on the left and gate 2 on the right). Figure 2 (bottom) also shows a schematic of the hybrid SQPCs in the InGaAs 2DEG system with information about their dimensions, the semiconductor heterostructure, and the measurements of electrical circuit configurations. The detailed fabrication and cryogenic electrical characterization of large-scale hybrid circuits were discussed in our recent work [21].

The hybrid SQPCs are biased with a source-drain voltage  $V_{sd}$  and the split gates are separately controlled via voltage signals  $V_{g1}$  and  $V_{g2}$ . We designed our devices in a way to have specific parameters to investigate their conductance reproducibility and robustness for their suitability for future unconventional and topological superconductivity investigations; therefore, our focus in the present study is on the conductance properties of the SQPC devices [22– 27]. The split-gate SQPC parameters are labeled on the device surface in Fig. 2, with  $L_c$  and  $W_c$  as the constriction length and width, respectively, and  $L_J$  and  $W_J$  as the junction length and width, respectively. For a single-interface device (bottom right), there is an Ohmic contact on the other side of the Nb contact. The top view of the hybrid split-gate SQPC double interface is shown in Fig. 7 in the Appendix.

The experiment was performed in an Oxford Instruments  $^3$ He cryostat with a base temperature T of 280 mK. Figure 3 shows the measured conductance as a function of split-gate voltage at B=0 T for eight double-interface SQPCs integrated into a single chip. We observed stepwise changes (quantization of conductance) in the conductance of seven of the eight SQPCs on a single chip as a function of gate-voltage sweep from zero to negative voltages, here to  $V_g=-1$  V, shown with L, and back to 0 V, shown with R in Fig. 3. For example, clear multiple conductance plateaus were measured in SQPC5, and an enlarged view is shown in Fig. 3(i). Note that the contact resistance of the presented devices is larger than in our previous

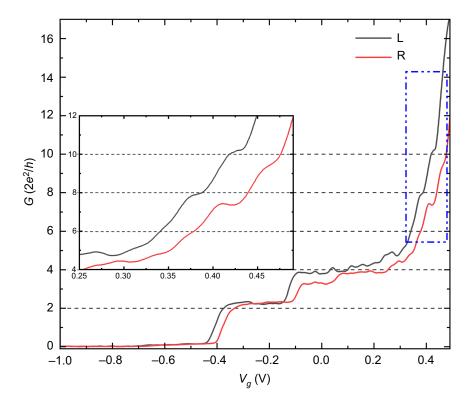


FIG. 4. Quantized conductance as a function of the electric field under the split gates for a hybrid Nb-In<sub>0.75</sub>Ga<sub>0.25</sub>As QW split-gate SQPC for two sweep directions: from right to left (*L*) and from left to right (*R*). It is clearly seen that quantized conductance attains a values of  $2 \times 2e^2/h$  for four observed plateaus for both gate-voltage sweep directions, confirming the formation of a high-quality interface between superconducting Nb and In<sub>0.75</sub>Ga<sub>0.25</sub>As QWs in the junction. The last two plateaus observed in the quantum transport measurements at T = 280 mK, and B = 0 T are enlarged and are plotted in the inset.

studies in hybrid superconductor-semiconductor devices [20,28,29].

There are a couple of facts that affected the quantum transport measurements of our SQPC arrays compared with a single normal QPC on a single chip: (i) Our devices are 2D planar junctions and have greater width, length, and constriction length  $L_c$  than conventional QPCs [8,28]. (ii) Down to the 2DEG area to make contact between 2DEG OWs and Nb (normal OPCs are usually formed on the surface of wafers). Some parts of QWs may be damaged or suppressed during the wet-etch nanofabrication processes. (iii) There might be a different etch depth and, therefore, different heights on each side of the junctions, so the transport might be asymmetric compared with that in normal QPCs, where a single narrow constriction of less than 100 nm is formed. (iv) There might be rough edges of the junction area underneath the split gates due to nanofabrication errors. (v) As the operating temperature of our devices is 280 mK, the observed conductance steps may be smeared out as the thermal energy, and the energy separation of the modes becomes comparable [3,30]. A few SQPC devices show resonance structures in their conductance steps (e.g., SQPC3, SQPC4, and SQPC8), likely due to quantum interference of quasiparticles [12–14,18].

Figure 4 shows the measured conductance as a function of split-gate voltage for a single-interface hybrid SQPC at B = 0 T. We observe a clear quantization of conductance as a function of split-gate electric field for two sweep directions: from left to right, and from right to left. We observe four plateaus with step heights of around  $2 \times 2e^2/h$ . The plateau  $6 \times 2e^2/h$  is slightly unclear. There could be different reasons for this, and further, in-depth investigations are required to understand the cause of this missing plateau. One reason could be due to the added characteristic of operation between the regions of positive and negative polarities for  $V_g$ . We further studied quantized conductance behavior in our SQPC devices by performing magnetic field-dependent conductance measurements for hybrid field-effect devices with either one interface (Nb-2DEG) or two interfaces (Nb-2DEG-Nb). The conductance of the hybrid field-effect SQPC devices is susceptible to magnetic fields [30,31]. The effect of the magnetic field on their conductance in superconducting states depends on the absolute value of gate voltage. When the gate voltage is relatively large, the current path will narrow depending on the constriction size. Still, if this path is within a dimension of the order of  $\lambda_F$ , the conductance may be less or may be insensitive to small magnetic fields.

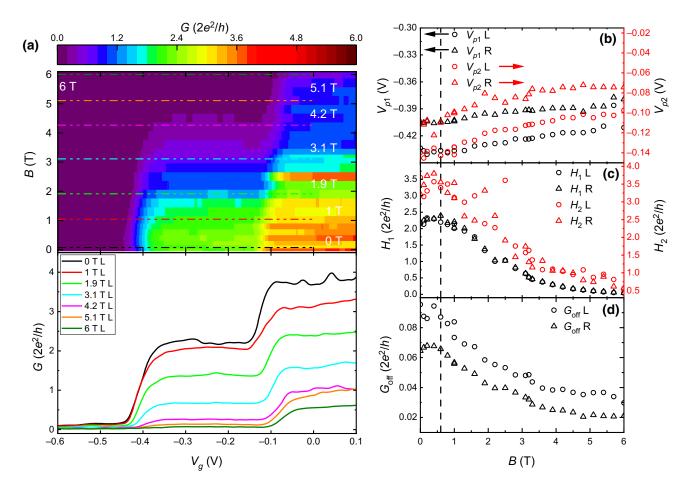


FIG. 5. (a) Colour-coded graph (top panel) showing the conductance as a function of the electric field on the split gates for a single-interface Nb-2DEG SQPC hybrid device at different perpendicular magnetic fields of up to 6 T at T = 280 mK. The line-cuts are shown in the bottom panel. There is only one sweep direction, from 0 to -1 V (denoted as L), shown and the sweep from -1 to 0 V (denoted as R) is shown in Fig. 8. A relatively good reproducibility rate is observed for all magnetic field strengths in this device. (b) Evolution of the conductance in the first and second steps as a function of applied perpendicular magnetic field for two gate-voltage sweep directions. (c) Conductance height for the first and second steps as a function of applied perpendicular magnetic field. (d) OFF-state conductance of the device as a function of the applied magnetic field for two gate-voltage sweep directions. The dashed line represents the border between the areas with a robust response with regard to the external magnetic fields (left) and the area with decreasing quantum conductance with regard to the applied magnetic fields (right).

Figure 5 shows the conductance versus gate-voltage sweeps of a hybrid field-effect SQPC with one Nb-2DEG interface at different perpendicular magnetic fields (see the caption for detailed information). The analysis in Figs. 5(b)-5(d) was derived from the conductance plateaus on the left, in which  $V_{p1}$  and  $V_{p2}$  are the pinch-off voltages of the first and second plateaus, respectively,  $H_1$  and  $H_2$  are the conductance heights measured from the first and second plateaus, and  $G_{\text{off}}$  is calculated from the average conductance when the hybrid SQPC is fully pinched off. We observe quantized conductance with step heights as large as approximately  $2 \times 2e^2/h$  at zero magnetic field, which is quite robust with regard to perpendicular magnetic fields B of up to 0.6 T. A monotonic decrease of conductance due to suppression of Andreev-reflection probability, as well as superconducting properties of Nb, is observed as the field strength increases to above 0.6 T [see Fig. 5(c)]. Above this point, the field magnitude is high enough to suppress the retro property of Andreev reflections, so the conductance height starts to decrease gradually. At around B=1.7 T, the device response becomes almost like that of normal QPCs. The pinch-off voltages for the first and second steps are plotted in Fig. 5(b), which shows a monotonic shift to higher fields (with relatively good reproducibility) for both directions of the split-gate voltage sweeps. The switching point where the hybrid SQPC switches from superconducting to an insulating state also moves to higher fields, as shown in Fig. 5(d).

Figure 6 presents the same measurements as discussed for Fig. 5 but for a hybrid split-gate SQPC device with two interfaces (Nb-2DEG-Nb). In this case, the induced superconductivity and Josephson coupling are dependent on the

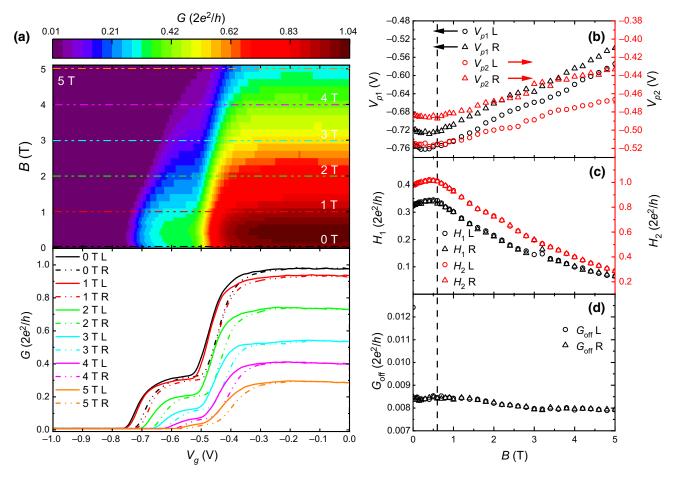


FIG. 6. Conductance as a function of electric field on the split gates for a hybrid Nb-2DEG-Nb SQPC at different perpendicular magnetic fields of up to 5 T and at T = 280 mK shown as a color-coded graph with the same analysis as discussed in the caption for Fig. 5.

distance between the two Nb contacts on each side of the In<sub>0.75</sub>Ga<sub>0.25</sub>As 2DEG in the hybrid SQPCs. If there is no Josephson coupling for long junctions ( $L_J$  much greater than the coherence length  $\xi$ ), a Nb-2DEG-Nb device can be considered as two Nb-2DEG devices in series, with conductance  $G_{\text{Nb-2DEG-Nb}} \approx (1/2)G_{\text{Nb-2DEG}}$  [32]. In this SQPC, quantized conductance with step heights as large as approximately  $0.32 \times 2e^2/h$  for the first plateau and approximately  $0.65 \times 2e^2/h$  for the second plateau at zero magnetic field are observed. The shift of the pinch-off voltage observed in double-interface SQPCs is much-more pronounced than that for a single-interface SQPC, which might be due to the magnetic field weakening-induced superconductivity or the Josephson coupling between two back-to-back In<sub>0.75</sub>Ga<sub>0.25</sub>As QW junctions [32–34]. As the magnetic field increases, the pinch-off voltage decreases due to weaker coupling between the two interfaces of the hybrid junction. The step height increases to approximately  $0.35 \times 2e^2/h$  and approximately  $0.69 \times 2e^2/h$  as the external magnetic field increases to 0.6 T, where the conductance starts to decrease. Current enhancement in

one-dimensional hybrid superconducting-semiconducting junctions has been observed and interpreted as of both non-topological [32] and topological [35] origin, but the actual cause of the effect is still under debate.

To the best of our knowledge, the observation of quantized-conductance enhancement under perpendicular (out-of-plane) magnetic fields has not been observed before in any hybrid quantum system. In addition to the origins mentioned above, weak antilocalization may also contribute to this effect. Elucidating the underlying aspects contributing to the magnetic field—dependent increase of current and conductance in hybrid SQPCs is a very interesting topic and strong motivation for future research work.

### IV. CONCLUSION

We have reported observation of quantized conductance in an array of hybrid split-gate SQPC devices based on the In<sub>0.75</sub>Ga<sub>0.25</sub>As 2DEG system and demonstrated a systematic experimental investigation of their quantum

transport at zero and high magnetic fields at millikelvin temperatures. We observed quantized conductance doubling in hybrid field-effect SQPC devices with single superconductor-semiconductor interfaces and found their robustness with regard to external perpendicular magnetic fields of up to 0.6 T. We further observed a clear transition from SQPC behavior to normal QPC behavior at high magnetic fields. By performing the same measurements on SQPC devices with two superconductor-semiconductor interfaces, we observed a stronger correlation between the pinch-off voltage and external magnetic fields, indicating that induced superconductivity, Josephson coupling, a split gate, and interface quality play important roles in SQPC behavior. Both single-interface and double-interface SQPC devices have slight conductance enhancement under the application of perpendicular magnetic fields; this observation requires further investigation in a large array of hybrid devices so the statistics and reproducibility of the data may help to understand the topological or nontopological origin of the effect. SQPCs offer unique quantum mechanical properties, such as accurate control of the flow of Cooper pairs, the quantization of superconducting order parameters, and the development of discrete energy levels. This allows the application of SQPCs in quantum metrology for extremely precise and stable voltage standards and for the development of cryogenic quantum nanoelectronics circuits and processors with ultrahigh sensitivity and robustness. Moreover, the proposed hybrid quantum circuit architecture may be implemented to investigate unconventional and topological superconductivity in a large array of coupled artificial hybrid devices for their potential applications in fault-tolerant topological quantum technology.

The data that support the findings of this study are available from the corresponding author upon reasonable request.

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## **APPENDIX**

In this section, we elaborate more the design and cryogenic measurements of the hybrid split-gate SQPC devices. Fig. 7 shows the top view of a hybrid SQPC double interface shown in Fig. 2. The color coded graph and line-cuts showing the conductance as a function of electric field on the split gates for a single interface Nb-2DEG SQPC hybrid device at different perpendicular magnetic

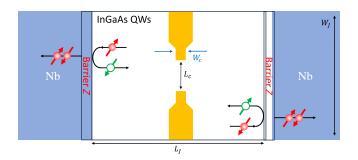


FIG. 7. Top view schematic of the SQPC-device structure showing shaded regions that represent a possible potential barrier at the Nb-InGaAs 2DEG interfaces, with Z representing the barrier height (strength). The junction width  $W_J$  and length  $L_J$  as well as the constriction width  $W_c$  and length  $L_c$  are defined accordingly. Andreev reflection is demonstrated on both sides of the Nb-InGaAs 2DEG interfaces, where an electron (red) is retroreflected as a hole (green), and a Cooper pair is formed on the Nb side.

fields up to B = 6 T, at T = 280 mK are shown in Fig. 8. Here, R in the legend denotes one sweep direction from -1 V to 0.

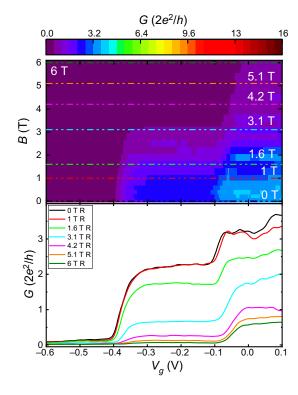


FIG. 8. Conductance as a function of electric field on the split gates for a single-interface Nb-In<sub>0.75</sub>Ga<sub>0.25</sub>As QW SQPC device at different magnetic fields of up to 6 T and at T= 280 mK shown as a color-coded graph at the top, where the line-cuts are shown at the bottom. Only one sweep direction is shown, -1 to 0 V (denoted as R). Compared with Fig. 5, relatively good reproducibility is observed for all magnetic field strengths in our hybrid SQPC nanodevices.

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