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Edge Acceleration for Machine Learning-based Motion Artifact Detection on fNIRS Dataset

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ABSTRACT

Machine Learning has potential applications across a wide spectrum of devices. However, current approaches for domain-specific accelerators have encountered difficulties in satisfying the most recent computational demands for machine learning applications. This work aims to create an adaptive acceleration framework for fNIRS motion artefact detection, which will be specifically designed for wearable devices. We evaluate the performance of the SVM classifier that has been implemented using SYCL on our fNIRS dataset across diverse devices and discuss the potential to accelerate more advanced motion artefact classifiers at the edge.

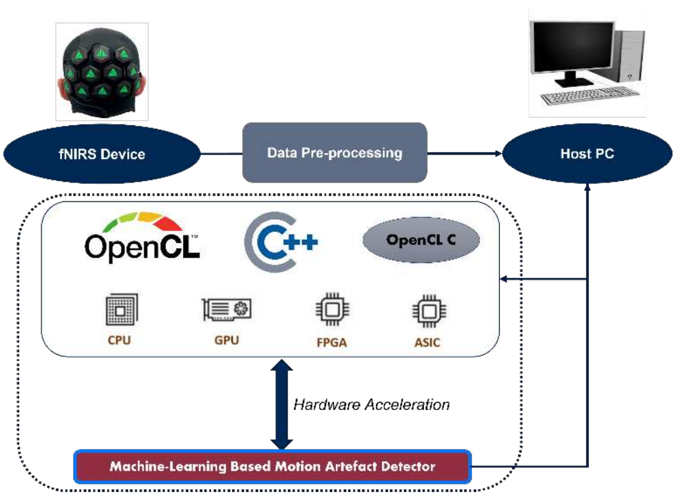

Figure 1: Overall design of the proposed real-time motion-artefact detection platform

The implementation of SVM with the ComputeCpp design flow is based on their project SYCL-ML . Their SVM implementation is properly designed to fit the MNIST dataset. The input dataset is firstly applied to Principal Component Analysis (PCA) in order to increase the training speed and accuracy. Then the data is fed to the classifier and performs the training process. However, the training function in this implementation is optimised for multi-class classification problems. The number of training iterations is correlated with the number of categories.

The confusion matrix presented in Table 1 after one epoch training, generated through the utilisation of OneDAL-SVM on the testing dataset, demonstrates the ability to accurately identify motion artefacts in fNIRS time series. However, the high number of false positives may result in an excessive intervention on the original fNIRS signals, potentially leading to a loss of information. In this study, the utilised version of OneDAL example and DPCPP compiler is 2023.0.0.

Table 1: Confusion Matrix of OneDAL-SVM result on fNIRS testing dataset

		Actual Values	
		Positive	Negative
Predicted Values	Positive	1418106	133765
	Negative	2186	13677
Sensitivity		0.998	

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Precision	0.913
Recall	0.888
F1 Score	0.986

Table 2 shows the processing speed on different hardware. The processing speed is calculated with the function 'high_resolution_clock' in 'chrono' header in microseconds and shown in the table in seconds. The data demonstrates that the GPU exhibits significantly enhanced processing speed in comparison to both the CPU and FPGA emulator. Although the processing speed of the CPU and FPGA emulator is similar, the FPGA emulator experiences a performance loss due to its simulation by the CPU.

Table 2: Training and inference speed on different hardware with OneDAL-SVM

	Training	Inference
CPU	100.13s	10.10s
GPU	32.20s	4.62s
FPGA Emulator	112.01s	11.31s

2 Conclusion

In this paper we have studied the possibility of building a heterogeneity- aware tool chain on machine learning based motion detection on fNIRS dataset. The results of our study indicate that the processing speed can be augmented by a factor of two by utilizing a GPU in comparison to utilizing a CPU and FPGA emulator. We have demonstrated the possibility of compilers across multiple platforms, yet it can be of interest also in other heterogeneous platforms such as neuromorphic memristors. We have shown how the approximation data conversation strategies are computationally plausible. In the Future, multiple types of machine learning techniques, such as VGG-16, U-net will be tested on heterogeneous platforms.

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