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ORIGINAL RESEARCH

Arbitrarily fast delayed signal cancellation PLL for grid-integration of renewable energy sources

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Abstract

Integrating renewable energy sources into an unbalanced distribution network requires fast and accurate extraction of fundamental frequency positive- and negative-sequence components from the unbalanced three-phase grid voltage signals. For this purpose, various methods are already available in the literature. Out of them, delayed signal cancellation (DSC) is prevalent. Conventional DSC can separate the sequence components using a quarter-cycle delay. Fast DSC tools can achieve the same with less than a quarter-cycle delay. However, neither conventional nor fast DSC can handle DC offset without requiring additional delayed signals. This article addresses this issue by proposing a modified DSC to estimate the sequence components with DC offset rejection and having arbitrarily fast convergence speed, that is, low memory requirement. Two equidistant delayed samples of the measured grid voltages/currents are required to implement the proposed technique and can easily be applied in a phase-locked loop (PLL). Comparative experimental results demonstrate the suitability of the proposed approach over other DSC methods.

1 | INTRODUCTION

In order to mitigate the negative impact of burning fossil fuels, renewable energy sources (RES) are becoming very popular worldwide. Many RES are now price competitive and/or cheaper compared to conventional gas/coal-fired electricity production. This has contributed to a broader societal acceptance of RES and also led to the large-scale integration of RES into the grid. RES, such as solar or wind, are interfaced with the power grid through power electronic converters. When the RES-powered grid-connected converter (GCC) operates in synchronization with the grid, maximum power transfer can be ensured. To achieve this, the control system of GCC requires the information on the grid, for example, phase, frequency, and amplitude in real-time. This process is commonly known as grid-synchronization [1–9], typically performed by the phase-locked loop (PLL).

RES are usually connected to the grid at the distribution network level. Due to the presence of single- and three-phase loads, per-phase loading of low-voltage distribution substations are not identical. This uneven connection of particularly single-phase loads causes phase unbalance at the distribution network level [10–15]. Integrating RES into the unbalanced distribution network is challenging due to the simultaneous presence of fundamental frequency positive-sequences (FFPS) and fundamental frequency negative-sequences (FFNS) components in the grid voltage. Fast and accurate estimation of these components is essential for grid fault-tolerant control of RES-interfaced power converters. Typical examples are fault-ride through (FRT) control [16–18], voltage compensation for sensitive loads [19], and PLL implementation [20–22], to name a few.

Delayed signal cancellation (DSC) [23, 24] is a popular method in the literature to estimate FFPS and FFNS components from unbiased and unbalanced three-phase signals. This technique uses quarter-cycle delayed samples of the measured grid voltage/currents to estimate the sequence components. A modified DSC operation with fast convergence is proposed in [25–28] to reduce the estimation delay. An equivalent version of this approach with the same delay but lower computational complexity is proposed in [29]. However, these modified DSCs cannot reject DC offset without using an additional half-cycle DSC operation. A key limitation of [28] and [29] is that this approach can work only when no DC offset is presented in

the grid. DC offset may appear due to a variety of reasons, for example, analog to digital conversion of measured signals [30], grid fault [31], current transformer saturation, geomagnetically induced currents [32] etc. In the presence of DC offset, the output of PLL has steady-state ripple, which causes undesirable reactive power injection to the grid. In addition, active power oscillation can also be observed, which degrades the power quality [33]. As such, mitigation of this DC offset is essential to ensure high-performance control of grid-connected converters.

To reject measurement bias, that is, DC offset, cascaded DSC (CDSC) is proposed in [23, 29]. In CDSC, an additional delayed signal cancellation block with a half-cycle delay is considered to reject the DC offset, increasing the overall estimation delay and augmenting the required memory to store the delayed samples. An improved DSC operation is presented in this work to overcome this issue. Our approach uses two equidistantly delayed samples of the measured signals to estimate the sequence components with DC offset rejection. The proposed solution is arbitrarily fast and has low computational complexity. Unlike other two-delayed-samples-based FFPS sequence component estimation techniques [34], our solution is generic since it can estimate FFPS and FFNS components. In addition, our method can reject DC offset, unlike [34].

Like various variants of conventional DSCs [28, 29], the proposed modified DSC is also affected by voltage/current harmonics. Additional pre-loop and/or in-loop filtering stages or cascaded DSCs [21, 23] have to be implemented. This issue is addressed by integrating our method into a CDSC-PLL where the proposed technique replaces the DC offset and FFNS rejection DSC blocks. Reducing the memory requirement, and, consequently making the convergence time faster for DSC-PLL, is this work's main contribution. Compared to existing DSC-PLLs [23, 28], the proposed method can have up to 26% lower memory requirement, which makes the technique very suitable for real-time implementation in low-cost embedded devices.

The rest of this article is organized as follows: development of the proposed estimator is given in Section 2, experimental results are provided in Section 3, and finally, concluding remarks are given in Section 4.

2 | ESTIMATOR DESIGN

An overview of solar energy-powered GCC, including the control system block, is given in Figure 1. As shown in Figure 1, grid-synchronization through PLL plays an important role in the outer voltage controller. Here, PLL separates the sequence components and extracts the grid voltage phase for the in-phase operation of the GCC with the grid. It is to be noted here that in this work, the focus is on PLL only, and Figure 1 is used solely to contextualize the location of PLL in the converter control system. To facilitate this, let us consider the unbalanced three-phase grid voltages with measurement offset in the stationary

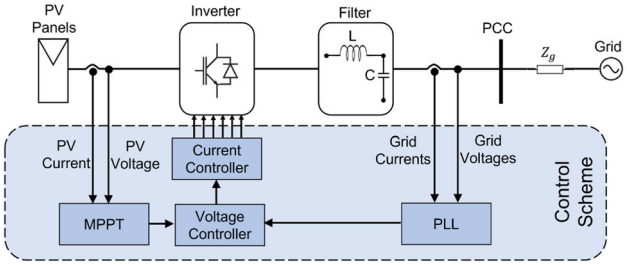

FIGURE 1 An overview of a general grid-connected converter control system with PLL-based grid-synchronization method

reference frame as given by:

$$v_\alpha(t) = V_{\alpha 0} + V^+ \cos(\omega t + \delta^+) + V^- \cos(\omega t + \delta^-), \quad (1)$$

$$v_\beta(t) = V_{\beta 0} + V^+ \sin(\omega t + \delta^+) - V^- \sin(\omega t + \delta^-), \quad (2)$$

where the superscripts $+$ and $-$ denote the positive and negative sequences, $\theta^\pm = \omega t + \delta^\pm$ are the total phase, $V^\pm, \omega$, $\delta^\pm$, $V_{\alpha 0}$, and $V_{\beta 0}$ represent the amplitude, angular frequency, phase angle, and DC offsets in phases α and β, respectively. The extraction of the FFPS components $v_\alpha^+ = V^+ \cos(\theta^+)$, $v_\beta^+ = V^+ \sin(\theta^+)$; of the FFNS components $v_\alpha^- = V^- \cos(\theta^-), v_\beta^- = V^- \sin(\theta^-)$, and of the DC offsets $V_{\alpha 0}, V_{\beta 0}$ are considered in this article. In the sequel, the time-dependence of a signal is often not explicitly stated for convenience. Moreover, continuous- and discrete-time signals may be mixed for brevity.

2.1 | Delayed signal cancellation based sequence separation

Let us consider the voltage vector of (1), (2) defined as $\vec{v}_{\alpha\beta} = v_\alpha + jv_\beta$. Then, by applying the DSC method, the FFPS and FFNS sequences can be estimated as [35]:

$$\hat{\vec{v}}^+_{\alpha\beta}(t) = \frac{1}{2}\left(\vec{v}_{\alpha\beta}(t) + j\vec{v}_{\alpha\beta}\left(t - \frac{T}{n}\right)\right), \quad (3)$$

$$\hat{\vec{v}}^-_{\alpha\beta}(t) = \frac{1}{2}\left(\vec{v}_{\alpha\beta}(t) - j\vec{v}_{\alpha\beta}\left(t - \frac{T}{n}\right)\right), \quad (4)$$

where T is the nominal signal period and $n = 4$ is the delay factor. This delay factor represents a quarter-cycle delay. However, this delay can not block the DC offset. Another DSC operation with $n = 2$ needs to be connected in series ([23]) to block the DC offset. As such, the total delay of sequence separation operation reaches three-quarters of a cycle. To reduce the quarter-cycle delay of sequence separation in the unbiased measurement case, that is, without any DC offset, enhanced DSC is proposed in [28], requiring less than a quarter-cycle delay. Any arbitrary value of $n < 4$ can be used for sequence

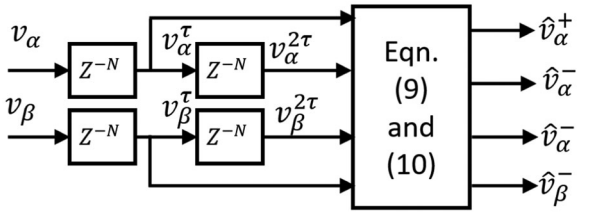

FIGURE 2 Proposed arbitrarily fast modified DSC method

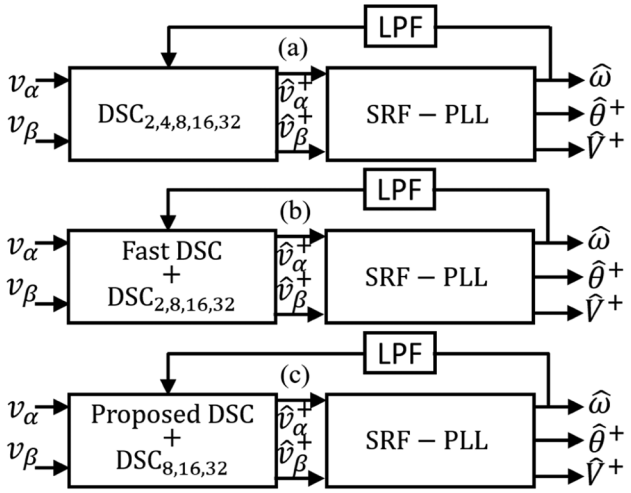

FIGURE 3 DSC-based PLL implementations: (a) conventional CDSC-PLL; (b) fast CDSC-PLL; and (c) proposed method

separation, making this method arbitrarily fast. A simplified version of this tool is proposed in [29]. However, it still requires another DSC operation in-series with $n = 2$. So, the total delay is less than three-quarters of a cycle but more than half-cycle of the signal period. Higher memory requirements and slow convergence issues are addressed below through our technique.

2.2 | Proposed method

To facilitate the calculations, let us write $v_\alpha^\tau = v_\alpha(t-\tau)$, $v_\alpha^{2\tau} = v_\alpha(t-2\tau)$, $v_\beta^\tau = v_\beta(t-\tau)$ and $v_\beta^{2\tau} = v_\beta(t-2\tau)$, where the time delay $\tau = NT_s$ with N being the number of delayed samples and T_s the sampling time. Then, the grid voltage (1), (2) and its two equidistant delayed samples v_α^τ, $v_\alpha^{2\tau}$, v_β^τ and $v_\beta^{2\tau}$ are given by:

$$v_\alpha^\tau(t) = V_{\alpha 0} + \left(V^+\cos\left(\theta^+\right) + V^-\cos\left(\theta^-\right)\right)\cos\left(\phi_\tau\right) + \left(V^+\sin\left(\theta^+\right) + V^-\sin\left(\theta^-\right)\right)\sin\left(\phi_\tau\right), \tag{5a}$$

$$v_\alpha^{2\tau}(t) = V_{\alpha 0} + \left(V^+\cos\left(\theta^+\right) + V^-\cos\left(\theta^-\right)\right)\cos\left(2\phi_\tau\right) + \left(V^+\sin\left(\theta^+\right) + V^-\sin\left(\theta^-\right)\right)\sin\left(2\phi_\tau\right), \tag{5b}$$

$$v_\beta^\tau(t) = V_{\beta 0} + \left(V^+\sin\left(\theta^+\right) - V^-\sin\left(\theta^-\right)\right)\cos\left(\phi_\tau\right) + \left(V^-\cos\left(\theta^-\right) - V^+\cos\left(\theta^+\right)\right)\sin\left(\phi_\tau\right), \tag{6a}$$

$$v_\beta^{2\tau}(t) = V_{\beta 0} + \left(V^+\sin\left(\theta^+\right) - V^-\sin\left(\theta^-\right)\right)\cos\left(2\phi_\tau\right) + \left(V^-\cos\left(\theta^-\right) - V^+\cos\left(\theta^+\right)\right)\sin\left(2\phi_\tau\right), \tag{6b}$$

where $\phi_\tau = \omega\tau$. Then, the following algebraic relationship between the sequence components, DC offset, measured voltages, and its two equidistant delayed samples can be obtained as:

$$\boldsymbol{v} = \boldsymbol{\Phi}\boldsymbol{\Omega}, \tag{7}$$

where

$$\boldsymbol{v} = \begin{bmatrix} v_\alpha & v_\beta & v_\alpha^\tau & v_\beta^\tau & v_\alpha^{2\tau} & v_\beta^{2\tau} \end{bmatrix}^T,$$

$$\boldsymbol{\Omega} = \begin{bmatrix} V_{\alpha 0} & v_\alpha^+ & v_\alpha^- & V_{\beta 0} & v_\beta^+ & v_\beta^- \end{bmatrix}^T,$$

$$\boldsymbol{\Phi} = \begin{bmatrix} 1 & 1 & 1 & 0 & 0 & 0 \\ 0 & 0 & 0 & 1 & 1 & -1 \\ 1 & c_\tau & c_\tau & 0 & s_\tau & s_\tau \\ 0 & -s_\tau & s_\tau & 1 & c_\tau & -c_\tau \\ 1 & c_{2\tau} & c_{2\tau} & 0 & s_{2\tau} & s_{2\tau} \\ 0 & -s_{2\tau} & s_{2\tau} & 1 & c_{2\tau} & -c_{2\tau} \end{bmatrix},$$

$c_\tau = \cos(\phi_\tau)$, $c_{2\tau} = \cos(2\phi_\tau)$, $s_\tau = \sin(\phi_\tau)$, and $s_{2\tau} = \sin(2\phi_\tau)$. From (7), $\boldsymbol{\Omega}$ can be estimated as follows:

$$\hat{\boldsymbol{\Omega}} = \boldsymbol{\Phi}^{-1}\boldsymbol{v}, \tag{8}$$

where $\hat{\cdot}$ indicates estimated value and

$$\Phi^{-1} = \begin{bmatrix} \frac{1}{2(1-c_\tau)} & 0 & \frac{c_\tau}{c_\tau - 1} & 0 & \frac{1}{2(1-c_\tau)} & 0 \\ \frac{1+c_\tau - c_\tau^2 - 2c_\tau^3}{2\left(1-c_\tau^2\right)} & \frac{1+c_\tau - 2c_\tau^2}{2s_\tau} & \frac{2c_\tau^2 - 1}{2(1-c_\tau)} & \frac{1-2s_\tau^2}{2s_\tau} & \frac{s_\tau^2 - 1}{2s_\tau^2} & -\frac{c_\tau}{2s_\tau} \\ \frac{c_\tau\left(2+c_\tau - 2c_\tau^2\right)}{2\left(c_\tau^2 - 1\right)} & \frac{-\left(c_\tau - 2c_\tau^2 + 1\right)}{2s_\tau} & \frac{1+2c_\tau - 2c_\tau^2}{2(1-c_\tau)} & \frac{2s_\tau^2 - 1}{2s_\tau} & \frac{1+c_\tau - c_\tau^2}{2\left(c_\tau^2 - 1\right)} & \frac{c_\tau}{2s_\tau} \\ \frac{1+2c_\tau}{2s_\tau} & 1 & \frac{-(1+c_\tau)}{s_\tau} & 0 & \frac{1}{2s_\tau} & 0 \\ \frac{-c_\tau(1+2c_\tau)}{2s_\tau} & \frac{1}{2} - c_\tau & \frac{c_\tau(1+c_\tau)}{s_\tau} & c_\tau & -\frac{c_\tau}{2s_\tau} & -\frac{1}{2} \\ \frac{-\left(1+c_\tau - 2c_\tau^2\right)}{2s_\tau} & c_\tau - \frac{1}{2} & s_\tau & -c_\tau & \frac{c_\tau - 1}{2s_\tau} & \frac{1}{2} \end{bmatrix}.$$

By simplifying (8), the sequences can be found as:

$$\widehat{v_\alpha^{\pm}} = \frac{1}{\gamma}\Big(2s_\tau c_\tau\left(v_\alpha - v_\alpha^\tau\right) \pm \left(1-2s_\tau^2\right)\left(v_\beta - v_\beta^\tau\right) \pm c_\tau\left(v_\beta^{2\tau} - v_\beta\right) \pm \left(v_\beta^\tau - v_\beta^{2\tau}\right) + s_\tau\left(v_\alpha^{2\tau} - v_\alpha\right)\Big), \quad (9)$$

$$\widehat{v_\beta^{\pm}} = \frac{1}{\gamma}\Big(\pm 2s_\tau c_\tau\left(v_\beta - v_\beta^\tau\right) + \left(1-2s_\tau^2\right)\left(v_\alpha^\tau - v_\alpha\right) c_\tau\left(v_\alpha - v_\alpha^{2\tau}\right) + \left(v_\alpha^{2\tau} - v_\alpha^\tau\right) \pm s_\tau\left(v_\beta^{2\tau} - v_\beta\right)\Big), \quad (10)$$

where $\gamma = 4s_\tau(c_\tau - 1)$. The presented sequence separation equations require few arithmetic operations and are very simple to implement in real-time. As shown in (9) and (10), two trigonometric operations are required to implement the equations. The implementation block diagram of the proposed technique is given in Figure 2.

2.3 | Application to phase-locked loop

Sequence separation formulas, as developed in Section 2.2, require the information on actual grid frequency. To obtain the actual grid frequency, CDSC-PLL [23] can be a suitable choice. An overview of the CDSC-PLL is given in Figure 3a. For more details about this PLL, the interested reader may consult [23, 36] and the references therein. In this approach, several DSC blocks are cascaded to eliminate the effect of harmonics and DC offset. Out of the five different DSC blocks, DSC_2 is used to eliminate the effect of DC offset, while DSC_4 is used to extract the FFPS component. These two blocks can be replaced by our method while the other DSC blocks are used as it is. CDSC-PLL with the proposed sequence extraction formulas is shown in Figure 3c. Directly using the estimated frequency in the DSC blocks can cause instability. A low-pass filter (LPF) is added to ensure stability and to avoid any algebraic loop.

3 | RESULTS AND DISCUSSIONS

An overview of the experimental setup used in this work is given in Figure 4. In this setup, a dSPACE 1104 board is used to generate the grid voltage signals. This signal is then passed through digital-to-analog converters (DAC). A Texas Instrument C2000 F28379D digital signal processor (DSP) is used for the practical implementation of the algorithms. These algorithms were exported from Matlab/Simulink using code generation. A sampling frequency of 16 kHz is considered. Experimental results are exported to Matlab for plotting purposes. As comparative techniques, we have selected CDSC-PLL [23] (Figure 3a) and Fast DSC-PLL (FDSC-PLL) (Figure 3b). In the CDSC-PLL, five DSC blocks are used in series namely DSC_2, DSC_4, DSC_8, DSC_{16}, and DSC_{32}. In FDSC-PLL, only the DSC_4 operator of CDSC-PLL is replaced by the fast DSC method proposed in [28, 29], whereas the remained DSC blocks of CDSC-PLL are kept as it is. Similarly, in the proposed method, only the DSC_2 and DSC_4 blocks are replaced by the developed single DSC block. Parameters of the synchronous reference frame (SRF)-PLL [37] are selected the same for all three techniques. Cut-off frequency of the low-pass filter is selected as 60Hz. To imple-

FIGURE 4 Overview of the experimental setup

TABLE 1 Comparative time-domain performance summary

Performance indicators ⇓	CDSC	FDSC	Proposed
Frequency settling time (±0.1Hz) (s)	0.94	0.0914	0.0884
Frequency peak overshoot (Hz)	0.35	0.26	0.18
Phase error settling time (±0.2°) (s)	0.164	0.15	0.115
Peak phase error (°)	7.68	6.07	4.62
FFPS settling time (±0.02 p.u.)	0.0168	0.016	0.0133
FFNS settling time (±0.02 p.u.)	0.0172	0.0152	0.0139
Total delay	$\frac{31T}{32}$	$\frac{27T}{32}$	$\frac{23T}{32}$

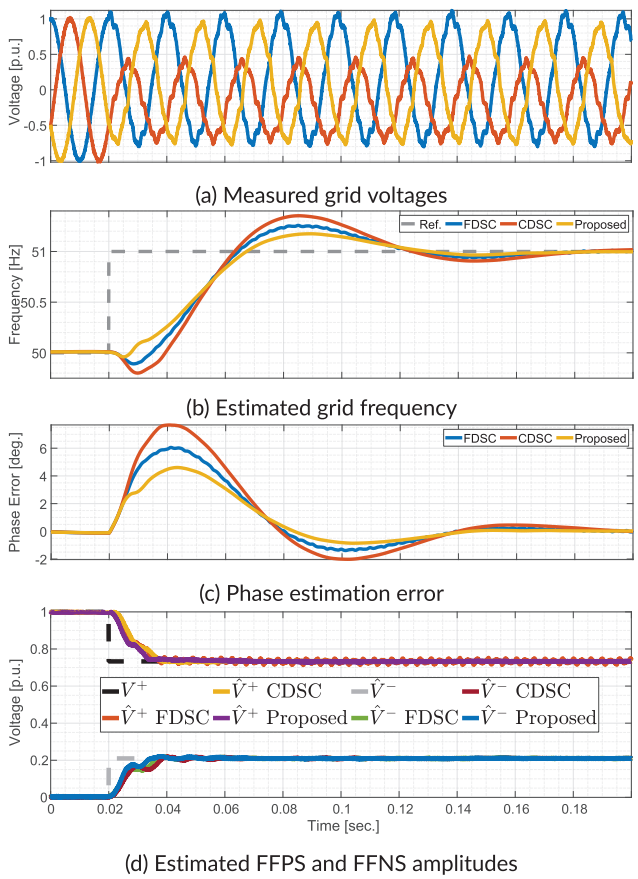

FIGURE 5 Comparative experimental results

ment the proposed DSC method, $\tau = T/4$ is considered while $\tau = T/8$ is considered for the fast DSC method. Total delays of the comparative techniques are given in Table 1.

For experimental validation, initially, the grid was balanced. At $t = 0.02$ s, the grid became unbalanced, distorted, and biased. The considered unbalanced grid is composed of $\vec{v}^{+1} = 0.733\angle 0°, \vec{v}^{-1} = 0.21\angle -45°, \vec{v}^{-5} = 0.031\angle 45°$, $\vec{v}^{+7} = 0.028\angle -45°, \vec{v}^{-11} = 0.024\angle 180°, \vec{v}^{+13} = 0.015\angle -180°$, and $\vec{v}^{+30\text{Hz}} = 0.01\angle 90°$. In addition, DC offsets of 0.15p.u., −0.15p.u, and 0.1p.u. are added to the first, second and third phases of the three-phase voltage signals, respectively. The experimental signal had a signal-to-noise ratio of 38dB. Experimental results are given in Figure 5. In this test, frequency step change of +1Hz is considered. Despite using the same loop-filter gain for all PLLs, the proposed method has a faster convergence with lower peak overshoot for the frequency estimation, as shown in Figure 5a. Similar performance can be observed for the phase estimation error as well. This is particularly important as the estimated phase is used for reference fame transformation in the control system of grid-connected converter. So, a fast convergence would imply improved stability margin, facilitating a large-scale integration of RES in the power grid. The summary of the results is tabulated in Table 1. Results show that the proposed method has the fastest convergence time and the lowest peak overshoot in all indicators. The estimated FFPS and FFNS amplitudes in Figure 5d show that fast DSC is sensitive to noise and harmonics. However, despite using lower memory than the conventional CDSC method, the steady-state performance of our method is similar to CDSC. So, it can be claimed that the proposed method can help achieve a faster convergence time without sacrificing the steady-state accuracy. The total memory requirement of the proposed method can be reduced further if $\tau = T/8$ is considered. However, this value amplifies the measurement noise. If the signal is fairly clean and undistorted, we recommend this value. Otherwise, $\tau = T/4$ can be a suitable choice in the presence of noise and harmonics.

4 | CONCLUSION AND FUTURE WORKS

An enhanced delayed signal cancellation method was proposed in this article for the grid-integration of distributed RES. The developed method can easily be integrated into the conventional cascaded delayed signal cancellation phase-locked loop, making it suitable as a grid-synchronization tool for grid-connected converters. The developed approach can estimate FFPS and FFNS components with a fast settling time. The proposed technique can estimate the signals within a fraction of the delay compared to the conventional counterpart being arbitrarily fast. However, a judicious choice must be made for the practical implementation between the convergence time, noise sensitivity, and peak overshoot. Experimental results showed that a total delay of half-cycle is a good choice for the proposed DSC technique in a distorted grid with noisy measurements. The method proposed in this work will ensure a fast and accurate integration of RES into an unbalanced distribution grid.

PLL is an integral part of the grid-connected converter system. Typically, a small-signal model of PLL is required for comprehensive tuning and stability analysis of the converter control system. Developing a small-signal model of the PLL can be considered as a future work. There is a growing interest in the power system community on studying the harmonic distortion caused by supraharmonics (i.e. between 2kHz and 150kHz). Sensitivity analysis of the proposed PLL to suprahramonics can also be considered as future work.

AUTHOR CONTRIBUTIONS

Hafiz Ahmed (GE): Conceptualization, formal analysis, funding acquisition, methodology, software, validation, visualization,

writing - original draft, writing - review and editing. Rosane Ushirobira: Conceptualization, formal analysis, methodology, supervision, writing - original draft, writing - review and editing. Denis Efimov: Conceptualization, formal analysis, methodology, supervision, writing - original draft, writing - review and editing.

CONFLICT OF INTEREST

The authors have declared no conflict of interest.

DATA AVAILABILITY STATEMENT

The data that support the findings of this study are available from the corresponding author upon reasonable request.

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