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Sensor Applications

Single-Phase SOGI-PLLs For Fast and Accurate Frequency Ramp Tracking

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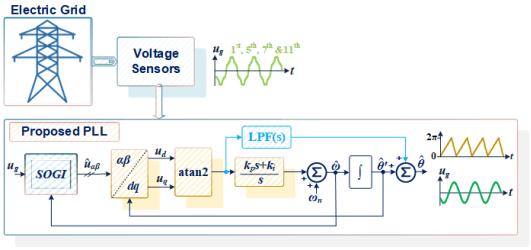
Abstract—This letter explores accurate frequency and phase tracking for single-phase power grid applications. While the conventional type-2 phase-locked loop (PLL) offers fast dynamic response, it exhibits steady-state tracking error in the presence of frequency ramp caused by rapid changes in power generation and/or consumption. The higher-order type-3 PLL can address this, albeit with slower dynamics. Our contribution introduces quasi-type-2 PLLs, which excel at accurate phase tracking during frequency ramps, outperforming conventional type-2 PLLs and maintaining a faster dynamic response than type-3 counterparts. This enhancement relies on linear phase error forward compensation. Experimental validation across four test scenarios underscores the superiority of our proposed PLLs over traditional methods. Achieving zero tracking error during frequency ramps, our methods prove useful for controlling grid-connected power converters.



Index Terms—Sensor applications, sensor signal processing, PLL, power grid, single-phase, frequency ramp

I. INTRODUCTION

Grid synchronization (GS) is responsible for the stable and efficient integration of various converter-interfaced energy sources into a microgrid. Conventionally, this is achieved using a phase-locked loop (PLL), which estimates the grid voltage frequency and phase from the measured signal. PLL is a type of filtering system, and filtering methods are widely employed in various sensor applications [1]–[4]. To achieve fast and accurate GS, the PLL needs to be robust in the face of various grid disturbances. One such disturbance is frequency ramping, which may be particularly pronounced in islanded microgrids. Frequency ramps can be caused by sudden changes in power generation, for example, an increase in solar intensity leading to a ramp-up in solar PV output, and/or consumption, such as in the evening when domestic users often connect multiple loads simultaneously, causing a ramp-up in the load demand. Therefore, PLL-based converter control systems need to be capable of tracking frequency ramps without any steady-state errors to facilitate the integration of large-scale renewable energy into the grid.

Type-2 (T2)-PLL, favored for grid-connected power converter control [5], struggles with phase tracking during frequency ramps, resulting in steady-state error (SSE). A remedy involves a second-order loop-filter (LF) in a type-3 (T3)-PLL [6], but this addition introduces complexity in both development (extra tuning gain) and implementation (extra second-order integrator). Additionally, it exhibits slow dynamics, potentially posing microgrid stability risks during frequency ramps. This has prompted researchers to enhance the T2-PLL, aiming for zero SSE in phase tracking without compromising fast dynamics. In [7], a forward compensation (FC) term improves the T2-PLL, albeit at the cost of increased tuning complexity due to an additional low-pass filter (LPF). Depending on LPF tuning, PLL stability may be compromised. To mitigate this issue, [8] suggests changing the LPF position for enhanced performance. These PLLs are designed exclusively for three-phase systems and are not applicable to single-phase ones. Moreover, the FC term in [7], [8] is amplitude-dependent and may introduce the division-by-zero case, complicating practical implementation.

In the single-phase scenario, several variations of T3-PLLs exist. In [9], a T3-PLL is combined with a second-order generalized integrator (SOGI) as the orthogonal signal generator (OSG). To improve dynamic response, a phase-lead compensator is added, albeit at the expense of harmonics robustness. Another modified T3-PLL in [10] operates even with DC offset in measurements but still grapples with dynamic response issues, requiring a phase-lead compensator for resolution.

To address the above-mentioned issues, we present modified T2-PLLs for single-phase systems. These PLLs are third-order systems in a closed-loop configuration, capable of completely eliminating phase tracking steady-state error (SSE) during frequency ramps. We propose two versions of the PLL, one with an additional low-pass filter (LPF) and one without, each with its own set of advantages and disadvantages. The ideas presented in this work are motivated by [7], [8]. The proposed PLLs are designed for a single-phase system and use an amplitude-independent FC term, which avoids the division-by-zero case, unlike [7], [8]. As such, the proposed PLLs can be considered as an improved single-phase version of [7], [8].

This letter makes three main contributions: Firstly, it introduces an amplitude-independent FC term, simplifying three-phase PLL implementations [7], [8]. Secondly, it integrates this term into a single-phase PLL structure, ideal for single-phase systems like domestic

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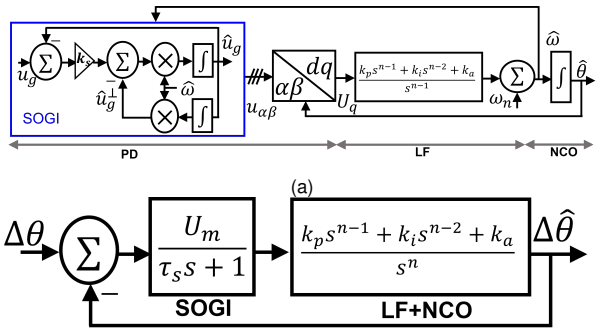

Fig. 1. Conventional single-phase SOGI-PLLs: (a) block diagram and (b) small-signal model (SSM) [11].

grid-connected solar PV system. Lastly, it applies constructive gain tuning methods for PLL LF gains, enabling performance comparison and assisting practitioners in selecting the appropriate PLL technique. The rest of this letter is organized as follows: Sec. II provides a brief overview of single-phase SOGI-PLLs. Details of the proposed PLLs are given in Sec. III. Comparative experimental results can be found in Sec. IV. Finally, this letter is concluded in Sec. V.

II. SINGLE-PHASE SOGI-PLL

Conventional single-phase T2 and T3 SOGI-PLLs, as depicted in Fig. 1, have PLL orders determined by LF configuration ($n = 2, 3$). The T2-PLL is characterized by $k_a = 0$. In single-phase PLLs, an additional OSG filter is required compared to the three-phase PLL counterpart due to the absence of orthogonal signals, which is characterized by $\mathcal{G}_s(s) = 1/(\tau_s s + 1)$, where $\tau_s = 2/k_s\omega$, $k_s > 0$, with ω denoting the signal frequency. In the quasi-locked state, the PD output of the PLL, without OSG dynamics, is given by:

$$U_q \approx U_m \left(\Delta\theta - \Delta\hat{\theta}\right), \tag{1}$$

where U_m is the signal magnitude, $\theta = \int \omega dt$ and $\hat{}$ indicates the estimated value. The PLL employs the phase error (PE) to synchronize its output with the input signal's phase. The open-loop and PE ($\theta_e = \theta - \hat{\theta}$) transfer functions of the SOGI-PLL can be derived as:

$$\mathcal{G}(s) = \left(U_m/(\tau_s s + 1)\right)\left(\left(k_p s^{n-1} + k_i s^{n-2} + k_a\right)/s^n\right). \tag{2}$$

$$\theta_e(s) = \left(1 + \mathcal{G}(s)\right)^{-1}\theta(s). \tag{3}$$

Then, for a ramp frequency input (with ramp rate r), the SSE for T2- and T3-PLLs can be obtained by using eq. (3) as:

$$\text{T2:}\quad \theta_e^{ss} = \lim_{s\to 0} s\theta_e(s)\left(r/s^3\right) = r/(U_m k_i). \tag{4}$$

$$\text{T3:}\quad \theta_e^{ss} = \lim_{s\to 0} s\theta_e(s)\left(r/s^3\right) = 0. \tag{5}$$

Steady-state errors reveal that the T2-PLL, unlike the T3-PLL, struggles with accurate phase tracking during frequency ramps. The T3-PLL, with its added gain and second-order integrator, enhances noise robustness but at the expense of slower dynamics.

III. PROPOSED PLL METHODS

A. Proposed Quasi Type 2 SOGI-PLL

Modified three-phase T2-PLLs [7], [8] calculate the FC term from eq. (1), but it can lead to division-by-zero issues due to amplitude-dependent phase estimation error. To address this, this study employs a linear PD with *atan2* operation to extract amplitude-independent phase error. The proposed single-phase T2-PLL is depicted in Fig. 2. When an input signal features a frequency ramp, it introduces a non-zero SSE, as per eq. (4), affecting the linear PD output. By incorporating this error as the FC term, phase tracking SSE can be eliminated. This additional compensation allows the proposed PLL to achieve T3 performance while using a T2 LF, resulting in its designation as the quasi T2 (QT2)-PLL.

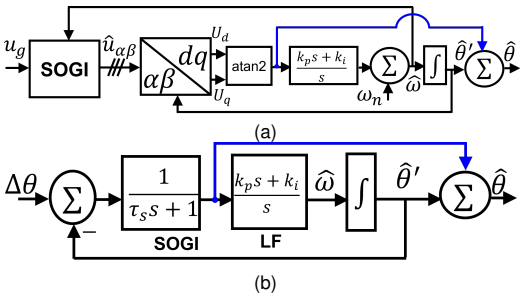

Fig. 2. Proposed QT2 SOGI-PLL: (a) block diagram and (b) SSM.

1) Zero SSE Phase Angle Tracking and Gain Tuning: Open-loop transfer function of the proposed PLL is given by:

$$\mathcal{G}(s) = s^2 + k_p s + k_i/\tau_s s^3. \tag{6}$$

Then, using eq. (3), the PE transfer function calculated as:

$$\theta_e(s) = \theta(s)\left(\tau_s s^3\right)/\left(\tau_s s^3 + s^2 + k_p s + k_i\right). \tag{7}$$

Then, the zero SSE for ramp frequency input can be verified as:

$$\theta_e^{ss} = \lim_{s\to 0} s\theta_e(s)\left(r/s^3\right) = 0. \tag{8}$$

The proposed QT2L-PLL involves four tuning parameters: k_s (τ_s), τ_l, k_p, and k_i. For tuning the noise-robust LPF, a compromise is necessary between dynamic response and disturbance rejection. After extensive simulations, a cutoff frequency of 50rad./sec. is selected, corresponding to $\tau_l = 0.02$. This value strikes an optimal balance between dynamic response and disturbance rejection. To adjust the LF gains, the open-loop transfer function (6) is written as:

$$G(s) = \alpha(s + \beta)^2/s^3, \tag{9}$$

where $\alpha = 1/\tau_s$ and β are the stability-enhancing coincident zeros to be designed. Phase margin (PM) [12] of (9) can be obtained as:

$$\text{PM} = -90^\circ + 2\tan^{-1}(\omega_c/\beta), \tag{10}$$

where ω_c is the crossover frequency. PLL literature suggests a phase margin of $30^\circ \sim 60^\circ$. The mid-point (45°) is selected in this work. Similarly, a ω_c between 110 ~ 140 rad./sec. is also recommended in the literature [9] and the mid-point 125 rad./sec. is selected, corresponding to $\beta = 51.78$. Then, eq. (9) can be written as:

$$G(s) = \alpha(s + 51.78)^2/s^3. \tag{11}$$

By comparing eqs. (6), (9), and (11), the LF gains can be obtained as, $k_p = 2\beta$ and $k_i = \beta^2$.

B. Proposed Filtered Quasi Type 2 SOGI-PLL

The additional compensation term (blue line in Fig. 2) lacks further filtering. High grid total harmonic distortion (THD) can negatively impact phase estimation. To address this, an extra LPF with time

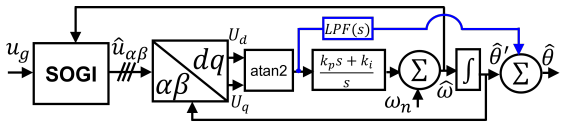

Fig. 3. Proposed QT2 SOGI-PLL with additional LPF.

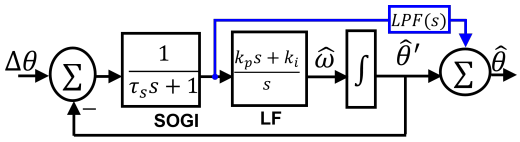

Fig. 4. Small-signal model of the proposed PLL with additional LPF.

constant τ_l can be added to the FC path, as shown in Fig. 3. This results in the QT2 with LPF (QT2L)-PLL configuration.

1) Zero SSE Phase Angle Tracking and Gain Tuning: Open-loop transfer function (Fig. 4) of the QT2L-PLL found as:

$$\mathcal{G}(s) = \left(\left(1 + k_p\tau_l\right)s^2 + \left(k_p + k_i\tau_l\right)s + k_i\right)/\left(\gamma s^4 + \delta s^3\right), \quad (12)$$

where $\gamma = \tau_l\tau_s$ and $\delta = \tau_l + \tau_s$. Then, by using eq. (12), the zero SSE of the proposed PLL can be verified as:

$$\text{QT2L:} \quad \theta_e^{ss} = \lim_{s\to 0} s\theta_e(s)\left(r/s^3\right) = 0. \quad (13)$$

The proposed QT2L-PLL has four tuning parameters: k_s (τ_s), τ_l, k_p, and k_i. Through extensive simulation, a cut-off frequency of 50rad./sec. is selected, which corresponds to $\tau_l = 0.02$ for the LPF. For LF tuning, transfer function (12) is rewritten as:

$$\mathcal{G}(s) = \left(K\left(s + \omega_{p1}\right)\left(s + \omega_{p2}\right)\right)/\left(s^3\left(s + \omega_{p3}\right)\right), \quad (14)$$

where $K = 1/\alpha$, $\omega_{p3} = \delta/\gamma$, and $\omega_{p1,2}$ are roots of the numerator polynomial. PM of the open-loop transfer function obtained as:

$$PM = -90^\circ + \tan^{-1}\left(\frac{\omega_c}{\omega_{p1}}\right) + \tan^{-1}\left(\frac{\omega_c}{\omega_{p2}}\right) - \tan^{-1}\left(\frac{\omega_c}{\omega_{p3}}\right). \quad (15)$$

In eq. (15), the unknown variables are ω_c, ω_{p1}, and ω_{p2} while $\omega_{p3} = 272.14$rad./sec. Moreover, coincident zeros can be considered, i.e., $\omega_{p1} = \omega_{p2} = \omega_p$. Then, eq. (15) can be simplified as:

$$PM = -114.67^\circ + 2\tan^{-1}\left(\omega_c/\omega_p\right). \quad (16)$$

Solving eq. (16) for a 45° phase margin, $\omega_p = 22.4122$rad./sec. can be found. With the selected values, eq. (14) can be rewritten as:

$$\mathcal{G}(s) = \left(11107.21\left(s + 22.41\right)^2\right)/\left(s^3\left(s + 272.14\right)\right). \quad (17)$$

By comparing eqs. (12), (14), and (17), one can find that $k_p = 114.24$ and $k_i = 1649.97$.

TABLE 1. PLL LF GAINS.

Methods (All With 45° Phase Margin)				
LF	Type 2	Type 3	QT2	QT2L
k_p	139.4	69.4	103.6	114.2
k_i	4855.4	2768	2681.2	1649.9
k_a	–	27586.4	–	–

IV. EXPERIMENTAL RESULTS AND DISCUSSIONS

Using the dSPACE DS1004 hardware-in-the-loop (HiL) platform, the performance of the proposed methods have been evaluated using a sampling frequency of 10kHz. As a comparative method, conventional T2 and T3 SOGI-PLLs have been used [9]. Tuning parameters of the selected PLLs are given in Tab. 1. The selected methods have been implemented in Matlab/Simulink and exported to dSPACE using code-generation for real-time implementation. For details about the considered experimental setup, interested readers may consult [13, Sec.6]. **To ensure fair comparison, the same phase margin has been used for tuning all the PLLs given in Tab. 1**. In the subsequent part of this Section, frequency and phase tracking error results have been scaled by 50Hz and, 45°, respectively, for per unit [p.u.] presentation. Moreover, the used legends are: T2 (▬), T3 (▬), QT2 (▬) and QT2L (▬). To comprehensively assess the proposed method's performance, four tests are conducted. The first test involves a frequency ramp with acceleration and deceleration (AaD), illustrated in Fig. 5 (a). In this scenario, the frequency increases from 50Hz to 52Hz and then decreases back to 50Hz. It's observed that the T2-PLL exhibits a constant error in tracking the frequency ramp, as supported by eq. (4). The proposed PLLs exhibit significantly faster tracking (QT2 - almost instantaneous and QT2L - 92 msec.) than the T3 method (152 msec.). Notably, the proposed QT2L-PLL displays slower dynamics compared to the QT2-PLL, attributed to the presence of the LPF in its forward path. Fast PE convergence will improve the ability of power converter-interfaced renewable energy sources to quickly respond to ramp variation in grid frequency. In the second test, a +1Hz frequency step is examined, and the outcomes are presented in Fig. 5 (b). It's observed that the proposed QT2 exhibits the smallest peak overshoot (56% lower than T2 and 37% lower than T3), while QT2L and T2 demonstrate comparable overshoot. Despite being tuned with the same phase margin, the T3 PLL exhibits notably slower dynamic response and the highest peak overshoot. In the third case, sinusoidal variation in the frequency have been considered as $\omega = \omega_n\left(1 + \sin\left(15t\right)\right)$ [9] and the results can be found in Fig. 5 (c). Results show that all methods are unable to accurately track the sinusoidal frequency variation. However, the proposed QT2 has the lowest phase tracking error (87% lower than T3 and 75% lower than T2) followed by the QT2L. This shows the suitability of the proposed PLL in tracking the challenging sinusoidal frequency variation case.

In the final test with harmonically distorted grid voltage (Fig. 6), all methods exhibit minor oscillations in phase estimation error. T3 has the smallest oscillation band-width (0.0033p.u.), followed by QT2L (0.0062p.u.), T2 (0.0073p.u.), and QT2-PLLs (0.0165p.u.), respectively. The LPF in QT2L effectively reduces harmonic effects. Although T3 had the poorest performance overall, it has the lowest estimation ripple in this context, indicating a trade-off between harmonic mitigation and dynamic performance. QT2L strikes a balanced performance, excelling in both dynamic response and harmonic disturbance rejection.

Tab. 2 summarizes time domain comparisons for the first two test cases. No methods achieved zero SSE in the last two test cases. So, those cases are not included in Tab. 2. The proposed QT2-PLL excels with the lowest overshoot and fastest settling time. While the proposed QT2L-PLL lags slightly behind the T2-PLL, its ability to track frequency ramps enhances its versatility over the T2-PLL.

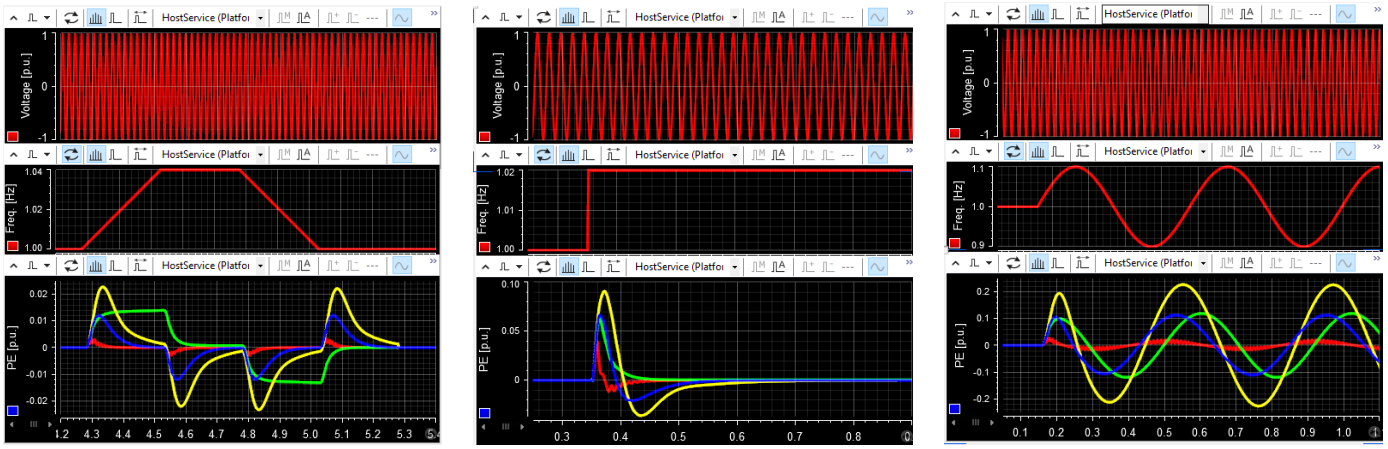

Fig. 5. Comparative experimental results for frequency variation (a) AaD, (b) step, and (c) sinusoidal.

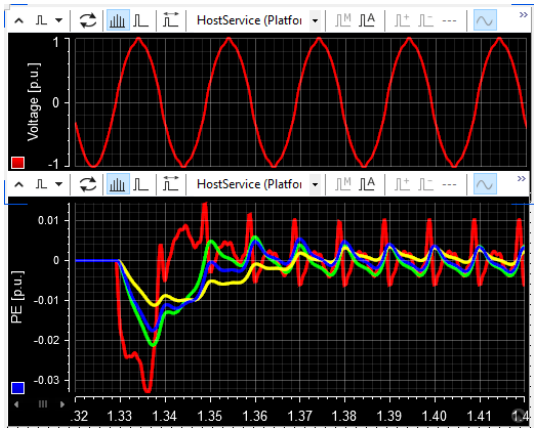

Fig. 6. Experimental results for harmonically distorted grid voltage.

V. CONCLUSION AND FUTURE WORKS

This letter presented single-phase T2 PLLs which are able to accurately track the phase even during frequency ramp. Technical details of the proposed techniques including zero error phase tracking ability and tuning are well detailed. Four comprehensive tests have been conducted to demonstrate the suitability of the developed methods. Experimental results showed that the proposed QT2-PLL method achieved a more than 50% lower overshoot compared to conventional alternatives. Similarly, the proposed QT2L method either had similar or better (depending on the cases) steady-state and dynamic performance compared to the conventional counterparts. These results show that the proposed methods are well-suited to serve as the grid-synchronization tool for grid-connected converter-interfaced renewable energy sources.

The proposed PLLs have two limitations: Firstly, none of the proposed methods, nor the comparative ones, can eliminate DC offset, which can be resolved by incorporating a third-order SOGI filter. Secondly, the proposed methods exhibit lower harmonic sensitivity compared to T3-PLL, attributed to the absence of an additional second-order integrator. This can be mitigated by adding pre- or in-loop filters. Addressing these limitations presents potential avenues for future research.

TABLE 2. QUANTITATIVE PERFORMANCE COMPARISON.

Test	Scaled Peak PE [p.u.]				Settling Time [msec.]			
	T2	T3	QT2	QT2L	T2	T3	QT2	QT2L
AaD	NA	0.023	0.004	0.013	∞	152	0	92
Freq.	0.09	0.063	0.04	0.067	61	189	44	140

Not applicable (NA) as it has steady-state error; ∞ implies that the SSE never reached the settling band (± 0.005p.u.) used for calculating the settling time.

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