
Proceedings Paper:
Pay, M.L., Christensen, J., He, F. et al. (3 more authors) (2023) A comparative study of FLL and PLL in boost PFC converter control for smart greenhouse farming application. In: 2023 IEEE International Conference on Agrosystem Engineering, Technology & Applications (AGRETA) Proceedings. 2023 IEEE International Conference on Agrosystem Engineering, Technology & Applications (AGRETA), 09 Sep 2023, Shah Alam, Malaysia. Institute of Electrical and Electronics Engineers (IEEE) . ISBN 9798350347340

https://doi.org/10.1109/agreta57740.2023.10262537

A Comparative Study of FLL and PLL in Boost PFC Converter Control for Smart Greenhouse Farming Application

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***Abstract*—LED lights have become very popular recently for smart farming applications, where they provide artificial light as the substitute for sunlight in a greenhouse or indoor farming environment. To ensure a low total operational cost and improve the efficiency of farming in those environments, it is imperative that the overall LED lighting system is energy efficient. LED is a dc system, whereas the grid is an ac system. As such, an LED driver is needed to perform the necessary voltage conversion. The boost power factor correction (PFC) converter is a popular LED driver that provides output voltage regulation and power factor correction at the same time. As the LED driver is grid-connected, its control system requires real-time estimation of the grid voltage parameter information for reference current generation. In this study, a comparison between frequency- and phase-locked loops as the grid detection method inside the converter control system is provided. For the phase-locked loop (PLL), a single-phase quasi-type-1 structure is considered. It is then compared with the conventional second-order generalised integrator (SOGI)-frequency-locked loop (FLL). Comprehensive numerical studies are performed to evaluate the performance of FLL and PLL in challenging grid voltage cases. Results show that the source current has a lower total harmonic distortion when PLL is used as the synchronisation tool over the FLL counterpart. This can be attributed to the use of moving average filter in the PLL, which provides additional harmonic robustness compared to FLL. Lower distortion by the PLL method will the make LED driver, consequently smart farming more energy efficient.**

***Index Terms*—Power Factor Correction, Frequency-Locked Loop, Boost Converter, Phase-Locked Loop.**

I. Introduction

The global population is growing steadily. To feed this growing population, food production needs to increase to meet the demands. However, this will require more land and fertilizer usage, causing further increase in carbon emission. To address this issue, smart greenhouse farming through speed-breeding [1] has emerged as a suitable alternative to conventional farming. The speed-breeding method essentially enhances crop productivity by changing daylight exposure to plants grown in the greenhouse, and more importantly without the need for additional land use. LED lights are often used to mimic the natural day-night cycle and it has been shown in [2] that crop productivity can be doubled by artificially prolonging the daylight through these LED lights.

Given the importance of LED lights in smart greenhouse farming, making the LED driver efficient, will have a significant impact in lowering the total operational cost and increasing the efficiency of the smart farming system [3]–[5]. An LED driver acts as an ac/dc converter that converts the ac grid voltage into dc voltage for powering the LED lights. In addition, it needs to provide power factor correction to make it grid-friendly.

In the literature, several popular ac/dc converter circuit topologies are available as the LED driver. Interested readers may consult [3], [6] and the references therein for an overview of the existing converter topologies. Among the reported topologies, the boost PFC converter [7] is widely used as the LED driver due to its simplicity in design and reliable operation over long time.

High-performance operation of the boost PFC converter is ensured by the converter control system. The improvement to the boost PFC converter performance leads to a more efficient LED driver, thereby could improve the overall efficiency of smart greenhouse farming. This motivated us to study the control of boost PFC converter. For a comprehensive summary of boost PFC converter control system, [8] and the references therein can be consulted. In summary, there are four main types of controller for the boost PFC converter [8], where the most popular one being the two-loop architecture, where a voltage and a current controller are cascaded to regulate the opening/closing of the power semiconductor switch in the boost part of the converter. A detailed graphical overview of this controller can be found in the next section.

In the two-loop architecture, the reference current is generated by the grid voltage detection scheme. This has motivated researchers to develop advanced grid detection schemes where PLL is often employed. Popular PLLs for boost PFC converter are two-sample PLL [9], running-average filter-based

PLL [10], power-PLL [11], digital PLL [12], second-order generalised integrator (SOGI-PLL) [13] etc., to name a few.

Besides PLL, the use of frequency-locked loop (FLL) for grid detection is starting to gain attention [14], [15]. However, to our best knowledge, a comprehensive study that compares the performance of PLL and FLL in controlling the boost PFC converter has not been considered in the literature. Thus, the goal of this paper is to fill this void. In this paper, a simple quasi type-1 PLL is first developed for the single-phase LED driver. Then, this PLL is compared with the conventional SOGI-FLL [15] in terms of harmonics distortion in the source current drawn from the grid. The comparative results obtained here can be useful to future researchers and industrial practitioners in selecting the suitable grid detection scheme for the boost PFC converter.

The remaining section of this paper is categorised as follows: An overview of the boost PFC converter circuit and control method is presented in Section II. The developed PLL and the conventional FLL are detailed in Section III. Section IV discussed and analysed the obtained comparative results. Concluding remarks are given in Section V.

II. Control of Boost Converter

A boost PFC converter can convert ac input voltage into fixed dc output voltage. This makes it a suitable choice for driving LED lights [7]. In addition, this converter can also be used to improve the power factor as per IEEE Std. 519 [16]. The circuit diagram and the control system of this converter are shown in Fig. 1.

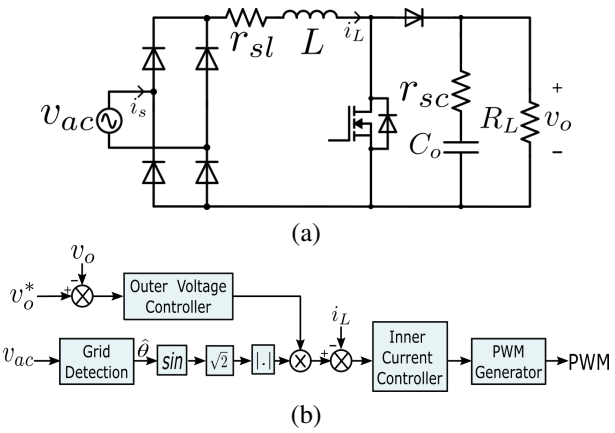

Figure 1. Boost PFC converter (a) Circuit diagram [8] and (b) control system adapted from [17].

The controller for boost PFC converter needs the instantaneous phase of the grid voltage signal's fundamental component, which is often harmonically distorted in practice. This requires the development of an advanced grid detection scheme, which can improve the overall control performance and reduce the harmonic distortion in the source current introduced by the distortion in the voltage. Grid detection scheme is often achieved by PLL [8] or FLL [14]. In this paper, we aim to provide a systematic comparison between these two grid detection schemes for the boost PFC converter control system.

III. Frequency- and Phase-Locked Loops

As highlighted in Sec. II, in Type-IV Boost PFC controller, real-time extraction of grid voltage fundamental component is essential for effective operation of the converter. The voltage signal is conventionally modelled as:

$$v_{ac}(t) = V_{ac}\sin\underbrace{(\omega_g t + \phi)}_{\theta} + \sum_{h=3,5,7,\ldots} V_{ac,h}\sin\underbrace{(\omega_{g,h} t + \phi_h)}_{\theta_h}, \tag{1}$$

where the amplitude, frequency, phase offset, and instantaneous phase are represented by V_{ac}, ω_g, ϕ, and θ, respectively. The subscript h indicates the harmonics order. The frequency ω_g has a nominal value $\omega_n = 100\pi$ rad./sec. Considering the nominal value, the actual grid frequency can be written as, $\omega_g = \omega_n + \tilde{\omega}$, where the deviation from the nominal value is denoted by $\tilde{\omega}$. To maintain the unity power factor, voltage and current must be always in phase. As such, it is important to estimate the fundamental phase θ from the measured harmonically distorted voltage signal $v_{ac}(t)$, which can be done using either FLL or PLL. The harmonics in (1) affects the estimation accuracy since this terms is unknown in practice.

A. Phase-Locked Loop

Conventional PLL is developed for three-phase system. In the stationary reference frame (StRF), three-phase system can be characterised by two orthogonal signals. However, for the single-phase case, the orthogonal signal is missing. To address this issue, an all-pass filter (APF) can be considered [18], [19] as the orthogonal signal generator (OSG), which is shown in Fig. 2.

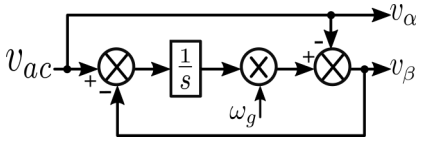

Figure 2. Time-domain realisation of APF.

Unlike other similar OSGs reported in the literature (e.g. complex coefficient filter [20], second-order generalised integrator [15], [21], Luenburger observer [22]), APF does not provide any harmonic robustness, albeit it is easy to implement, low-order and requires no tuning.

The transfer function of an APF is given by:

$$\frac{v_\beta(s)}{v_\alpha(s)} = \frac{\omega_g - s}{\omega_g + s}, \tag{2}$$

where v_α is the measured in-phase voltage signal and v_β is the orthogonal component of the grid voltage obtained through the APF. The magnitude and phase of this transfer function are given by:

$$\frac{v_\beta(s)}{v_\alpha(s)} = 1\angle -2\tan^{-1}\left(\frac{\omega}{\omega_g}\right). \tag{3}$$

From (3) and Fig. 3, one can see that APF only effects the phase.

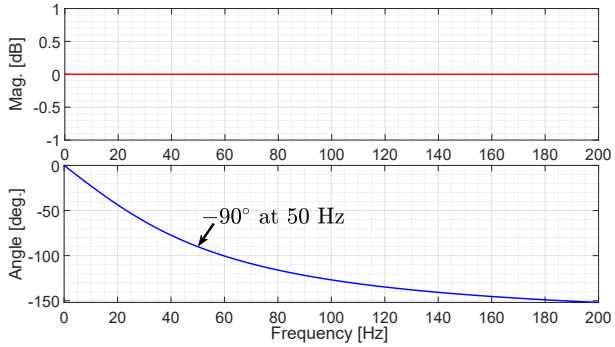

Figure 3. Magnitude and phase responses of the APF.

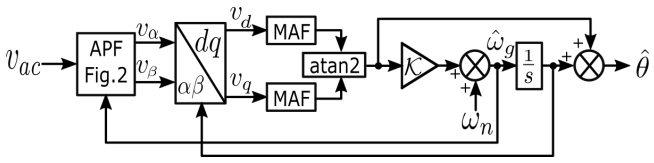

Figure 4. APF-based Quasi Type-1 PLL.

Using the estimated orthogonal signal, a quasi type-1 PLL [23] can be implemented as shown in Fig. 4. In this PLL, a proportional loop filter (LF) with gain $\mathcal{K} > 0$ is used. In addition, a moving average filter (MAF) is used for harmonic filtering purpose, in which the continuous- and discrete-time transfer functions are respectively given by,

$$\text{MAF}(s) = \frac{1 - e^{-\mathcal{T}_c s}}{\mathcal{T}_c s}, \tag{4}$$

$$\text{MAF}(z) = \frac{1}{\mathcal{T}_d}\frac{1 - z^{-\mathcal{T}_d}}{1 - z^{-1}}, \tag{5}$$

where $\mathcal{T}_c$ is the filter window length in time and $\mathcal{T}_d$ is the corresponding number of discrete samples, which can be obtained as $\mathcal{T}_d = \mathcal{T}_c/T_s$ with T_s being the sampling-time used for discrete-time implementation. Various international standards impose strict limitations on odd-order harmonics (e.g. IEEE Std. 519 [16]). As such, a half-cycle window length is selected here, which is known to eliminate all odd-order nominal frequency harmonics [23].

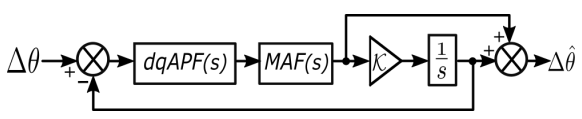

Figure 5. Small-signal model of the developed single-phase QT1-PLL.

1) Parameter Tuning: To tune the gain $\mathcal{K}$, a small-signal model is developed as shown in Fig. 5. In this model, the StRF transfer function of APF is replaced by the synchronous frame counterpart, which is given by [19]:

$$\text{dqAPF}(s) = \frac{1}{2}\frac{s + 2\omega_n}{s + \omega_n}. \tag{6}$$

where $\omega_n = 100\pi$ rad./sec (see Section III) is the nominal grid frequency. Then, through block diagram simplification, the open-loop transfer function can be found as:

$$G(s) = \frac{\text{dqAPF}(s)\text{MAF}(s)}{1 - \text{dqAPF}(s)\text{MAF}(s)}\left(\frac{\mathcal{K} + s}{s}\right). \tag{7}$$

The open-loop phase margin as a function of the LF gain is given in Fig. 6. In the PLL literature, a phase margin of $30^\circ \sim 60^\circ$ is often recommended [24]. Here, the middle point (45°) is considered, which corresponds to $\mathcal{K} = 75$ and this value has been selected for the LF.

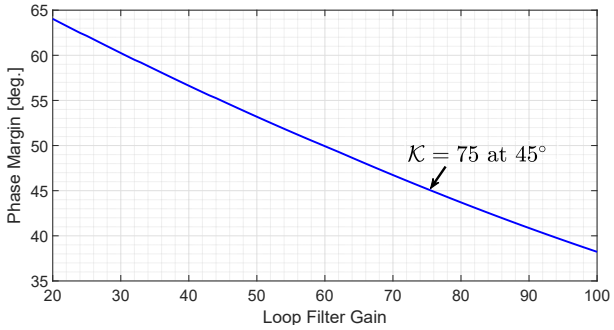

Figure 6. PLL phase margin as a function of $\mathcal{K}$ with $\mathcal{T}_c = 10$msec.

B. Frequency-Locked Loop

FLL is a popular method for harmonically robust estimation of θ from $v_{ac}(t)$ and the SOGI-FLL is the most popular method for the single-phase system [15], [25], where the SOGI is used as an adaptive filter for orthogonal signal generation purpose. The block diagram of SOGI-FLL is depicted in Fig. 7. Transfer functions of the SOGI filter are given by:

$$G_\alpha(s) = \frac{\hat{v}_\alpha(s)}{v_{ac}(s)} = \frac{\gamma\hat{\omega}_g s}{s^2 + \gamma\hat{\omega}_g s + \hat{\omega}_g^2}, \tag{8}$$

$$G_\beta(s) = \frac{\hat{v}_\beta(s)}{v_{ac}(s)} = \frac{\gamma\hat{\omega}_g^2}{s^2 + \gamma\hat{\omega}_g s + \hat{\omega}_g^2}, \tag{9}$$

where $\gamma > 0$ is the tuning gain and $\hat{\cdot}$ represents the estimated value. The Bode plot of (8) and (9) are shown in Fig. 8.

The Bode plots show that $G_\alpha(s)$ is a band-pass filter where grid frequency determines the frequency band of the allowed signals. Conversely, $G_\beta(s)$ is showing a low-pass filter characteristics, with the pass-band being determined by the grid frequency. In addition, this transfer function shows a 90° phase difference. These filtering characteristics make SOGI very suitable as an adaptive filter for FLL application.

SOGI requires the estimated grid frequency, which can be obtained by the FLL. As shown in Fig. 7, the FLL is implemented as a product of the SOGI estimation error and

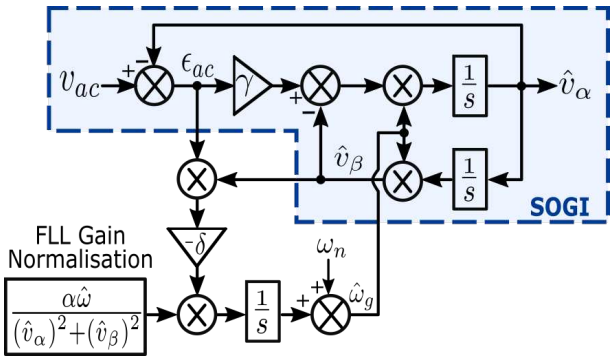

Figure 7. SOGI-FLL for single-phase system [15].

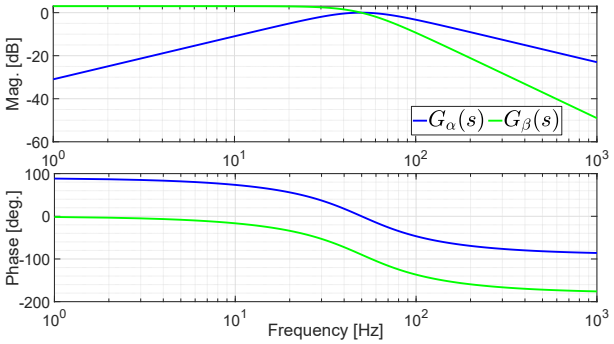

Figure 8. Bode diagram of SOGI with $\gamma = \sqrt{2}$ and $\hat{\omega}_g = 100\pi$ rad./sec.

the quadrature component. The error transfer function of the SOGI filter is given by:

$$E\left(s\right) = \frac{\epsilon_{ac}(s)}{v_{ac}(s)} = \frac{s^2 + \hat{\omega}_g^2}{s^2 + \gamma\hat{\omega}_g s + \hat{\omega}_g^2}. \tag{10}$$

The phase plot of transfer functions (9) and (10) are shown in Fig. 9. The input variables have the same phase when the frequency is lower than the SOGI resonant frequency, however, they are out of phase when the input frequency is higher than the resonant frequency. As such, one can define the variable that represent the frequency error. By using a simple tunable integral controller with tuning parameter $\delta > 0$, the unknown frequency can be easily estimated. The normalisation term in FLL ensures that the frequency estimation convergence is independent of the signal amplitude. The FLL dynamics can be approximated by a first-order LPF [15], which is given by

$$\frac{\hat{\omega}_g}{\omega_g} = \frac{\delta}{s + \delta}. \tag{11}$$

As such, the FLL gain can be tuned as a function of the desired settling time, for a which the formula is available in the literature [26].

IV. Results and Discussions

To study the effect of PLL and FLL in boost PFC converter control performance, a MATLAB/Simulink simulation study is considered here. The circuit and control parameters listed in [27] are used for the comparative study. The default PLL

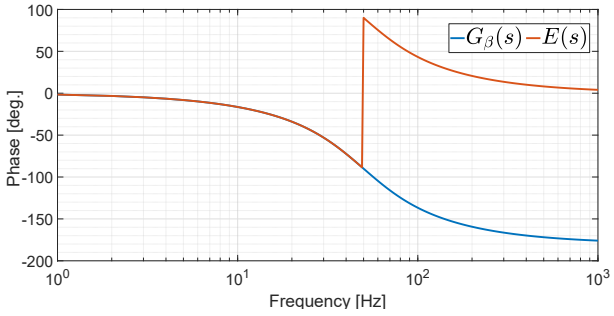

Figure 9. Bode phase plot of FLL input variables.

model in [27] are replaced by the PLL (Section III-A) and FLL (Section III-B) methods as described previously. The PLL parameters are selected as $\mathcal{T}_c = 10$ msec. and $\mathcal{K} = 75$. $\gamma = \sqrt{2}$ and $\delta = 50$ are selected for the FLL following [15]. To comparatively evaluate the performance of PLL and FLL, two challenging test scenarios have been considered involving voltage sag and swell together with harmonic distortion. In both cases, the grid is distorted with 0.1p.u. 3^{rd}-order, 0.08p.u. 5^{th}-order, 0.06p.u. 7^{th}-order and 0.05p.u. 11^{th}-order harmonics.

In the first case, a fundamental component voltage sag of -0.25p.u. is considered, and the results are depicted in Figs. 10-12. As the underlying controller is the same for both PLL and FLL-based control scheme, both methods show similar dynamic performance for the PFC output voltage and source current. However, the two methods behaviors are very different in the case of total harmonic distortion, which is measured by the following formula:

$$\text{THD} = \frac{\sqrt{\sum_{n=2,3,\ldots} I_n^2}}{I_1}, \tag{12}$$

where the RMS values of the currents are denoted by I and the subscript 1 and n represent the fundamental and harmonic components, respectively.

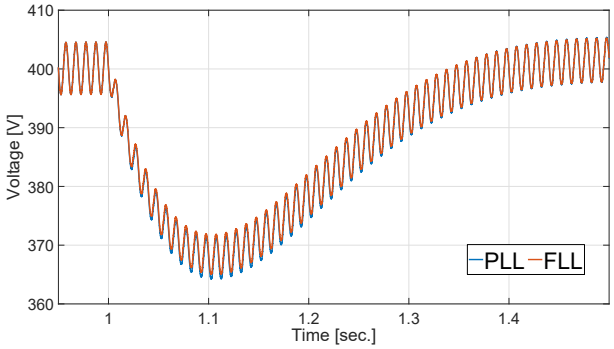

Figure 10. Output voltage for the case of grid voltage sag.

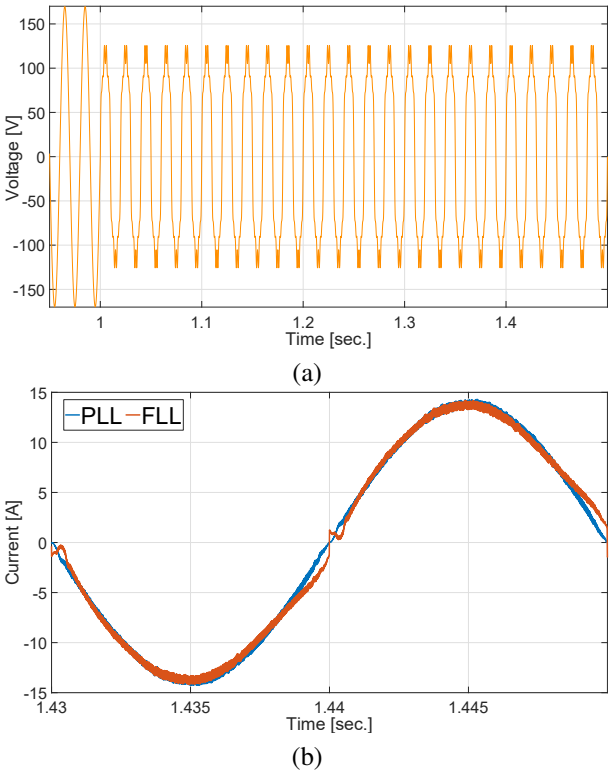

Figure 11. Grid voltage and currents for the case of grid voltage sag: (a) Grid voltage and (b) Source current.

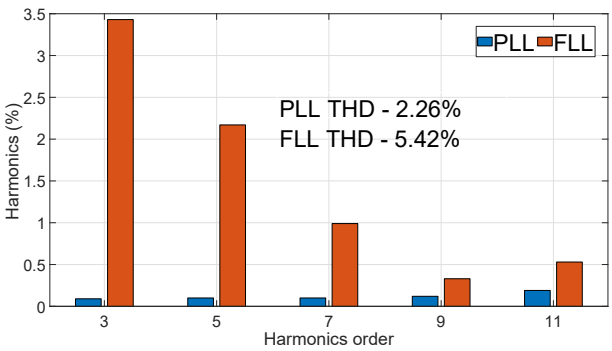

Figure 12. Source current THD for the case of grid voltage sag.

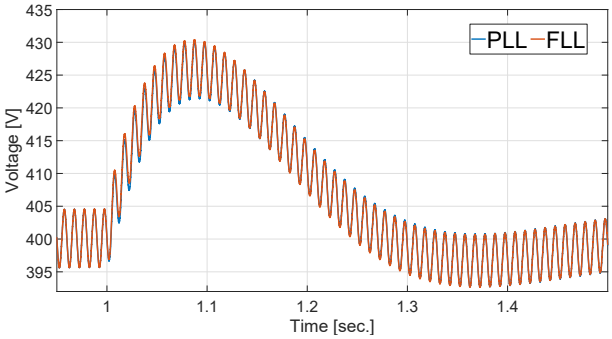

Figure 13. Output voltage for the case of grid voltage swell.

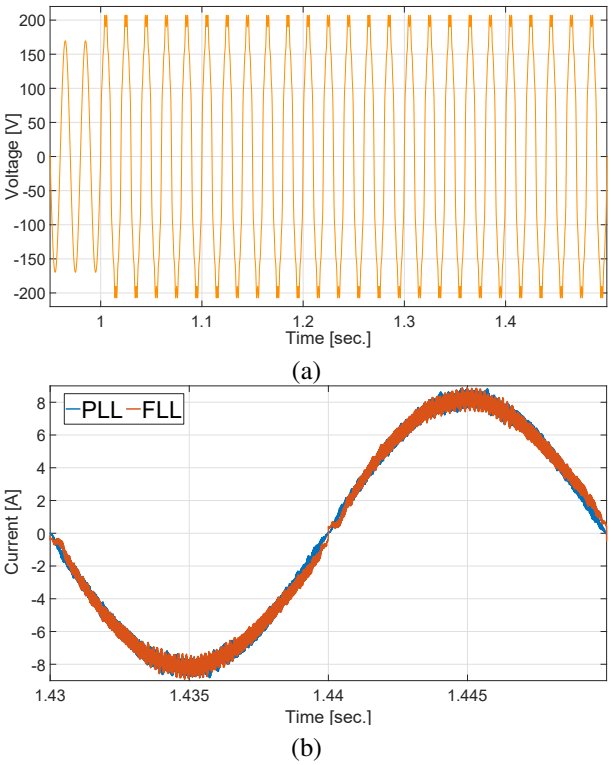

Figure 14. Grid voltage and currents for the case of grid voltage swell: (a) Grid voltage and (b) Source current.

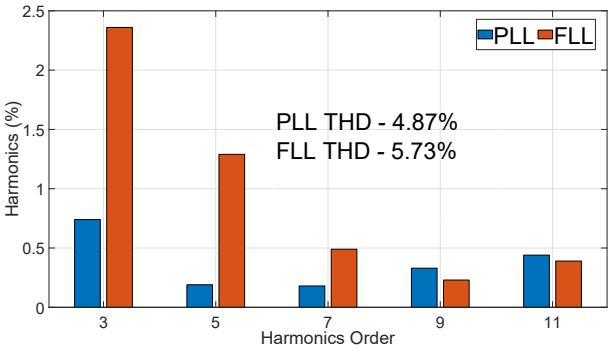

Figure 15. Source current THD for the case of grid voltage swell.

The results in Fig. 12 show that the THD in source current by PLL is $\approx 58\%$ lower than the FLL counterpart. In Fig. 12, only the distortion results with respect to the considered voltage harmonic-order are shown to show the impact of voltage harmonics on the current harmonics. A lower THD is always preferable as it reduces the reactive power consumption by the load, which will improve the overall efficiency of the system.

In the second case, a fundamental component voltage swell of $+0.25$p.u. is considered. The comparative simulation results are given in Figs. 13-15. In Fig. 14, only the zoomed view is presented, as the dynamic responses are almost non-distinguishable. The results for this case are consistent with the results obtained in the previous case, i.e., the dynamic

performances are very similar for PLL and FLL-based control schemes. However, the difference appears mainly in the steady-state behavior of the source current. In this case, the THD in source current by PLL is $\approx 15\%$ lower than the FLL counterpart. This shows the superiority of PLL over FLL in the case of voltage swell.

The results in this section show that PLL and FLL have similar dynamic performance when the grid is harmonically distorted and undergoes voltage sag/swell. However, they differ significantly in the steady-state behavior of source current drawn by the PFC from the grid. PFC converters are subject to power quality standards such as the IEEE Std. 519 [16]. Satisfying this standard will require the THD value to be within a specific limit. Our results show that the THD with PLL was always less than 5%, while this is not the case for FLL. As such, PLL may offer better solution compared to the FLL for boost PFC converter control. As this converter works as the LED driver for smart farming, a lower THD will also make smart greenhouse farming more energy efficient.

V. Conclusions

This paper studied the control of boost PFC converter, which is ubiquitously used in smart greenhouse farming as the LED driver. Grid detection plays an important role in controlling the converter and this has been achieved by developing a quasi type-1 PLL for the single-phase system. The technical details and parameter tuning are provided for the developed PLL. As a comparison, the conventional single-phase FLL is selected. The simulation results show that our proposed method is always able to provide lower THD compared to FLL. In addition, the THD of PLL never exceeded 5%, which this is not the case for FLL. So, the developed PLL is suitable to meet strict power quality requirement imposed by various international standards. Moreover, a lower THD from using the developed PLL would result in an efficient LED driver, which has the potential to make smart greenhouse farming further attractive through a lower operational cost.

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