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Soft switching voltage regulation for inductorless piezoelectric transformers: a cyclic mode analysis

Zijiang Yang[1], Jack Forrester, Jonathan N. Davidson, Martin P. Foster and David A. Stone

***Abstract*-This paper describes a novel methodology for predicting the ability of an inductorless driven piezoelectric transformer (PT)-based H-bridge inverters to simultaneously achieve zero-voltage switching and output regulation. A new idea for output voltage regulation by controlling deadtime interval is presented. A model is derived using cyclic-mode analysis to estimate the state-variable parameters of the circuit for a given operating condition. The model is then used to demonstrate operation in the zero-voltage switching (ZVS) region and to estimate the deadtime period, load and operating frequency along the ZVS boundary. The output voltage regulation profile is presented and regions where voltage regulation can be continuously achieved while still obtaining ZVS are shown. Both SPICE simulation and experimental results taken using a ring-dot radial-mode PT are presented as verification. The proposed method for a H-bridge PT-based inverter is able to achieve a 5V output from 15V-60V input with simultaneous ZVS and voltage regulation.**

I. INTRODUCTION

Piezoelectric transformers (PTs) have raised great research interest over the past few years, and are an exciting alternative to traditional magnetic transformers owing to the advantages in low electromagnetic interference (EMI), high power density (>40W/cm^3), high efficiency, reduced weight and simpler manufacturing process [1]–[4]. PTs exhibit high quality factor since they are constructed from high-quality factor materials, such as lead zirconate titanate (PZT), and so are excellent devices for power electronics applications [5]–[8]. By using the electro-mechanical properties of the piezoelectric materials, the energy is transferred from the input to the output electrodes via mechanical vibrations. PTs normally operate in a narrow frequency band close to their primary resonant frequency, and the optimum operating frequency is dependent on parameters such as temperature, load, vibration mode and geometry [1][5][9].

Several circuit topologies have been reported in the literature to drive PTs, such as class-E, push-pull and half-bridge [1][5][10]. However, zero-voltage switching (ZVS) is difficult to achieve due to the large input capacitance of the PT and limited availability of the resonant current. Thus, careful consideration should be taken when designing the control circuit and PT to ensure that sufficient current is available to charge the PT input capacitance to the DC (direct current) rail during the necessary deadtime period [10][11]. If the deadtime interval is too small or the amplitude of the resonant current is insufficient, the input capacitor voltage cannot reach DC input voltage before the high-side MOSFET is turned on and switching loss occurs (i.e. ZVS is not achieved).

For traditional resonant converters, the deadtime period is small compared to the switching period due to the large resonant current circulating. For these converters, one may assume that the resonant current is constant during deadtime, simplifying analysis [12]. However, for a PT-based converter, this assumption is not valid because the large input capacitance (C_{in} shown in Fig. 1 requires considerable charging time (typically around a quarter of the switching cycle) meaning one must consider the variation of the resonant current over this quarter cycle. Early implementations [2] of PT-based power supplies used magnetic inductors to simplify soft switching. The inductorless design used in this paper avoid this additional bulky component.

Several authors have developed analytical models to estimate circuit behaviour and ZVS ability in order to maximise the efficiency of a PT-based converter under different operating conditions. In [7], the ZVS characteristics of an inductorless PT-based converter are presented. However, [7] presents an overly conservative estimation of ZVS ability, due to the switching waveform shape assumption of the PT input capacitor voltage (i.e. square wave) and the resonant current phase shift. In addition, its application is limited since only the deadtime period is varied as a control parameter whereas ZVS is also dependent on switching frequency and load.

In [13], the ZVS ability is represented as a function of the input-to-output capacitance ratio and derived using a parametric sweep of the equivalent circuit parameters. Although good agreement between simulation and calculation is indicated by this approach, the ZVS predictions are less accurate as the parameter sweep is dependent on a curve-fit obtained from a specific PT characterisation. In [14], a state-variable model is employed to describe the circuit operating conditions of a PT-based inverter. A fundamental-mode approximation (FMA) is used to describe the nonlinear behaviour of the bridge rectifier and load. A numerical method is then employed to indicate the ZVS region as a function of

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duty cycle and switching frequency. Although these methods are presented with improved accuracy, they are difficult to implement in practice due to the lack of both normalised parameter analysis and design example.

In [15], a piecewise linear state-variable model is presented with improved accuracy for predicting ZVS. The ZVS ability of an inductorless PT-based inverter is assessed using cyclic-mode analysis. The ZVS profile is generated as a function of deadtime, switching frequency and load. ZVS boundary has been highlighted for different PTs and the appropriateness of PTs for different applications are assessed.

In [11], an analytical model of the inductorless half-bridge driven PT is derived using a describing function approach. A critical design criterion is derived to guarantee ZVS is achieved and the difficulty associated with multiple parameter control for ZVS operation is highlighted.

However, all of the methods previously described exhibits one or more of following problems: —

1) They do not adequately describe how to obtain continuously achievable ZVS, especially when the ZVS region is disconnected at the matched load condition (the worst-case scenario for achieving ZVS).
2) They lack a design example and practical implementation requires complex control circuitry for simultaneous parameter control [16] (e.g. switching frequency and deadtime).

Several methods are proposed in literature to regulate the output voltage of a PT-based converter. In [17], a hybrid half-bridge H-bridge converter is employed and output voltage regulation is achieved by separately controlling the on-period for each switch. Energy and charge conservation are used to calculate the state variables and the ZVS boundary is found as a function of voltage gain. A simulated efficiency of 93.6% is achieved with 10W output power at 500V input and 120V output.

To ensure an adjustable voltage gain, a tuneable radial-mode PT (an additional piezoelectric section is added between primary and secondary) with an external control capacitance is presented in [8] and [18], with duty-cycle control used to compensate for input voltage and load variations. The output is regulated at 55V with 220V input and 45% load variation in [8], and 41.5V with 250V input and 30% load variation in [18].

To improve the voltage regulation ability, compensation networks are employed in [19]. A comprehensive analysis of the impacts of the compensation networks on the characteristics of the PT is provided. Several input and output matching networks are employed via different combinations. The voltage gain can be tuned during the design phase by changing the compensation networks. General guidelines for the selection of matching networks are provided for a given PT with output voltage regulation requirements.

These three methods, however, experience one or more of the following drawbacks: —

1) No analytical model is employed to estimate the circuit behaviour and therefore ZVS cannot be guaranteed during the output regulation process.
2) The output regulation ability is limited since the ZVS region as a function of any particular circuit parameter is unclear, especially when the ZVS region is discontinuous.
3) Although employing a series inductor would enlarge the ZVS operating region, it reduces the output regulation ability of the converter [19].

In this paper, a novel inductorless H-bridge-driven PT-based power supply is proposed that can simultaneously achieve ZVS and output regulation through the introduction of a zero-voltage level during the deadtime interval. A piecewise linear state-variable model is presented, which provides predictions of switching waveforms from which cyclic mode analysis is used to provide the ZVS profile, ZVS boundary and output voltage characteristics. Output regulation with continuously achievable ZVS is obtained by controlling the duration of the zero-voltage level during the deadtime interval via a H-bridge topology.

The contribution of the proposed work includes: —

1) Achieving voltage regulation.
2) Achieving ZVS in the PT input capacitance and with all MOSFET capacitances.
3) Cyclic mode analysis to estimate circuit behaviour, ZVS and voltage regulation characteristics.
4) Control of an H-bridge to achieve the above objectives.

This article is organized as follows: The basic operation of the PT-based inductorless H-bridge inverter is given in section II. Section III describes the piecewise linear state-variable model with the corresponding operating modes and the deadtime interval requirement for each mode. The cyclic modelling analysis and state-variable solution for ZVS and output voltage is given in section IV. Experimental results are demonstrated in section V. Section VI illustrates the ZVS and output voltage characteristics at different circuit conditions. Section VII demonstrates simultaneous voltage regulation and ZVS performance for a given PT. Practical design consideration regarding PT design, ZVS and voltage regulation are demonstrated in section VIII.

II. Operation of Inductorless H-bridge PT-based Resonant Inverter

A. Operating principle

When a PT operates near resonance, it generally exhibits a high quality factor (Q) and its electrical behaviour can be modelled by the Mason equivalent circuit shown within the dashed box in Fig. 1. The input capacitor (C_{in}) and output capacitor (C_{out}) represent the capacitances created between the electrodes of the PT. Components C_1, L_1, and N model the mechanical resonant behaviour, and R_1 corresponds to the loss (or damping) in the PT. Sufficient dead-time intervals are applied between the gate signals of the MOSFETs to prevent shoot-through and to achieve ZVS by allowing time for the resonant current i_{L1} to charge C_{in} from $-V_{\text{dc}}$ to $+V_{\text{dc}}$ (and vice versa).

Fig. 2 shows the steady-state switching waveforms for the inverter shown in Fig. 1 under ZVS condition, where $v_{C\text{in}}$, i_{L1} and v_L are the PT input capacitor voltage, resonant current and

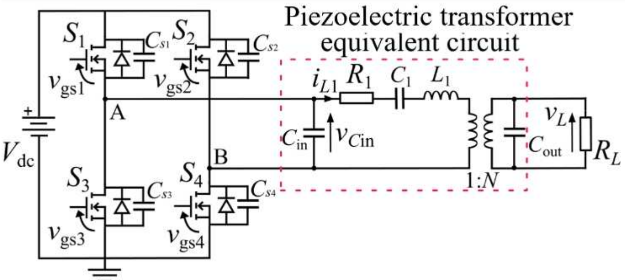


Fig. 1. Inductorless driven PT-based H-bridge inverter.

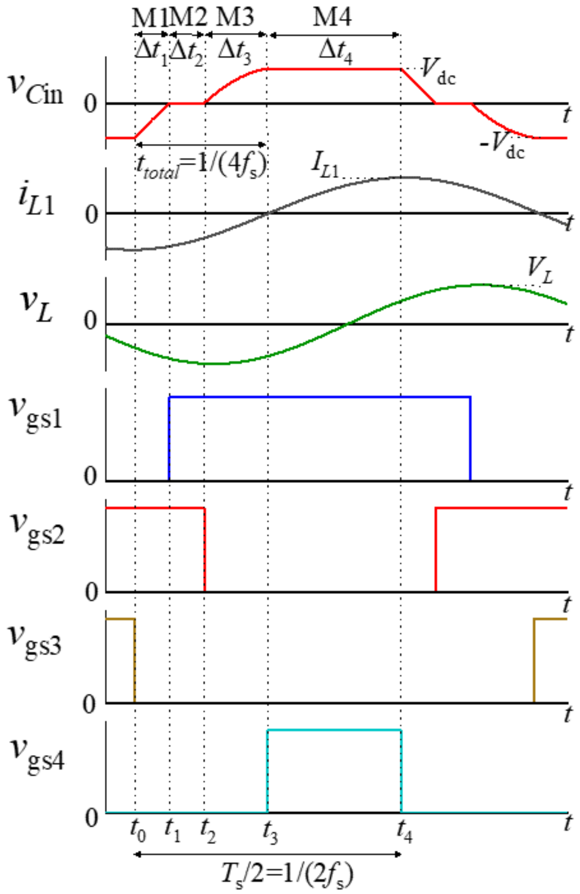


Fig. 2. Switching waveforms of the inductorless driven PT-based H-bridge inverter.

output (load) voltage, respectively. The resonant current is assumed to be sinusoidal due to the high Q-factor of the PT and its peak value is shown as I_{L1}. f_s is the switching frequency. Output voltage regulation is afforded by adjusting the duration of the zero-voltage interval labelled as Δt_2 in Fig. 2.

For the purpose of simplifying the analysis for ZVS operation it is assumed that the circuit exactly achieves ZVS and so can be described entirely by the mode sequence M1→M2→M3→M4 due to the half-cycle symmetry exhibited by the circuit operation. The first mode (M1) starts at time $t=t_0$ and the transition from mode i to mode i+1 occurs at time t_i. The transition times are labelled above the v_{Cin} waveform in Fig. 2. The mode time durations, Δt_1, Δt_2, Δt_3 and Δt_4 (where $\Delta t_i = t_i - t_{i-1}$) refer to the deadtime during M1; the conduction time of S_1 & S_2 during M2 when v_{Cin}=0; the deadtime during M3; and the conduction time of S_1 & S_4 during M4 to maintain V_{dc} (or S_2 & S_3 conduction period in M4 to maintain $-V_{dc}$ for the second half-cycle), respectively. t_{total} is the total deadtime period (i.e. $t_{\text{total}} = \Delta t_1 + \Delta t_2 + \Delta t_3$). As can be seen, ZVS is achievable if $v_{Cin}(t_3) \geq V_{dc}$.

During a half-cycle period, the inverter exhibits one of the following four modes of operation, depending on the control of the switches.

M1: $t \in [t_0, t_1]$: Prior to time t_0, MOSFETs S_2 and S_3 are on so $v_{Cin}(t_0) = -V_{dc}$. At $t=t_0$, only S_2 is turned on and so the resonant current, i_{L1}, circulates through C_{in}, thus v_{Cin} is being charged from $-V_{dc}$ towards 0V.

M2: $t \in [t_1, t_2]$: At $t=t_1$, S_1 and S_2 are turned on to set v_{Cin}=0 and so i_{L1} flows through both S_1 and S_2.

M3: $t \in [t_2, t_3]$: At $t=t_2$, only S_1 is turned on and i_{L1} once again circulates through C_{in} charging it in a positive direction towards V_{dc}.

M4: $t \in [t_3, t_4]$: At $t=t_3$, $v_{\text{Cin}}(t_3) = V_{\text{dc}}$. S_1 and S_4 are turned on thereby achieving zero-voltage switching (ZVS). Zero voltage derivative switching (ZVDS) can be achieved if v_{Cin} hits V_{dc} at the start of this mode thus $\mathrm{d}v_{\text{Cin}}/\mathrm{d}t|_{t=t_3} \propto i_{L1}(t_3) = 0$.

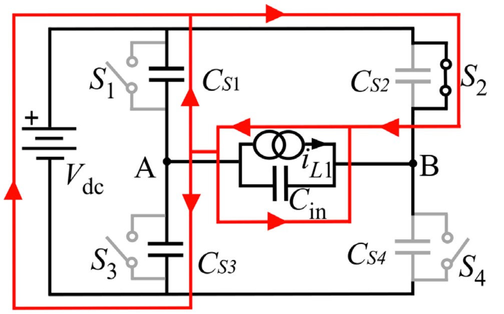
To ensure ZVS operation for an inductorless PT-based configuration, the critical criterion described in [11] is adapted. ZVS can be achieved for all load conditions if the input-to-output capacitance ratio meets $C_{in}/(N^2 C_{out}) \leq 2/\pi$ with $\pi/2$ total deadtime t_{total}. When the ZVS criterion is met, the resonant current i_{L1} must be in-phase with the gate signals, and thereby guaranteeing the total deadtime t_{total} begins at the negative peak of i_{L1} since this is where the quickest charging of C_{in} happens. This ensures the PT input voltage v_{Cin} is maximized by the end of the deadtime period. In this work, the output voltage is regulated by controlling Δt_2, and Δt_3 is controlled to ensure the total deadtime $t_{total} = \Delta t_1 + \Delta t_2 + \Delta t_3 = 1/(4f_s)$.

For the load conditions, the matched load corresponds to the highest efficiency point since it provides lowest resonant current. Therefore, a longer charging time is required for C_{in} during the deadtime. If ZVS is achievable at the matched load condition, ZVS can be achieved for all load conditions. The matched load is defined as

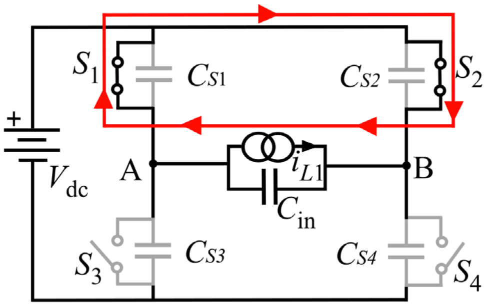
$$R_L = \frac{1}{2\pi f_0 C_{\text{out}}} \tag{1}$$

where $f_0 = 1/(2\pi\sqrt{L_1 C_1})$.

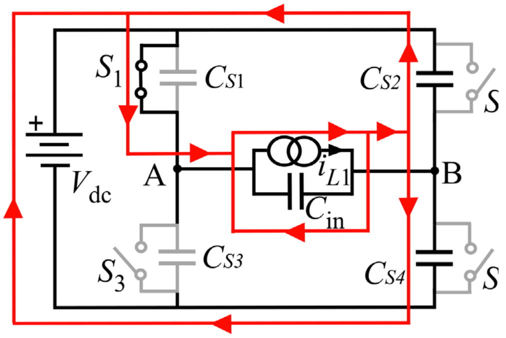
It should be noted that, although ZVS is achievable for C_{in}, ZVS also needs to be achieved for MOSFETs capacitance [21]. As can be seen from Fig. 3, the PT's resonant tank (L_1, C_1, R_1) can be modelled by a sinusoidal resonant current i_{L1}. During the total deadtime period t_{total}, the resonant current circulates in the resonant tank and charges the MOSFET capacitors and the PT input capacitance. The voltage across C_{in} is in the range $-V_{\text{dc}}$ to V_{dc} and, while it is charging, the voltage at the midpoint of each bridge is also increasing. At the start of M1, t_0, the left bridge v_A (i.e. C_{S1} and C_{S3}) is at 0 and the right bridge v_B (i.e. C_{S3} and C_{S4}) is at V_{dc}. At the end of M3, t_3, the left bridge v_A is at V_{dc} while right bridge v_B is at 0. When C_{in} is at 0 during M2, the voltage across the left bridge is equivalent to the right bridge. Therefore, if $v_A = v_B$ (while $v_A \neq 0$), turning on two MOSFETs results in losses due to MOSFET output capacitor discharge. If $v_A \neq v_B$, losses always occurs when two MOSFETs turned on since $v_A \neq 0$, or $v_B \neq 0$ or both.



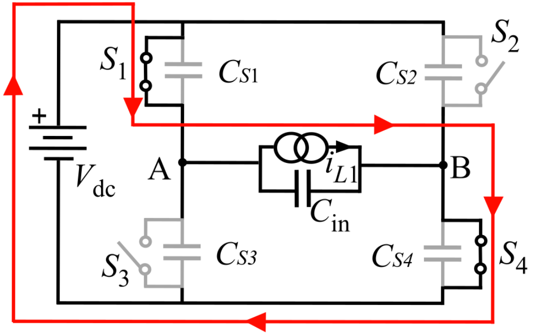
(a) Mode 1, $v_A(t_0)=0$, $v_A(t_1)=V_{\text{dc}}$, $v_B=V_{\text{dc}}$



(b) Mode 2, $v_A=V_{\text{dc}}$, $v_B=V_{\text{dc}}$



(c) Mode 3, $v_A=V_{\text{dc}}$, $v_B(t_2)=V_{\text{dc}}$, $v_B(t_3)=0$



(d) Mode 4, $v_A=V_{\text{dc}}$, $v_B=0$

Fig. 3. Proposed control sequence for the inductorless H-bridge PT-based inverter with equivalent circuit model. (v_A and v_B refer to the voltage on node A and B)

A new control (switching sequence) is implemented in this work (as shown in Fig. 3), such that the right hand bridge leg is turned off and output voltage of the right hand bridge is allowed to discharge from V_{dc} to 0 using the resonant current. Then the high-side MOSFET are turned on to obtain the 0V period (i.e. M2). The left-hand bridge leg is operated in a similar manner where it is turned off and its output voltage is charged to V_{dc}. Therefore, the switching loss can be eliminated in the MOSFETs.

B. *Controller description*

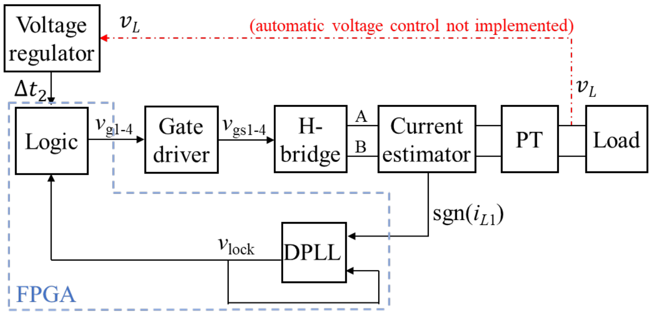


Fig. 4. Block diagram of the controller for a PT-based inverter.

TABLE I

STATE MACHINE OF THE CONTROLLER

Mode (state)	Gate signals v_{g1}	v_{g2}	v_{g3}	v_{g4}	Condition for mode to begin
M1$^+$	0	1	0	0	$\pi/2$ after M4$^-$
M2$^+$	1	1	0	0	$v_{C_{\text{in}}} = 0$
M3$^+$	1	0	0	0	Δt_2 after M2$^+$
M4$^+$	1	0	0	1	v_{lock}: 0→1
M1$^-$	1	0	0	0	$\pi/2$ after M4$^+$
M2$^-$	1	1	0	0	$v_{C_{\text{in}}} = 0$
M3$^-$	0	1	0	0	Δt_2 after M2$^-$
M4$^-$	0	1	1	0	v_{lock}: 1→0

+ and − represent the positive and negative half cycles

The block diagram of the proposed controller for H-bridge PT-based inverter is shown in Fig. 4. The control is performed dynamically by mix of digital and analogue techniques. The digital part is implemented by a field-programmable gate array (FPGA) together with a digital phase-locked loop (DPLL). The analogue part includes a current estimator.

Since the resonant current is internal to the PT and cannot be measured directly, we draw on our previous work where we developed a resonant current estimation circuit (using voltage sensing) [10]. As shown in Fig. 4, the resonant current is estimated and its direction sgn(i_{L1}) is given as an input to the

DPLL which ensures synchronisation of the gate signals to the resonant current. The DPLL output, v_{lock}, is used to indicate a DPLL locked condition. Therefore, sgn(i_{L1}) and v_{lock} are phase- and frequency-matched when the DPLL is locked on.

Programmable logic is used to generate the in-phase gate reference signals v_{g1} to v_{g4}. The logic implements a finite-state machine where the modes are the machine's states, as shown in Table I.

The modes progress in a single order from M1$^+$ to M4$^+$, then M1$^-$ to M4$^-$ and then restart at M1$^+$; the conditions for transition between modes are also shown. Under normal conditions, v_{lock} is in phase with sgn(i_{L1}). In our implementation, v_{Cin} is not measured, but the period of M1 (Δt_1) is calculated by solving (28).

Energy is input to the converter during M4 which lasts for half of each half cycle and begins when the current changes sign. M1, M2 and M3 are the deadtime. The period of M2, Δt_2, is controlled by the voltage regulator and holds v_{Cin} at zero during M2, reducing average power output to the load.

III. State-Variable Model Analysis

Since the operation of the circuit is divided into four modes (see the input capacitor voltage v_{Cin} in Fig. 2), then four piecewise state-variable models are required to describe the evolution of the state trajectories during a half-cycle period. Below, we use the technique described in [15] which models the cyclic behaviour of a converter using piecewise linear state-variable models. If the mode times are known, then the technique in [15] allows the cyclic mode initial condition $\boldsymbol{x}(t_0)$ to be determined and using (30).

In this section, a non-linear state-variable model is derived from the differential equations for the inductor current and capacitor voltages. This model is then decomposed into a piecewise linear model based on the operating modes previously described.

A. Stage I – Model Derivation

The inductor current is found from

$$\dot{i}_{L1} = \frac{v_{L1}}{L_1} = \frac{v_{\text{Cin}} - i_{L1}R_1 - v_{C1}}{L_1} - \frac{v_L}{NL_1} \tag{2}$$

The primary side capacitor voltage during M1-M4 is given by

$$\dot{v}_{C1} = \frac{i_{L1}}{C_1} \tag{3}$$

$$\dot{v}_{\text{Cin}} = \begin{cases} -\dfrac{i_{L1}}{C_{\text{in}}} & t_0 \le t < t_1 \\ 0 & t_1 \le t < t_2 \\ -\dfrac{i_{L1}}{C_{\text{in}}} & t_2 \le t < t_3 \\ 0 & t_3 \le t < t_4 \end{cases} \tag{4}$$

With the initial conditions: $v_{\text{Cin}}(t_0)=-V_{\text{dc}}$, $v_{\text{Cin}}(t_1)=0$, $v_{\text{Cin}}(t_2)=0$, $v_{\text{Cin}}(t_3)=V_{\text{dc}}$ and it is assumed that the circuit is operated in an appropriate manner to guarantee these conditions can be achieved.

The output voltage v_L is given by

$$\dot{v}_L = \dot{v}_{\text{Cout}} = \frac{i_{L1}}{NC_{\text{out}}} - \frac{v_L}{R_L C_{\text{out}}} \tag{5}$$

Combining (2)-(5) provides the complete state-variable model and coupling equations

$$\begin{bmatrix} \dot{i}_{L1} \\ \dot{v}_{C1} \\ \dot{v}_{\text{Cin}} \\ \dot{v}_L \end{bmatrix} = \begin{bmatrix} -\dfrac{R_1}{L_1} & -\dfrac{1}{L_1} & \dfrac{h_2(t)}{L_1} & -\dfrac{1}{NL_1} \\ \dfrac{1}{C_1} & 0 & 0 & 0 \\ \dfrac{-h_2(t)}{C_{\text{in}}} & 0 & 0 & 0 \\ \dfrac{1}{NC_{\text{out}}} & 0 & 0 & -\dfrac{1}{R_L C_{\text{out}}} \end{bmatrix} \begin{bmatrix} i_{L1} \\ v_{C1} \\ v_{\text{Cin}} \\ v_L \end{bmatrix} + \begin{bmatrix} h_1(t)\dfrac{V_{\text{dc}}}{L_1} \\ 0 \\ 0 \\ 0 \end{bmatrix} \tag{6}$$

where $h_1(t)$ and $h_2(t)$ are switching functions defined as

$$h_1(t) = \begin{cases} 0 & t_0 \le t < t_3 \\ 1 & t_3 \le t < t_4 \end{cases} \qquad h_2(t) = \begin{cases} 1 & t_0 \le t < t_1 \\ 0 & t_1 \le t < t_2 \\ 1 & t_2 \le t < t_3 \\ 0 & t_3 \le t < t_4 \end{cases} \tag{7}$$

B. Stage II – Decomposition into piecewise linear models

The state-variable model can be obtained from equation (6) and (7). For M1, it is given by (8).

$$\dot{\boldsymbol{x}} = \boldsymbol{A}_1\boldsymbol{x} + \boldsymbol{B}_1 \tag{8}$$

where $\boldsymbol{A}_1$ and $\boldsymbol{B}_1$ are defined as

$$\boldsymbol{x} = \begin{bmatrix} i_{L1} \\ v_{C1} \\ v_{\text{Cin}} \\ v_L \end{bmatrix}, \quad \boldsymbol{A}_1 = \begin{bmatrix} -\dfrac{R_1}{L_1} & -\dfrac{1}{L_1} & \dfrac{1}{L_1} & -\dfrac{1}{NL_1} \\ \dfrac{1}{C_1} & 0 & 0 & 0 \\ -\dfrac{1}{C_{\text{in}}} & 0 & 0 & 0 \\ \dfrac{1}{NC_{\text{out}}} & 0 & 0 & -\dfrac{1}{R_L C_{\text{out}}} \end{bmatrix}, \boldsymbol{B}_1 = \begin{bmatrix} 0 \\ 0 \\ 0 \\ 0 \end{bmatrix} \tag{9}$$

In M2, v_{Cin} is maintained at zero, thus $\dot{v}_{\text{Cin}} = 0$. Hence, M2 can be described as

$$\dot{\boldsymbol{x}} = \boldsymbol{A}_2\boldsymbol{x} + \boldsymbol{B}_2 \tag{10}$$

$$\boldsymbol{A}_2 = \begin{bmatrix} -\frac{R_1}{L_1} & -\frac{1}{L_1} & 0 & -\frac{1}{NL_1} \\ \frac{1}{C_1} & 0 & 0 & 0 \\ 0 & 0 & 0 & 0 \\ \frac{1}{NC_{\text{out}}} & 0 & 0 & -\frac{1}{R_L C_{\text{out}}} \end{bmatrix}, \boldsymbol{B}_2 = \begin{bmatrix} 0 \\ 0 \\ 0 \\ 0 \end{bmatrix} \tag{11}$$

Due to symmetric behaviour of the system, the model matrices for M3 are equivalent to M1, i.e. $\boldsymbol{A}_3 = \boldsymbol{A}_1$, $\boldsymbol{B}_3 = \boldsymbol{B}_1$.

For M4, v_{Cin} is maintained at V_{dc}, hence $\dot{v}_{C\text{in}} = 0$. M4 is defined as

$$\dot{\boldsymbol{x}} = \boldsymbol{A}_4\boldsymbol{x} + \boldsymbol{B}_4 \tag{12}$$

$$\boldsymbol{A}_4 = \begin{bmatrix} -\frac{R_1}{L_1} & -\frac{1}{L_1} & 0 & -\frac{1}{NL_1} \\ \frac{1}{C_1} & 0 & 0 & 0 \\ 0 & 0 & 0 & 0 \\ \frac{1}{NC_{\text{out}}} & 0 & 0 & -\frac{1}{R_L C_{\text{out}}} \end{bmatrix}, \boldsymbol{B}_4 = \begin{bmatrix} \frac{V_{\text{dc}}}{L_1} \\ 0 \\ 0 \\ 0 \end{bmatrix} \tag{13}$$

Finally, from the state-variable descriptions of each mode, and the time interval of each mode, the inverter operation in a cyclic mode can be determined.

IV. Modelling Cyclic Mode Behaviour

The proposed cyclic modelling is described as an extended Floquet-based method [22], by determining steady-state values of state-variables. It is an alternative to integration-based [11] methods and the state-space averaging technique [23] often used to model the periodically switching networks.

During a half cycle, the circuit operation is decomposed into four operating modes (M1→ M4, from $t=t_0$ to $t=t_4$), depending on the switch state, as shown by the waveforms given in Fig. 4. Therefore, the system in each mode can be described by the piecewise linear equation

$$\dot{\boldsymbol{x}}(t) = \boldsymbol{A}_i\boldsymbol{x}(t) + \boldsymbol{B}_i \tag{14}$$

where $\boldsymbol{x}(t)$ is the state vector, i is the mode index, $\boldsymbol{A}_i$ and $\boldsymbol{B}_i$ are the dynamical matrix and the input vector, respectively. Therefore, for $t_{i-1} \leq t \leq t_i$, the evolution of the state vector is given as

$$\begin{aligned} \boldsymbol{x}(t) = {} & \exp(\boldsymbol{A}_i(t - t_{i-1}))\boldsymbol{x}(t_{i-1}) \\ & + \int_{t_{i-1}}^{t} \exp(\boldsymbol{A}_i(t - \tau))\boldsymbol{B}_i d\tau \end{aligned} \tag{15}$$

Assuming the input voltage is constant for the duration of a mode, the state vector $\boldsymbol{x}(t)$ at $t=t_i$ can be solved from the state vector value at t_{i-1} using,

$$\begin{aligned} \boldsymbol{x}(t_i) &= \exp(\boldsymbol{A}_i(t_i - t_{i-1}))\boldsymbol{x}(t_{i-1}) \\ &\quad + \int_{t_{i-1}}^{t_i} \exp(\boldsymbol{A}_i(t_i - \tau))\boldsymbol{B}_i d\tau \\ &= \exp(\boldsymbol{A}_i d_i T_s)\boldsymbol{x}(\boldsymbol{t}_{i-1}) + \boldsymbol{A}_i^{-1}(\exp(\boldsymbol{A}_i d_i T_s) \\ &\quad - \boldsymbol{I})\boldsymbol{B}_i \\ &= \Phi_i \boldsymbol{x}(\boldsymbol{t}_{i-1}) + \boldsymbol{\Gamma}_i \end{aligned} \tag{16}$$

where $\boldsymbol{I}$ is the identity matrix, $\boldsymbol{\Phi}_i = \boldsymbol{\Phi}(t_i, t_{i-1}) = \exp(\boldsymbol{A}_i d_i T_s)$, $\boldsymbol{\Gamma}_i = \boldsymbol{A}_i^{-1}(\exp(\boldsymbol{A}_i d_i T_s) - \boldsymbol{I})\boldsymbol{B}_i$ and d_i is the duty cycle for the i^{th} mode: $d_i T_s = t_i - t_{i-1}$

Therefore, the complete cyclic-mode of the system can be determined from (16) once the initial circuit condition $\boldsymbol{x}(t_0)$ has been found, which has the form

$$\boldsymbol{x}(t_0) = [i_{L1}(t_0) \quad v_{C1}(t_0) \quad v_{C\text{in}}(t_0) \quad v_L(t_0)]^{\text{T}} \tag{17}$$

The values of the state-variables at the end of M1 are found from

$$\boldsymbol{x}(t_1) = \Phi_1 \boldsymbol{x}(t_0) + \boldsymbol{\Gamma}_1 \tag{18}$$

Similarly, at the end of mode 2, the state is given by

$$\boldsymbol{x}(t_2) = \Phi_2 \boldsymbol{x}(t_1^+) + \boldsymbol{\Gamma}_2 \tag{19}$$

where $\boldsymbol{x}(t_1^+)$ is the value of $\boldsymbol{x}$ immediately after the possible discontinuity in the state-variables at $t=t_2$ caused by the turning-on of S_3 & S_4 to clamp v_{Cin} at 0,

$$\boldsymbol{x}(t_1^+) = [i_{L1}(t_1) \quad v_{C1}(t_1) \quad 0 \quad v_L(t_1)]^{\text{T}} \tag{20}$$

From (19) and (20), a new matrix $\boldsymbol{K}$ can be introduced to reset the existing $v_{C\text{in}}$ to 0 at each switching instant. Where $v_{C\text{in}}$ takes a new value, an additional vector $\boldsymbol{x}_i$, representing the discontinuity in v_{Cin} due to MOSFETs switching, sets the new value of $v_{C\text{in}}$. Therefore, (16) can be modified as

$$\boldsymbol{x}(t_i) = \Phi_i[\boldsymbol{K}\boldsymbol{x}(t_{i-1}) + \boldsymbol{x}_i] + \boldsymbol{\Gamma}_i \tag{21}$$

$$\text{where } \boldsymbol{K} = \begin{bmatrix} 1 & 0 & 0 & 0 \\ 0 & 1 & 0 & 0 \\ 0 & 0 & 0 & 0 \\ 0 & 0 & 0 & 1 \end{bmatrix}, \ \boldsymbol{x}_1 = \boldsymbol{x}_2 = \boldsymbol{x}_3 = \begin{bmatrix} 0 \\ 0 \\ 0 \\ 0 \end{bmatrix}, \quad \boldsymbol{x}_4 = \begin{bmatrix} 0 \\ 0 \\ V_{\text{dc}} \\ 0 \end{bmatrix} \tag{22}$$

These equations can be expanded to give the solutions of the state vector for M2, M3 and M4

$$\boldsymbol{x}(t_2) = \Phi_2\boldsymbol{K}\Phi_1\boldsymbol{x}(t_0) + \Phi_2\boldsymbol{K}\boldsymbol{\Gamma}_1 + \boldsymbol{\Gamma}_2 \tag{23}$$

$$\begin{aligned} \boldsymbol{x}(t_3) = {} & \Phi_3\boldsymbol{K}\Phi_2\boldsymbol{K}\Phi_1\boldsymbol{x}(t_0) + \Phi_3\boldsymbol{K}\Phi_2\boldsymbol{K}\boldsymbol{\Gamma}_1 \\ & + \Phi_3\boldsymbol{K}\boldsymbol{\Gamma}_2 + \boldsymbol{\Gamma}_3 \end{aligned} \tag{24}$$

$$\begin{aligned} \boldsymbol{x}(t_4) = {} & \Phi_4\boldsymbol{K}\Phi_3\boldsymbol{K}\Phi_2\boldsymbol{K}\Phi_1\boldsymbol{x}(t_0) \\ & + \Phi_4\boldsymbol{K}\Phi_3\boldsymbol{K}\Phi_2\boldsymbol{K}\boldsymbol{\Gamma}_1 + \Phi_4\boldsymbol{K}\Phi_3\boldsymbol{K}\boldsymbol{\Gamma}_2 \end{aligned} \tag{25}$$

$$+\Phi_4\boldsymbol{K}\boldsymbol{\Gamma}_3+\Phi_4\boldsymbol{x}_4+\boldsymbol{\Gamma}_4$$

By using the odd-symmetry behaviour of the inverter during a half-cycle $\boldsymbol{x}(t_4) = -\boldsymbol{x}(t_0)$, the initial condition of the cyclic mode $\boldsymbol{x}(t_0)$ can be given by

$$\begin{aligned}\boldsymbol{x}(t_0) &\\ = [-\boldsymbol{I}-\Phi_4\boldsymbol{K}\Phi_3\boldsymbol{K}\Phi_2\boldsymbol{K}\Phi_1]^{-1}&[\Phi_4\boldsymbol{K}\Phi_3\boldsymbol{K}\Phi_2\boldsymbol{K}\boldsymbol{\Gamma}_1\\ +\Phi_4\boldsymbol{K}\Phi_3\boldsymbol{K}\boldsymbol{\Gamma}_2+\Phi_4\boldsymbol{K}\boldsymbol{\Gamma}_3&+\Phi_4\boldsymbol{x}_4+\boldsymbol{\Gamma}_4]\end{aligned} \tag{26}$$

The value of the PTs input capacitor voltage v_{Cin} at t=t_3 in M3 can be found by substituting equation (23) into equation (24) to give

$$\begin{aligned}v_{\mathrm{Cin}}(t_3) = [0\ \ 0\ \ 1\ \ 0][&\Phi_3\boldsymbol{K}\Phi_2\boldsymbol{K}\Phi_1\boldsymbol{x}(t_0)\\ &+\Phi_3\boldsymbol{K}\Phi_2\boldsymbol{K}\boldsymbol{\Gamma}_1+\Phi_3\boldsymbol{K}\boldsymbol{\Gamma}_2+\boldsymbol{\Gamma}_3]\end{aligned} \tag{27}$$

The deadtime value $\Delta t_1 = t_1 - t_0$ can be found from M1 in (18) when v_{Cin} is charged from $-V_{dc}$ to 0, which is given by

$$v_{\mathrm{Cin}}(t_1) = 0 = [0\ \ 0\ \ 1\ \ 0][\Phi_1\boldsymbol{x}(t_0)+\boldsymbol{\Gamma}_1] \tag{28}$$

The output voltage v_L is found from

$$v_L(t) = [0\ \ 0\ \ 0\ \ 1]\boldsymbol{x}(t) \tag{29}$$

Where $\boldsymbol{x}$ can be found, during the i^{th} mode as

$$\begin{aligned}\boldsymbol{x}(t) = \exp\big(A_i(t-t_{i-1})\big)\,&\boldsymbol{x}(t_{i-1})\\ &+A_i^{-1}\big(\exp\big(A_i(t-t_{i-1})\big)-\boldsymbol{I}\big)\boldsymbol{B}_i\end{aligned} \tag{30}$$

V. Model Verification

A. Charge Equivalence for ZVS

For a given PT, ZVS performance can be evaluated by comparing the value of $v_{Cin}(t_3)$ to V_{dc}. In general, ZVS is achieved if v_{Cin} is charged to (or above) V_{dc} during M3, that is $v_{Cin}(t_3) \geq V_{dc}$.

To evaluate the ZVS performance, we use a measure of the zero-voltage switching potential called K_{ZVS}. K_{ZVS} is the normalised input capacitor voltage at the point of switch turn-on that would result if the voltage were not clamped by the body diodes of the MOSFETs. In practice, v_{Cin} is clamped and therefore we project the voltage by assuming that the same resonant current i_{L1} flows into an unclamped but otherwise identical circuit. This unclamped voltage is termed $\tilde{v}_{Cin}$ and defined with K_{ZVS} as

$$\tilde{v}_{\mathrm{Cin}} = \begin{cases}\dfrac{1}{C_{\mathrm{in}}}\displaystyle\int_{t_2}^{t} i_{L1}\mathrm{d}t\,, & t_2 \leq t \leq t_3\\ \text{undefined}, & t_2 > t > t_3\end{cases} \tag{31}$$

$$K_{\mathrm{ZVS}} = \frac{\tilde{v}_{\mathrm{Cin}}(t_3)}{V_{\mathrm{dc}}} \tag{32}$$

Fig. 5 shows the experimental waveform for v_{Cin} under the ZVS condition and illustrates the calculation method for K_{ZVS}. A ring-dot radial-mode PT (shown in Fig. 7(b)) is used for validation. It has the measured equivalent circuit components values given in Table II. The resonant current i_{L1} is reconstructed experimentally using the current estimation method we developed in [10]. The reconstructed current, $i_{L1,a}$, is fitted to a sine wave, $i_{L1,b}$, whose amplitude and phase are used, together with C_{in}, to estimate K_{ZVS}.

TABLE II
PT PARAMETERS

C_1	L_1	R_1	Q	C_{out}	C_{in}	N
77.8pF	17.2mH	12.5Ω	1190	1.14nF	0.43nF	0.94

The magenta trace in Fig. 5 is the measured input capacitor voltage, v_{Cin}. A black line presents the portion of $\tilde{v}_{Cin}$ which extends above V_{dc}. v_{g2} and v_{g4} are the gate signals. The charge required to change v_{Cin} from 0 to V_{dc} and $K_{ZVS}V_{dc}$ are given as Q_{t2ta} and Q_{t2t3}, shown as blue dashed box and orange region, respectively.

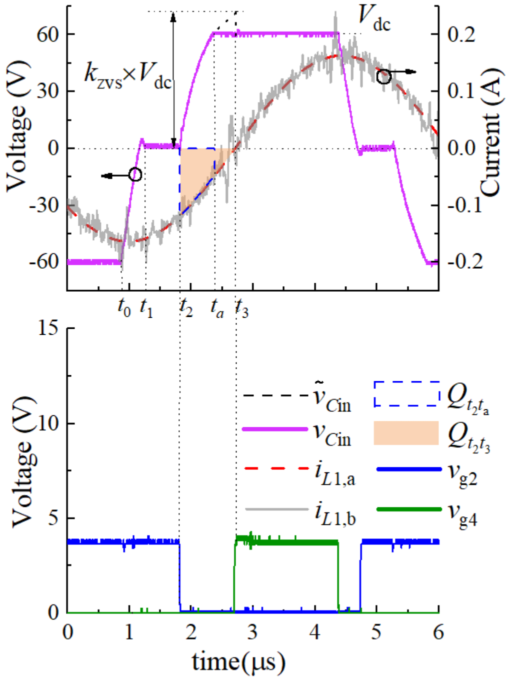


Fig. 5. Cyclic model and practical case of v_{Cin} under ZVS operation.

Q_{t2t3} can be found by integrating the resonant current during this deadtime period,

$$Q_{t2t3} = \int_{t2}^{t3} i_{L1}\mathrm{d}t \tag{33}$$

Evaluating (31), (32) and (33) at t_3 yields

$$K_{\mathrm{ZVS}} = \frac{\frac{1}{C_{\mathrm{in}}}\int_{t_2}^{t_3} i_{L1}\mathrm{d}t}{V_{\mathrm{dc}}} = \frac{Q_{t2t3}}{C_{\mathrm{in}}V_{\mathrm{dc}}} \tag{34}$$

This definition is valid both for zero-switching and non-zero-switching.

To validate the charge equivalence concept, Kzvs is evaluated by the cyclic model, SPICE simulation and practical measurements, respectively. For the cyclic model, the extrapolated final value $\tilde{v}_{\mathrm{Cin}}(t_3)$ is used to represent K_{ZVS} from (32). For the SPICE simulation, the PT is implemented as Mason equivalent circuit (as shown in Fig. 1), and the H-bridge operates with MOSFETs body diodes. K_{ZVS} in these cases is calculated by using (33) and (34). The gate signals are used to provide precise timing of t_2 and t_3 for integration limits.

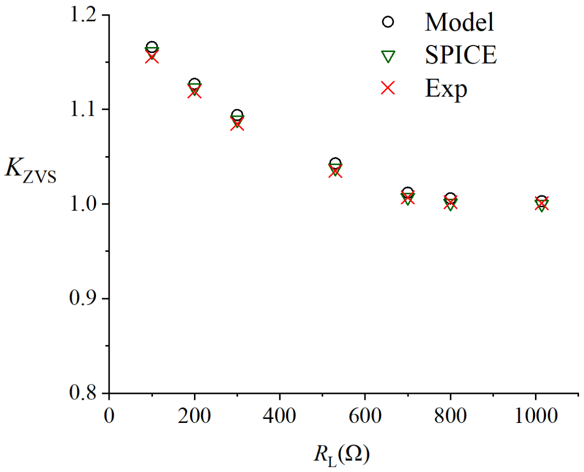


Fig. 6. K_{ZVS} comparison of cyclic model, SPICE and experimental results.

Fig. 6 shows a comparison of K_{ZVS} for the three methods. The cyclic model shows good agreement with the SPICE and experimental results, thereby providing evidence that the proposed cyclic mode is able to accurately predict ZVS ability of a PT-based inverter compared with practical case.

B. Experimental Result

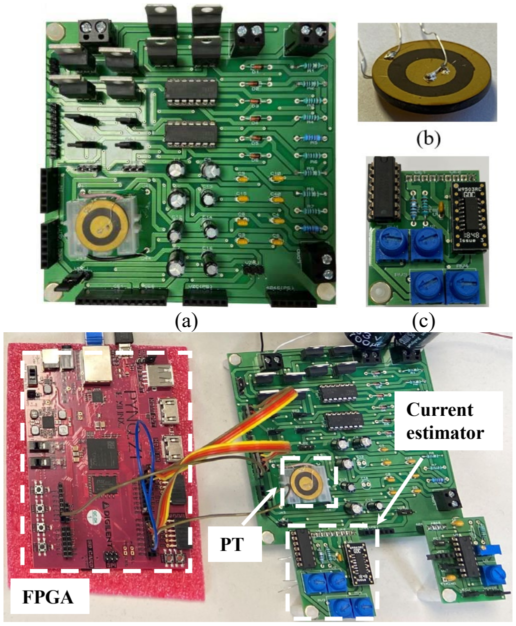

(a)
(b)
(c)
(d)

Fig. 7. (a) The prototype inductorless H-bridge PT-based inverter with (b) the ring-dot radial mode PT, (c) the resonant current estimation circuit and (d) the experimental platform.

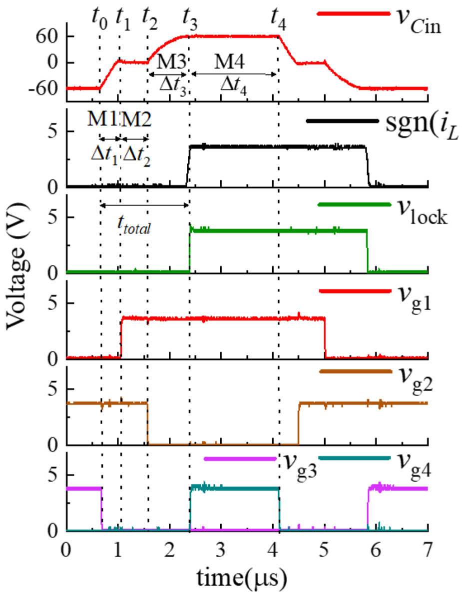


Fig. 8. Experimental measurements of the proposed H-bridge inverter.

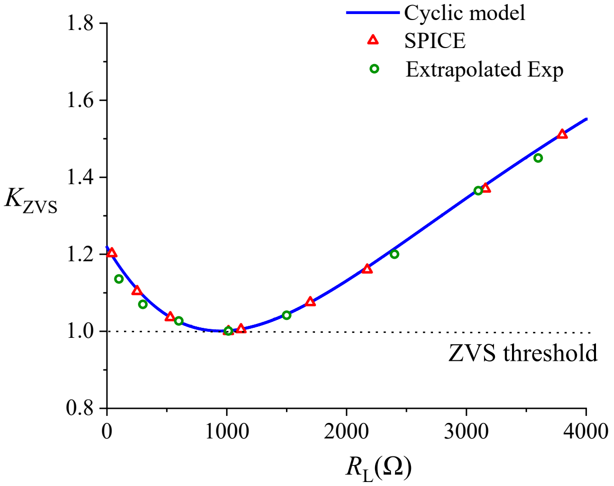
To verify the proposed cyclic modelling and to estimate the steady-state output voltage of a inverter, a prototype inverter based on the critical criterion [11] with a ring-dot radial-mode PT is employed, as shown in Fig. 7(a) and (b). A matched load (representing the worst case for achieving ZVS) of 1kΩ is used at the PT output. The current estimation technique developed in [10] was used (as shown in Fig. 7(c)) to estimate resonant current and indicate its direction $\mathrm{sgn}(i_{L1})$ for the FPGA control circuit (implemented by Xilinx Zynq-7000 PYNQ-Z1 as shown in Fig. 7(d)). The experimental setup is shown in Fig. 7(d) including the FPGA, the main board, the PT and the current estimation. The programmable logic generates the in-phase gate reference signals v_{g1} to v_{g4}. Fig. 8 shows the switching waveforms of the H-bridge inverter operating with the parameters listed in Table III. Signals $\mathrm{sgn}(i_{L1})$ and v_{lock} are the direction of the estimated resonant current and DPLL output signal, respectively. The duration of mode M1, Δt_1, where v_{Cin} increases from $-V_{\mathrm{dc}}$ to 0 in M1 can be found from (28) with initial condition of the cyclic mode $\boldsymbol{x}(t_0)$ from (26), while the duration of M3, Δt_3, can be found, for $K_{\mathrm{ZVS}} = 1$, from (27) by setting $v_{\mathrm{Cin}}(t_3) = V_{\mathrm{dc}}$. Subsequently, the time interval for M2 can be evaluated accordingly since the total deadtime $t_{\mathrm{total}} = 1/4f_s$ [11].

TABLE III
CIRCUIT OPERATING CONDITIONS

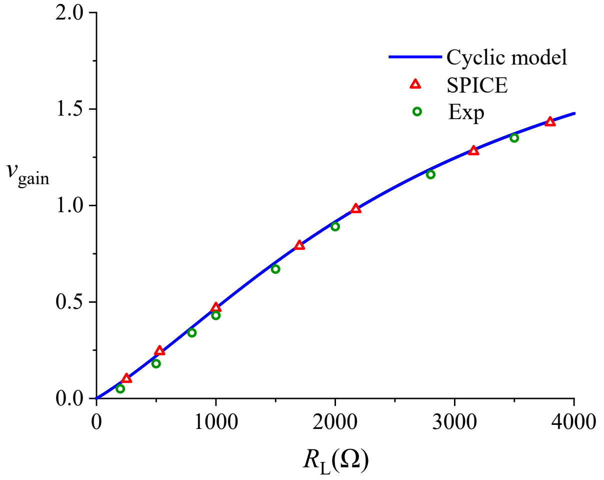
V_{dc}	f_s	Δt_1	Δt_2	Δt_3	R_L	$v_{L,\mathrm{RMS}}$
60V	145.3kHz	0.41μs	0.53μs	0.78μs	1kΩ	26.3V

As can be seen from Fig. 8, DPLL output signal v_{lock} is phase and frequency matched to the input signal $\mathrm{sgn}(i_{L1})$, indicating a DPLL locked operating condition. The zero crossings of resonant current are clearly indicated by $v_{\mathrm{zc},iL1}$, and ZVS is achievable as v_{Cin} reaches V_{dc} during the deadtime, that is $v_{\mathrm{Cin}}(t_3) \geq V_{\mathrm{dc}}$. Zero voltage derivative switching (ZVDS) is also obtained since the estimated current $i_{L1}(t_3) \propto \mathrm{d}v_{\mathrm{Cin}}/\mathrm{d}t|_{t=t_3} =$

0. This is to be expected since the radial-mode PT was design to meet the critical criterion described in [11].



(a)



(b)

Fig. 9. Model validation: (a) ZVS and (b) voltage gain of the H-bridge inverter

In Fig. 9, the ZVS and output voltage are illustrated as a function of load resistor R_L with the same circuit conditions and time intervals as given in Table III. Equation (27) can be used to evaluate ZVS performance of a given PT, and this is demonstrated in Fig. 9(a), where the ZVS factor K_{ZVS} is compared with SPICE simulation and experimental results. Experimental measurements for K_{zvs} are given as extrapolated values of $\tilde{v}_{Cin}(t_3)$ calculated using equation (34). As can be seen from Fig. 9(a), the input capacitor voltage v_{Cin} is normalised and represented as $K_{ZVS} = v_{Cin}(t_3)/(V_{dc})$. It is shown that the proposed cyclic model correlates well with the SPICE and experimental results. For this particular PT, ZVS is clearly achievable for all load resistor values, while the worst case occurs at the matched load condition where K_{ZVS}=1, which corresponds to the v_{Cin} waveform shown in Fig. 8. The RMS value of output voltage $v_{L,RMS}$ is normalised and given as the voltage gain $v_{gain}= v_{L,RMS}/(NV_{dc})$. As can be seen, the cyclic-mode model matches well with the simulation and experimental results.

VI. ZVS and Output Characteristics

A. Δt_1 Sensitivity Analysis

In general, the K_{ZVS} can be assessed quantitatively with (27), and this is done by controlling Δt_2. Since the range of Δt_2 variation is determined by Δt_1, the sensitivity of Δt_1 in terms of key circuit parameters should be evaluated initially.

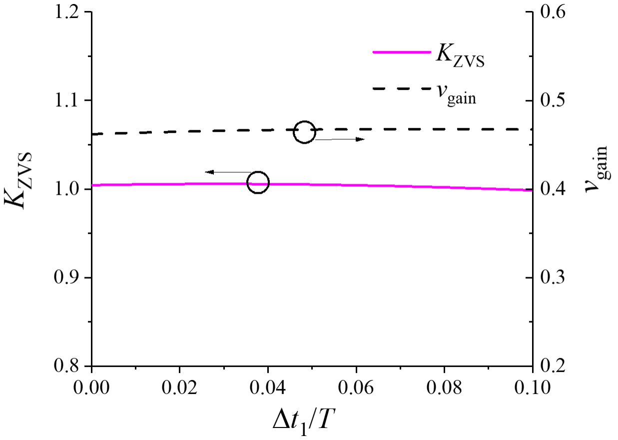


Fig. 10. Δt_1 sensitivity analysis for ZVS factor and voltage gain.

In Fig. 10, the ZVS factor K_{ZVS} and voltage gain v_{gain} are plotted against Δt_1 (deadtime in M1), and normalized to the switching period T_s (i.e. $1/f_s$). The same circuit parameters are used as in previous section. As can be seen, both K_{ZVS} and v_{gain} exhibit negligible change with Δt_1. Therefore, it is indicated that sensitivity of K_{ZVS} and v_{gain} to Δt_1 is low for modest changes in timing and the range of Δt_2 variation is fixed.

B. ZVS and Output Profile

The 3D plot shown in Fig. 11 illustrates the K_{ZVS} dependence on both load R_L and normalised operating frequency ($f_n = f_s/f_0$,, where f_s and f_0 are the switching frequency and resonant frequency) with the same fixed deadtime intervals employed to generate Fig. 8 (parameters are summarised in Table III). The K_{ZVS} curve in Fig. 9(a) is also indicated by the blue line in Fig. 11 for the same parameter range. As can be seen, this ring-dot PT exhibits two distinct regions where ZVS is achievable for the inductorless H-bridge configuration as indicated by the shaded areas. These two regions are located at high and low loads respectively and are barely connected at the matched load. Careful design of the PT could ensure the ZVS region can be maintained without disconnection for large load variations, and it brings the opportunity for output regulation since it is possible to simultaneously control Δt_2 (deadtime in M2), frequency and load to achieve ZVS continuously.

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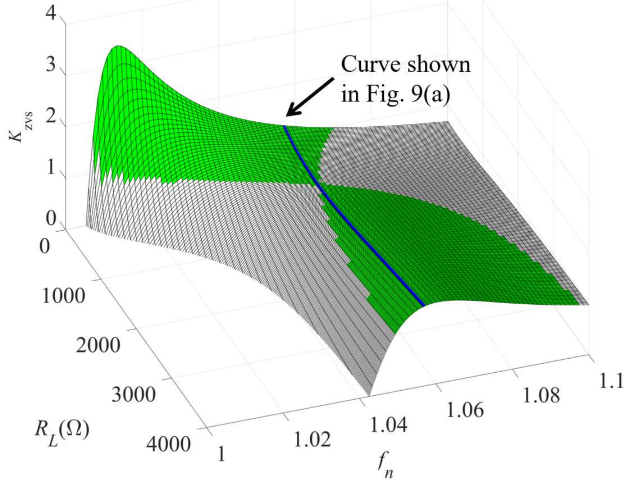
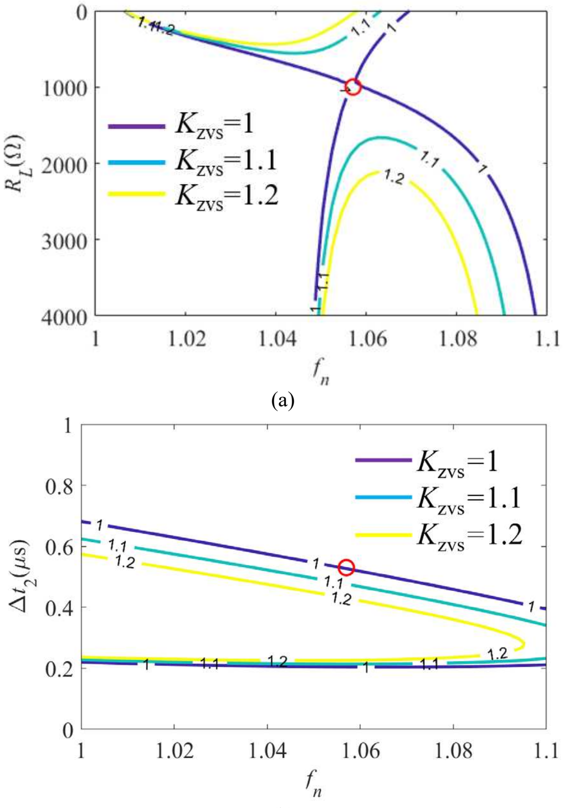


Fig. 11. ZVS characteristics for the radial-mode PT (shaded region is where $K_{\mathrm{ZVS}} \geq 1$).



(a)

(b)

Fig. 12. Contour plot of operating loci for the radial-model PT. (a) normalised frequency with load loci and (b) normalised frequency with time interval Δt_2 loci.

Expanding on the ZVS characteristics shown in Fig. 11, Fig. 12 shows the relationship between (a) the load and normalized frequency and (b) the time interval Δt_2 and normalised frequency for different K_{ZVS} conditions. The contour of $K_{\mathrm{ZVS}} = 1$ is equivalent to walking along the boundary of the shaded area in Fig. 11. The circuit operating condition listed in Table III is also indicated as a red circle in both Fig. 12 (a) and (b). In Fig. 12(a), ZVS is achievable at the matched load condition. To maintain ZVS, both switching frequency and Δt_2 should be varied simultaneously and a maximum of 0.45μs variation for Δt_2 is required (i.e. $K_{\mathrm{ZVS}}=1$), as shown in Fig. 12(b).

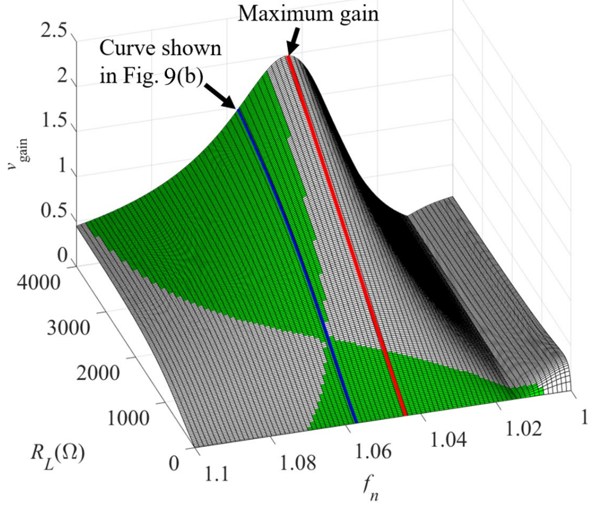


Fig. 13. Voltage gain profile of the radial-mode PT (shaded regions are where $K_{\mathrm{ZVS}} \geq 1$).

Fig. 13 shows the normalised output voltage gain characteristic with changes in both the operating frequency and the load for the same parameter range and circuit conditions with respect to Fig. 11. The voltage gain response corresponding to the conditions used to generate the Fig. 9(b) are indicated by the blue curve. As can be seen, the region of maximum achievable voltage gain is not completely covered by the ZVS region. The voltage gain increases with increasing load resistance, and for each load, the peak voltage gain occurs at $f_n = 1.043$ (shown as a red curve in Fig. 13). This can be further indicated in Fig. 14 (this is equivalent to the left-hand side view of Fig. 13), the matched load (red circle) and ZVS region (green area) are highlighted. As can be seen, $1.043 f_0$ clearly demonstrates the maximum gain condition among all the switching frequencies. This indeed indicates the optimal frequency for Δt_2 variation in order to obtain the maximum voltage gain for regulation.

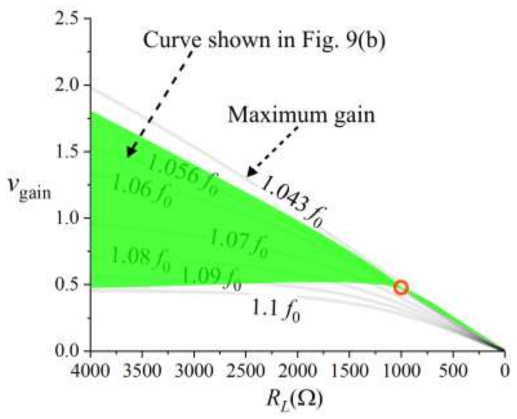


Fig. 14. Voltage gain operating loci of the radial-mode PT (shaded regions are where $K_{\mathrm{ZVS}} \geq 1$).

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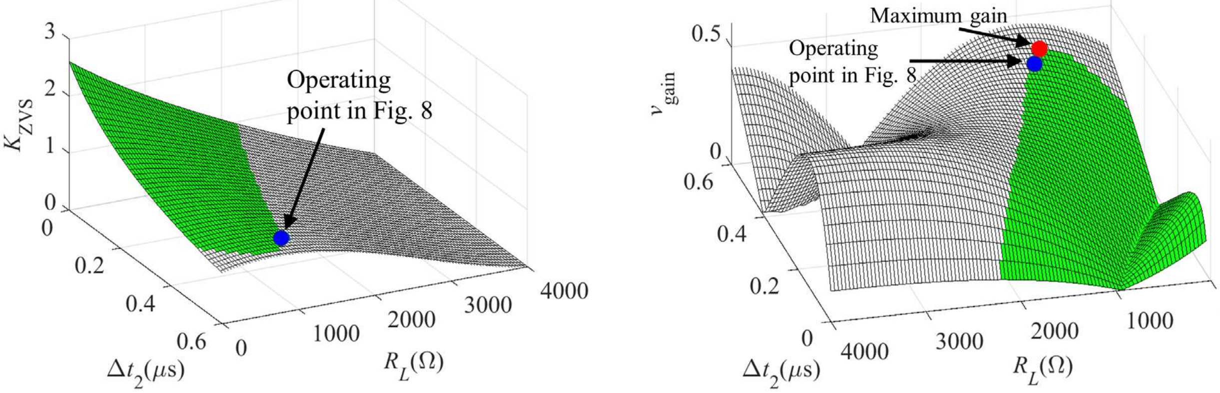
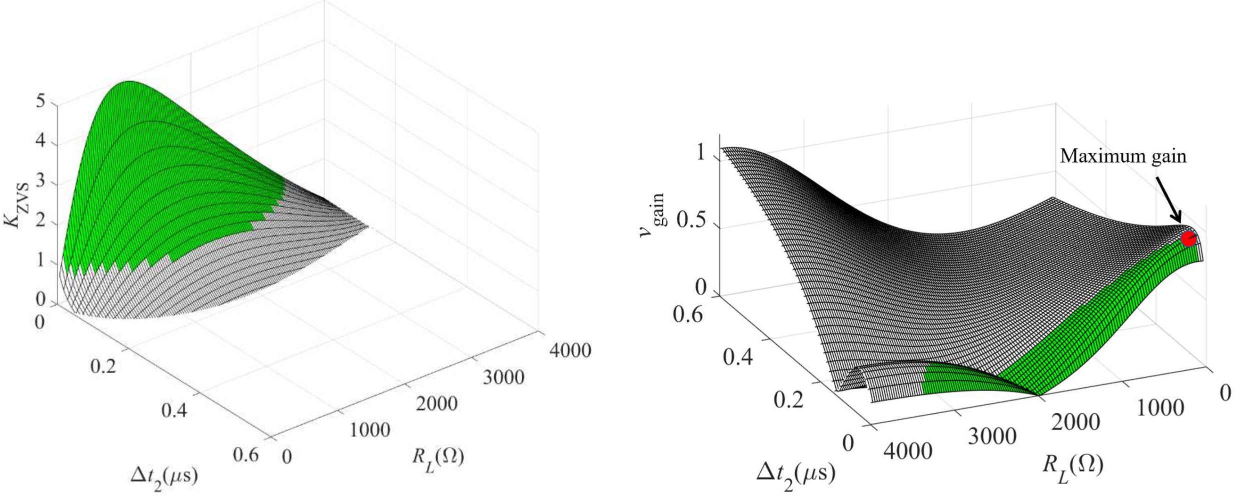


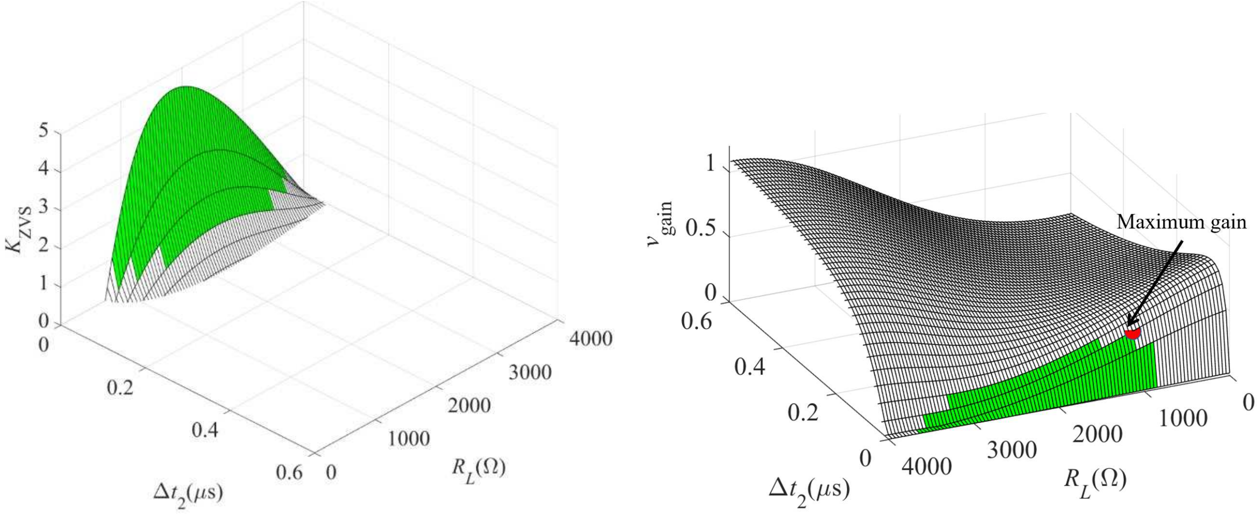
(a) K_{ZVS} at f_n=1.057

(b) v_{gain} at f_n=1.057



(c) K_{ZVS} at f_n=1.043

(d) v_{gain} at f_n=1.043



(e) K_{ZVS} at f_n=1.01

(f) v_{gain} at f_n=1.01

Fig. 15. ZVS profile and their corresponding normalised gain performance at (a) f_n=1.057, (b) f_n=1.043, (c) f_n=1.01(shaded region is where $K_{ZVS}\geq 1$).

VII. Simultaneous voltage regulation and ZVS

Although the highest efficiency can be achieved when the PT operates at the matched load condition, it is difficult to achieve ZVS for inductorless driven PTs under this condition in practice [24]. Moreover, it is difficult to regulate the output voltage while still achieving ZVS, since simultaneous parameter control should be employed and the ZVS region should be continuously connected during voltage regulation, as highlighted in [11][15][10]. Therefore, an analysis for achieving simultaneous ZVS and output voltage regulation is presented in this section based on the previous cyclic-mode analysis.

Fig. 15 highlights the K_{ZVS} and voltage-gain dependence on both the time interval Δt_2 and the load for f_n=1.057, f_n=1.043 and f_n=1.01. To demonstrate the ZVS and output voltage regulation ability, the analysis is performed with the same PT as used in the section V. By way of example, the operating locus for the condition f_n=1.057 is illustrated in Fig. 12. The duration required for Δt_1 can be calculated from (28) as 0.41µs, 0.406µs and 0.4µs, for each frequency respectively. The blue dot shown in Fig. 15(a) is the operating point for Fig. 8 (as indicated in Table III) and the blue dot on Fig. 15(b) is the gain calculated using Table II and III. These points are located at the boundary of the ZVS region ($K_{ZVS} = 1$ at the matched load). At the matched load condition, ZVS is no longer achievable when Δt_2 increases. This is to be expected as interval Δt_3 would be reduced accordingly to ensure total deadtime $t_{total} = 1/(4f_s)$ based on the design criterion [11], and as a result the input capacitor voltage v_{Cin} cannot reach V_{dc} during the deadtime. For the f_n=1.057 case, although ZVS can be continuously obtained over a wide range of operating conditions (as shown in Fig. 15(b)), the normalised voltage gain under ZVS region is relatively low (i.e. 0.43 maximum).

To achieve the maximum voltage gain under ZVS, the f_n=1.043 case performs the best as shown in Fig. 15(d). Although the ZVS region is reduced at 1.043f_0 compared with 1.057f_0, shown in Fig. 15(c), the corresponding voltage gain shown in Fig. 15(d) indicates a wide range of operation for output regulation with a maximum voltage gain of 0.9 at the 198 Ω load with 0.04 µs Δt_2. By comparison, in Fig. 15(b) and Fig. 15(f), the maximum achievable voltage gains are reduced to 0.43 and 0.42, respectively.

By way of example, Fig. 16 shows the practical load regulation performance of the proposed model at f_n=1.043 with 60V input voltage, ranging from 0.1 kΩ to 4 kΩ. As can be seen, by varying Δt_2 with a maximum of around 0.1 µs, the 4 k Ω case indicates the largest variation meanwhile still achieving ZVS. In addition, for this ring-dot radial mode PT, to ensure the voltage regulation is performed under ZVS, it is not recommended to operate at light load conditions since ZVS is no longer achieved. Fig. 17 shows the load regulation envelope at f_n=1.043 with input ranges from 20V-60V for the 5V output. The shaded green region is where ZVS is achieved. As can be seen, there are two distinctive regions (highlighted in dashed circle) where continuous voltage regulation can be achieved under ZVS. For example, to obtain a 5V output from a 60V input, the load should vary from 1.5kΩ to 1.8kΩ, and from 2.6kΩ to 3.3kΩ, to maintain ZVS.

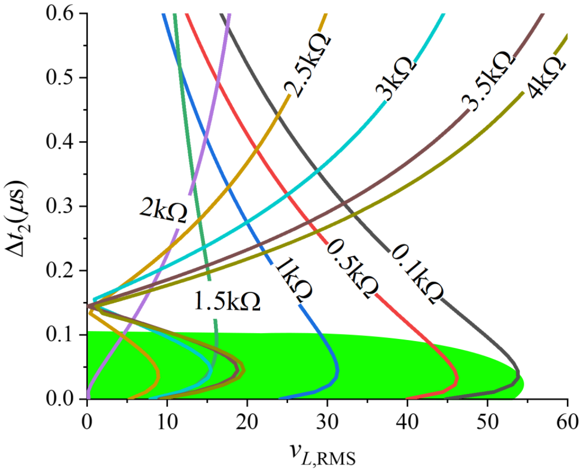


Fig. 16. Voltage regulation characteristics at 1.043f_0 under ZVS (shaded regions are where K_{ZVS}≥1).

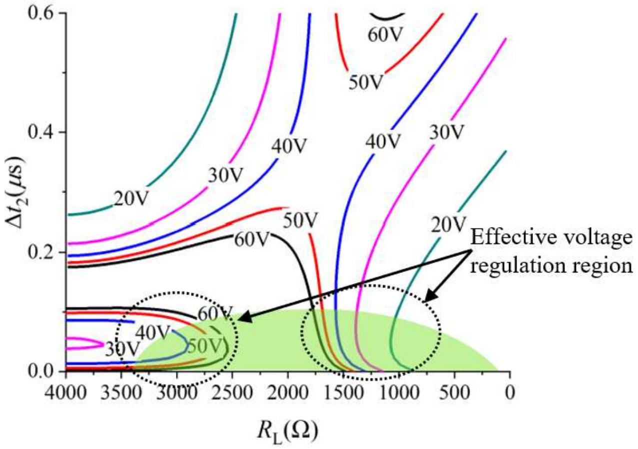


Fig. 17. Load regulation envelope at f_n=1.043 under ZVS for 5V output (shaded regions are where K_{ZVS}≥1).

The circuit performance using the cyclic model is compared with previous art and given in Table IV. To ensure a fair comparison, a ring-dot radial mode PT with the same parameters listed in Table II is employed. The proposed model shows the best performance since circuit behaviour can be clearly estimated. In addition, by varying Δt_2, voltage regulation can be performed with continuously achievable ZVS. Moreover, the proposed switching sequence enables ZVS for both MOSFET capacitance and PT.

TABLE IV
MODEL COMPARISON

Ref	ZVS region	Output characteristics	Simultaneous ZVS & voltage regulation	Regulation ability	
				Input	Output
[11]	predictable	unpredictable	not applicable	20V	5V
[15]	predictable	unpredictable	not applicable	20V	5V
[21]	predictable	predictable	not applicable	30V	5V
This work	predictable	predictable	applicable	15V-60V	5V

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VIII. Practical design considerations and discussion

Although the cyclic model presented in this paper mainly focuses on resistive loads, other types of load and output configurations are also applicable. In general, maximum power can be delivered to the load when the voltage gain of a PT is maximised. From the circuit design perspective regarding an output rectifier, it has been reported that, for a given PT, the AC output configuration gives a larger maximum PT output power compared to the DC output configuration [25]. From a PT design perspective, since the optimum operating frequency is changed from achieving highest efficiency to obtaining maximum voltage gain, the PT is not necessarily designed to achieve ZVS at the matched load condition (see Fig. 13, the maximum voltage gain occurs at f_n=1.04 while the lowest switching loss at matched load condition is at f_n=1.057). As a result, this would in turn reduce the PT dimension requirements (e.g. stacked disc-type Transoner PT), since the matched load indicates the highest efficiency point that requires smallest current (vibration velocity). If operating at matched load is no longer required, the critical criterion (i.e. the capacitor ratio, C_n) can be relaxed. For example, for a ring-dot PT, this might translate to requiring less electrode area on the output section. Relaxing the criterion reduces the mechanical current and improves the voltage gain [24].

For practical circuit design, the thermal performance should be considered since the frequency response of a PT depends on its piezoelectric properties (e.g. dielectric, elastic and piezoelectric constants [26]), which are temperature dependent. Temperature variation can change the frequency response of a PT by shifting the resonant frequency and decreasing the voltage gain, thereby limiting the regulation ability. One possible solution is using a PLL-based controller since it operates irrespective of circuit conditions [10].

In terms of the PT design, the quality factor change should be considered since it can be significantly reduced when a PT operates at high power levels due to vibration velocity [27] and heating [28]. The reduction of quality factor is associated with an increase of the damping resistor R_1, which further decreases the voltage gain.

Therefore, to investigate the ZVS and output voltage performance of a PT-based inverter for a temperature-dependent parameter variation, extreme value analysis should be used, and both extreme (e.g. no load/full load condition, zero and maximum Δt_2 time interval, extreme operating temperature) and expected circuit condition should be evaluated.

In general, with specified output voltage requirement, load and input range, the design process of achieving output voltage regulation under ZVS using the proposed model is summarised as follows: —

1) Generate K_{ZVS} and v_{gain} profiles using the cyclic model to find the optimum operating frequency which gives the maximum voltage gain.

2) After finding the optimum operating frequency, replot K_{ZVS} and v_{gain} with respect to the load and deadtime interval Δt_2.

3) Vary Δt_2, input voltage and load to see if this PT is able to meet voltage regulation requirement under ZVS using inductorless H-bridge configuration. If not, optimise the PT input-to-output capacitor ratio and repeat step 1, 2 and 3.

4) Build a prototype inverter and PT if both voltage regulation and ZVS can be achieved simultaneously.

To summarise, with the proposed switching sequence, ZVS can be obtained in both MOSFET capacitance and PT. By employing the proposed cyclic model, circuit behaviour can be estimated, the ZVS boundary and voltage gain as a function of circuit parameters (i.e. switching frequency and deadtime) are clearly demonstrated, and can be used to find the operating frequency for achieving maximum voltage gain. Subsequently, by controlling the time interval Δt_2 and input voltage at the optimum frequency, the output voltage regulation can be realised with continuously achievable ZVS.

X. Conclusion

A methodology for estimating the ZVS and output voltage ability of an inductorless driven PT-based inverter is presented. A new control sequence is developed to ensure ZVS for both PT and MOSFET capacitance. A new concept for output voltage regulation by controlling deadtime interval is demonstrated. Through the application of cyclic-mode analysis, an analytical model of the PT under ZVS operation is derived. Measurements taken from a radial-mode PT is used to validate the proposed model. Subsequently, the model is employed to show the ZVS profile, ZVS boundary and the requirement for continuously achieving ZVS. By using an H-bridge configuration, the output can be controlled by varying the deadtime period. Furthermore, the optimum operating frequency for maximum voltage gain is demonstrated under continuous ZVS region. The output voltage characteristics of the radial-mode PT is generated at different frequencies, highlighting the importance of PT selection in order to obtain maximum achievable voltage gain meanwhile still achieving ZVS. Since the ZVS and output regulation ability is dependent on input capacitance, deadtime period, resonant current and operating frequency, the proposed model can be used to assess the appropriateness of the PT for a given application. Potential areas for the further development include developing a second control loop for the automatic voltage control.

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