Proceedings Paper:
Vardhan, H. and Das, A. (2017) Analysis of space vector diagram of a modular H-Bridge Converter with bypassed cells during fault condition. In: 2017 19th European Conference on Power Electronics and Applications (EPE'17 ECCE Europe). 2017 19th European Conference on Power Electronics and Applications (EPE'17 ECCE Europe), 11-14 Sep 2017, Warsaw, Poland. Institute of Electrical and Electronics Engineers (IEEE) . ISBN 9789075815276

https://doi.org/10.23919/epe17ecceeurope.2017.8098999

Analysis of Space Vector Diagram of a Modular H-Bridge Converter with Bypassed Cells during Fault Condition

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Keywords

«Modular H-bridge», «Common mode voltage», «Fault tolerant operation», «Irregular six sided polygon», «Space Vector Diagram».

Abstract

This paper proposes a new analysis for the fault tolerant operation of Modular H-Bridge Converter using space vector diagram. The converter can be operated during fault condition after bypassing of faulty cells. Geometrical analysis is included to create balanced line voltages from unbalanced pole voltages due to bypass of faulty cells. The space vector diagram of unbalanced pole voltages becomes an irregular six sided polygon and depending on the number of cells faulty, the space vector diagram alters its shape. Sine-triangle based implementation of the space vector diagram is used to derive a general expression for common mode voltage. The modulation index is maximized by addition of common mode voltage. The biggest circle inscribed the irregular six sided polygon gives an expression for the maximum modulation index. The modified reference waveform is used in Level Shifted Pulse Width Modulation (LSPWM) technique for the converter topology. Simulation and experimental results are included to validate the proposed strategy.

Introduction

Modular converter is very popular [1] and used in various applications like high power medium voltage electric drives, photo voltaic power generation, power quality equipment etc. [2]-[5]. It consists of several identical building blocks called Sub Modules (SM) or cells, in full bridge configuration as shown in Fig. 1. Modular structure of the converter gives advantage of generation of high voltage using low rated devices, easy scalability, lower voltage THD and Fault tolerant operation [6]-[8].

This paper focusses on fault tolerant operation of the converter, where some of the cells are bypassed after becoming faulty. The pole voltage (V_{ao}, V_{bo}, V_{co}) becomes unbalanced [9]-[12]. However, by adjusting the phase angles of the three reference signals, the line voltage can be made balanced [13]-[17]. It is found that the space vector diagram under unbalanced pole voltages becomes an irregular six sided polygon. Depending on the number of cells faulty, the space vector diagram alters its shape. Space Vector

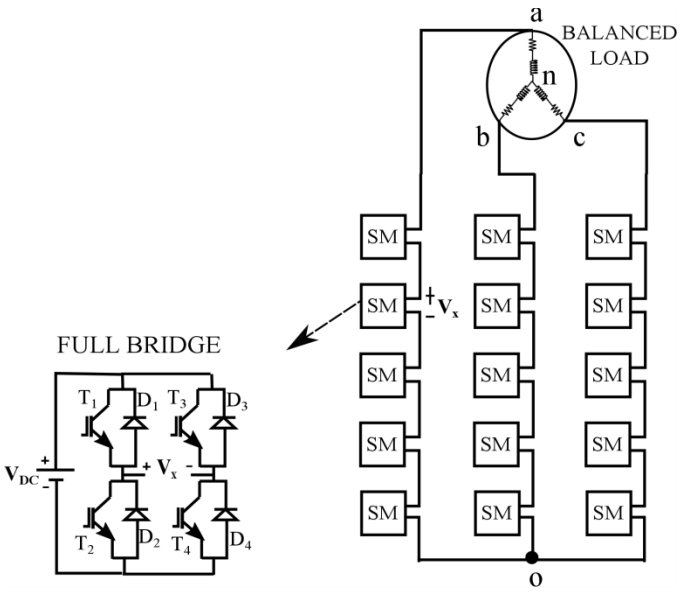

Fig. 1: Modular H-Bridge Converter

PWM (SVPWM) requires a proper combination of active and zero state vectors from space vector diagram to estimate a given voltage reference. In this paper, the equivalence in conventional SVPWM and Sine-triangle based PWM (SPWM) is derived. Sine-triangle based implementation of the space vector diagram is used to derive a general expression for common mode voltage. To obtain maximum line voltage possible, the modulation index is maximized by addition of common mode voltage. The biggest circle inscribed the irregular six sided polygon gives an expression for the maximum modulation index. The modified reference waveform will be used in level shifted pulse width modulation (LSPWM) technique for the converter topology. Simulation and experimental results is given to validate the proposed strategy.

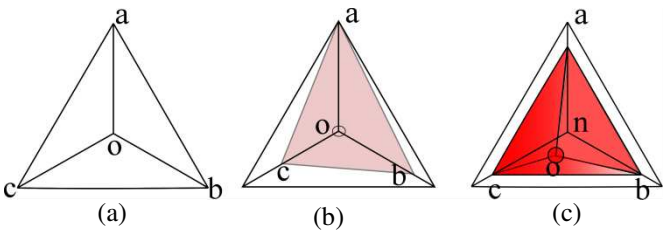

Fig. 2: Geometrical interpretation on (a) normal condition (b) fault condition and (c) modified bypassed fault condition.

Analysis of converter during fault

In order to continue the operation of the converter during faulty condition, the faulty cells should be bypassed. Fig. 2 represents the phasor diagram of pole and line voltages of the converter on normal condition, fault condition, and post-fault modified condition (here, the sides of the triangle represent the line voltages while the pole voltages are denoted by the median or arm sides of the triangle).During normal condition, all cells are operative in each phase. So balanced output voltage will be delivered as shown in Fig. 2(a). During fault condition when faulty cells are being bypassed intentionally, then output line voltage will be less and unbalanced as shown in Fig. 2(b). The angle between pole voltages is adjusted such that to produce balanced line voltages as shown in Fig. 2(c).

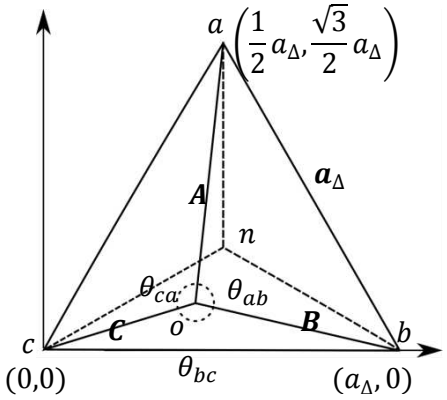

Fig. 3: Geometrical analysis

Geometrical analysis

An equilateral triangle can be formed by unequal pole voltages as shown in Fig. 2(c) which is redrawn in Fig. 3. The magnitude of the sides (a_Δ) represents balanced line voltages and is given by Eqn. (1) and the modified phase angles between the pole voltages are given in Eqn. (2)-(4). [18]

$$a_\Delta = \sqrt{0.5\left\{(A^2+B^2+C^2) + \sqrt{(6A^2B^2+6B^2C^2+6C^2A^2-3A^4-3B^4-3C^4)}\right\}} \quad (1)$$

By cosine rule, angles between pole voltages are found as,

$$\theta_{ab} = \cos^{-1}\left(\frac{A^2+B^2-{a_\Delta}^2}{2AB}\right) \quad (2)$$

$$\theta_{bc} = \cos^{-1}\left(\frac{B^2+C^2-{a_\Delta}^2}{2BC}\right) \quad (3)$$

$$\theta_{ca} = \cos^{-1}\left(\frac{\mathrm{A}^2+\mathrm{C}^2-{a_\Delta}^2}{2\mathrm{AC}}\right) \quad (4)$$

Please refer to Fig. 3 for variables used in above equations.

There occurs a condition for the formation of equilateral triangle as seen from Eqn. (1). This condition is concluded from the term present under the square root in Eqn. (1) which must be greater than or equal to zero. The condition states that the sum of the two (among A, B and C) should always be

greater than or equal to the third one. All combinations forming equilateral triangle for Modular H-Bridge converter containing 5 cells in each phase are tabulated in **Table I.**

Generation of three phase SPWM reference signals

In this paper, notation $[A\ B\ C]$ is used to denote the cell configuration of the converter after bypassing the faulty cells, where A, B and C are positive integers indicating the number of operative cells in phase a, b and c respectively. For $[A\ B\ C]$ configuration, the three reference signals with adjusted phase angle for Sine-PWM (SPWM) technique are given as,

$$V_a = A\cos(\omega t) \tag{5}$$

$$V_b = B\cos(\omega t - \theta_{ab}) \tag{6}$$

$$V_c = C\cos(\omega t + \theta_{ca}) \tag{7}$$

Since, the three reference signals are not having equal magnitudes; SPWM technique requires three carrier signals with amplitude of A , B and C respectively for three phases for proper utilization of the DC bus.

In normal operation of converter (say $[A\ A\ A]$), the reference signals are having equal magnitudes with $120°$ phase difference. Equal carrier signals are compared with the three balanced reference signals to produce gate signals. In order to work in the linear modulation region, the magnitude of reference signals should be less than or equal to carrier signal peak. During over modulation, lower frequency harmonics comes in the pole voltage waveform which is not desirable. Space Vector based PWM (SVPWM) technique increases the magnitude of voltage obtainable from converter by the factor of 1.1547 times to the magnitude of voltage obtained from SPWM technique under balanced condition. This maximum modulation index (m_a) over linear range can also be obtained from SPWM technique by adding common mode component (V_{cm}) to the three balanced reference signals which is expressed generally as Eqn. (8).

$$V_{cm} = \frac{-(max\{V_a, V_b, V_c\} + min\{V_a, V_b, V_c\})}{2} \tag{8}$$

The modified reference signals can be found as,

$$V_x{}^* = V_x + V_{cm} \qquad \forall\, x \in \{a, b\ and\ c\}\ phases \tag{9}$$

For $[A\ B\ C]$ configuration, V_x given by Eqn. (5)-(7) along with common mode component are used for generation of modified reference signals for carrier based implementation of SVPWM technique. The following section covers Space Vector diagram analysis of a Modular H-Bridge converter with bypassed cells during fault condition and equivalence of SVPWM and SPWM technique is shown by finding the general expression of common mode voltage component under unbalanced condition.

Space Vector Diagram for general [A B C] configuration

In terms of the instantaneous pole voltages, the space vector of pole voltage is defined as,

$$\overrightarrow{V_S}(t) = V_\alpha(t) + jV_\beta(t) = V_{ao}(t)e^{j0^\circ} + V_{bo}(t)e^{j120^\circ} + V_{co}(t)e^{j240^\circ} \tag{10}$$

Note that, $V_{ao}(t), V_{bo}(t)$ and $V_{co}(t)$ can be balanced or unbalanced. For $[A\ B\ C]$ case, the three instantaneous fundamental pole voltages in normalized form (taking DC bus voltage as unity) are equal to reference signals as given in Eqn. (5)-(7). The parametric equation of α and β component in space plane mentioned in Eqn. (10) follows the trajectory of a circle under the balanced condition as well as unbalanced condition and is given by,

$$\sqrt{\left(V_\alpha(t)\right)^2 + \left(V_\beta(t)\right)^2} = \frac{\sqrt{3}}{2}(a_\Delta) \tag{11}$$

Thus, the reference voltage vector is of constant magnitude equal to $\frac{\sqrt{3}}{2}(a_\Delta)$ and rotating with uniform angular frequency. The maximum fundamental voltage produced by SPWM technique has magnitude equal to ' r_{SPWM}'.

$$r_{SPWM} = \frac{\sqrt{3}}{2} a_\Delta$$

With the addition of common mode voltage, under unbalanced condition, the magnitude of fundamental voltage is increased and has magnitude equal to the radius of maximum circle inscribed inside the irregular space vector diagram formed by the converter with bypassed faulty cells.

For analysis purpose, a hypothetical two-level Modular H-bridge converter under unbalanced condition is taken [19]-[20]. Thus eight voltage vectors as shown in Fig. 4(a) forms the boundary of the irregular space vector diagram for [A B C] configured Modular H-Bridge converter. Several properties of this irregular six sided space vector diagram as shown in Fig. 4(a) are found and are listed below:

1) The zero vectors splits into two non-zero vectors (V_0 and V_7) and they do not coincide with the origin.
2) If these two vectors are switched for equal duration of time, then the resultant vector is equivalent to the virtual zero vector and coincides with the origin.
3) The reference voltage vector is realized by the two adjacent active vectors and one virtual zero vector in any of these six sectors.
4) Opposite triangles in the irregular six sided polygon are congruent, thus forming six sectors with three types of triangles.
5) Some combination like [654], [543], [432], [321] are having same V_0 and V_7 non-zero vectors as shown in Fig. 4(b).

Using property (2) it is possible to derive the common mode voltage.

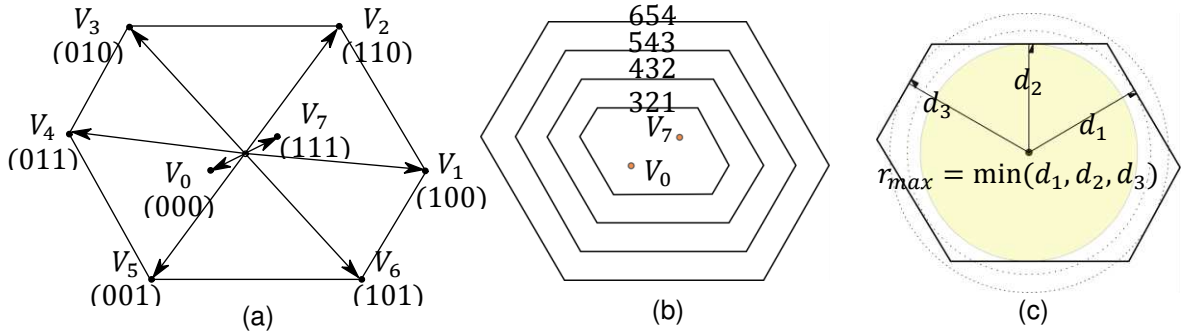

Fig. 4: a) Voltage Vectors, b) V_0 and V_7 vectors and c) Maximum modulation index calculation

The biggest inscribed circle in space vector diagram gives the maximum modulation index and thus maximum output balanced line voltage possible for the converter. In order to calculate the radius of the biggest inscribed circle, it is noted that the six sided polygon consists of three sets of congruent triangles and then any three consecutive sides are taken and the perpendicular distance from virtual zero vector is measured as shown in Fig. 4 (c). The minimum among these three distances will give the radius of maximum circle inscribed. Thus maximum value of modulation index (m_A) is defined as,

$$max\ (m_A) = \frac{r_{max}}{r_{SPWM}} \tag{12}$$

All possible cases of increased modulation index with faulty cells are obtained from Equation (12) and tabulated in **Table I**. The second column of the table indicates the maximum line voltage possible with sine triangle PWM. The third column shows the radius of the biggest inscribed circle inside the space vector diagram. The fourth column shows the increase in the modulation index that is possible by addition of common mode voltage.

The space vector diagram for different fault conditions is different. Some of the cases of different space vector diagram with maximum modulation index possible are presented in Fig. 5. The original space vector diagram is included in all for the comparison purpose.

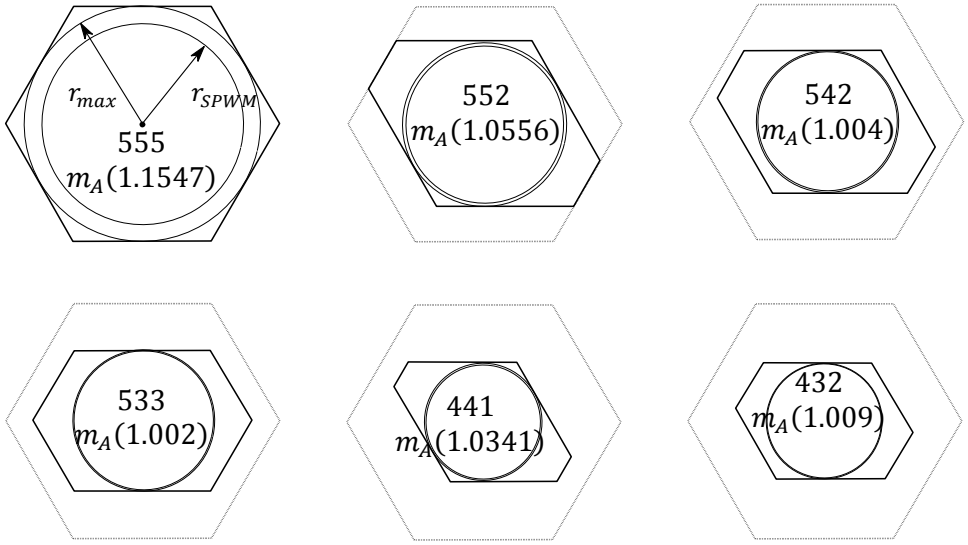

Fig. 5: Different Space Vector diagrams for different [A B C] cell configurations.

Table I: Maximum modulation index for different [A B C] configuration

$[A\ B\ C]$	r_{SPWM}	r_{max}	$max\ m_A$		$[A\ B\ C]$	r_{SPWM}	r_{max}	$max\ m_A$
555	8.66	10	1.154734		***441***	4.835	5	1.034126
554	8.047	9	1.118429		***433***	5.7	6	1.052632
553	7.368	8	1.085776		***432***	4.956	5	1.008878
552	6.631	7	1.055648		***431***	3.606	4	1.109262
551	5.841	6	1.027221		***422***	3.464	4	1.154734
544	7.453	8	1.073393		***333***	5.196	6	1.154734
543	6.766	7	1.034585		***332***	4.56	5	1.096491
542	5.972	6	1.004689		***331***	3.824	4	1.046025
541	4.583	5	1.090988		***322***	3.921	4	1.020148
533	5.988	6	1.002004		***321***	2.646	3	1.133787
532	4.359	5	1.147052		***222***	3.464	4	1.154734
444	6.928	8	1.154734		***221***	2.803	3	1.070282
443	6.306	7	1.110054		***211***	1.732	2	1.154734
442	5.605	6	1.070473		***111***	1.732	2	1.154734

Equivalence of Space Vector PWM and Sine PWM

For $[A\ B\ C]$ configuration the SPWM technique requires three carrier signals with amplitude V_{pa}, V_{pb} and V_{pc} which are equal to A, B and C respectively for three phases for proper utilization of the DC bus. The three reference voltages $V_a{}^*, V_b{}^*$ and $V_c{}^*$ (Eqn. (9)) are taken constant during the switching cycle as shown in Fig. 6 which are found by adding common mode voltage to the reference signals V_a, V_b and V_c.As shown in Fig. 6 by applying equal divisions of null vector time, three expressions of common mode component are found which is given in Eqn. (13).

$$V_{CM1} = -\left(\frac{\frac{V_c}{V_{pc}} + \frac{V_b}{V_{pb}}}{\frac{1}{V_{pc}} + \frac{1}{V_{pb}}}\right);\ V_{CM2} = -\frac{\left(\frac{V_a}{V_{pa}} + \frac{V_c}{V_{pc}}\right)}{\left(\frac{1}{V_{pa}} + \frac{1}{V_{pc}}\right)}\ and\ V_{CM3} = -\frac{\left(\frac{V_a}{V_{pa}} + \frac{V_b}{V_{pb}}\right)}{\left(\frac{1}{V_{pa}} + \frac{1}{V_{pb}}\right)} \quad (13)$$

There occurs three expressions of common mode voltage based on the location of V_a^*, V_b^* and V_c^*. One of the locations has been shown in Fig. 6, where T_7 is dependent on V_c^* (v_{min}) while T_0 is dependent on $V_b^*(v_{mid})$. Thus by applying equal dwell times, one expression of common mode voltage (V_{cm1}) is found as in Eqn. (13),

$$T_7 = T_0$$

$$\Rightarrow \frac{V_c^*}{V_{pc}} = \frac{V_b^*}{V_{pb}}$$

$$\Rightarrow \frac{V_c + V_{cm1}}{V_{pc}} = \frac{V_b + V_{cm1}}{V_{pb}}$$

If V_a^* is greater than a critical value (V_{cr});

$$V_{cr} = v_{mid}\frac{V_{pa}}{V_{pb}}$$

Then there exists another common mode V_{cm2} because T_0 is now dependent on $V_a^*(v_{max})$ while T_7 is dependent on V_c^* (v_{min}). Similarly V_{cm3} will exist when T_0 is dependent on $V_a^*(v_{max})$ and T_7 is dependent on V_b^* (v_{min}). Among the common mode voltages given in Eqn. (13), the common mode voltage V_{cm} which is added to the reference signals is given by the value which is middle of the above three.

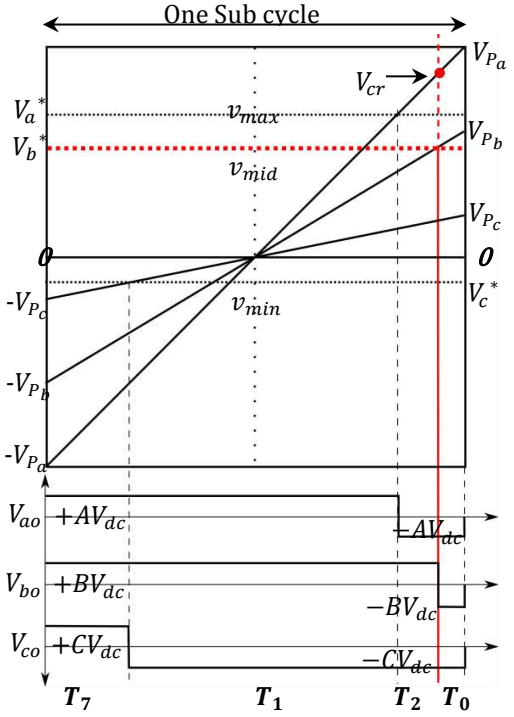

Fig. 6: Four segment switching sequence

$$V_{cm} = mid(V_{cm1}, V_{cm2}, V_{cm3}) \quad (14)$$

This common mode value is having fundamental component under unbalanced condition.

Fig. 7 shows the block diagram for the generation of three modified reference signals for $[A\ B\ C]$ configuration. V_x given by Eqn. (5)-(7) and common mode component given by Eqn. (14) are used for generation of modified reference signals for carrier based implementation of SVPWM technique. These modified reference signals are capable of giving balanced and maximum possible line voltage from the converter under faulty conditions. The next sections show the simulation and experimental results of the converter operating under fault conditions.

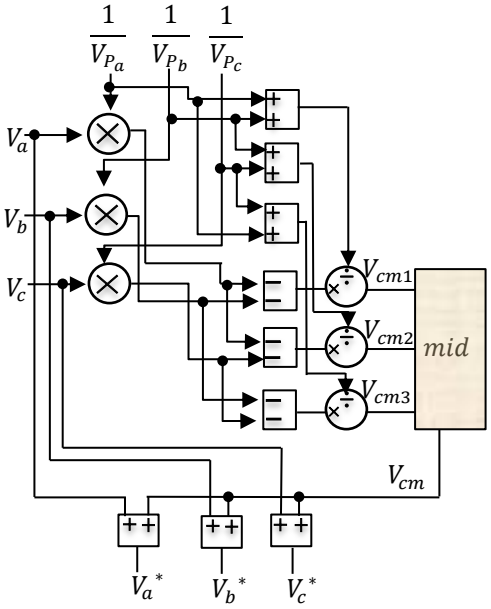

Fig. 7: Generation of three reference signals

Simulation Results

To verify the proposed concept, software simulation of modular H-Bridge converter with Level Shifted Pulse Width Modulation (LSPWM) is carried out. This section shows the simulation results with two cell configured converter i.e. [4 3 2] and [3 3 1]. Switching

frequency is 2 kHz and 1000 V DC bus voltage is given on each cell of the converter.

Fig. 8 shows the increase in linear modulation region for [3 3 1] configured converter after the addition of common mode voltage to its original reference signal (V_x). Modified reference signal (V_x^*) is also shown in the figure.

Fig. 9 and Fig. 10 shows the simulation results for the [4 3 2] and [5 5 1] configured converter respectively.

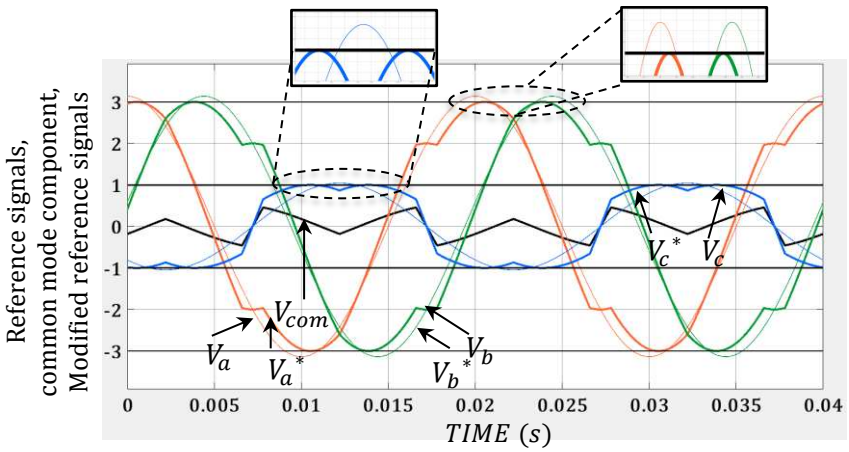

Fig. 8: Modified reference signal showing increase in *linear modulation range* for [3 3 1] configuration

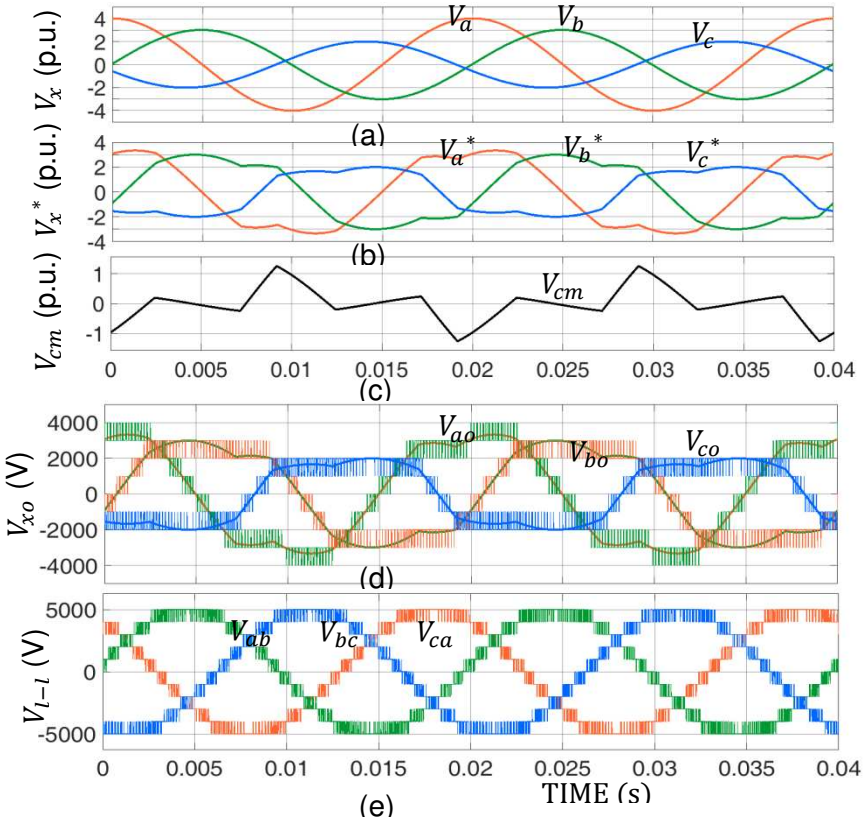

Fig. 9: Different waveforms for [4 3 2] configuration; (a) reference signals, (b) common mode voltage,(c) (a) reference signals after addition of common mode voltage, (d) output pole voltages and (e) balanced output line voltages.

Fig. 9(a) shows the three reference signals without the addition of common mode voltage (shown in Fig. 9(c)). The three modified reference signals which are compared with triangular carrier waveforms

are shown in Fig. 9(b). Now, LSPWM technique is implemented to produce gate signals to [4 3 2] configured converter. Pole voltages V_{ao}, V_{bo} and V_{co} are shown in Fig. 9(d) with 2489V, 2197V and 1541V RMS respectively. Pole voltages V_{ao}, V_{bo} and V_{co} are with 9, 7 and 5 voltage levels respectively Fig. 9(e) shows the balanced line voltages V_{ab}, V_{bc} and $V_{ca}$with equal RMS voltage of 3535 V.

Similarly results from [5 5 1] configuration are shown in Fig. 10. Fig. 10(a)-(c) shows its three reference signals and common mode voltage. Fig. 10(d) shows pole voltages V_{ao}, V_{bo} and V_{co} with 11, 11 and 3 voltage levels respectively. Pole voltages V_{ao}, V_{bo} and V_{co} are shown in Fig. 10(d) with 3450V, 3450V and 814.5V RMS respectively. Fig. 10(e) shows the balanced line voltages V_{ab}, V_{bc} and $V_{ca}$with equal RMS voltage of 4130 V.

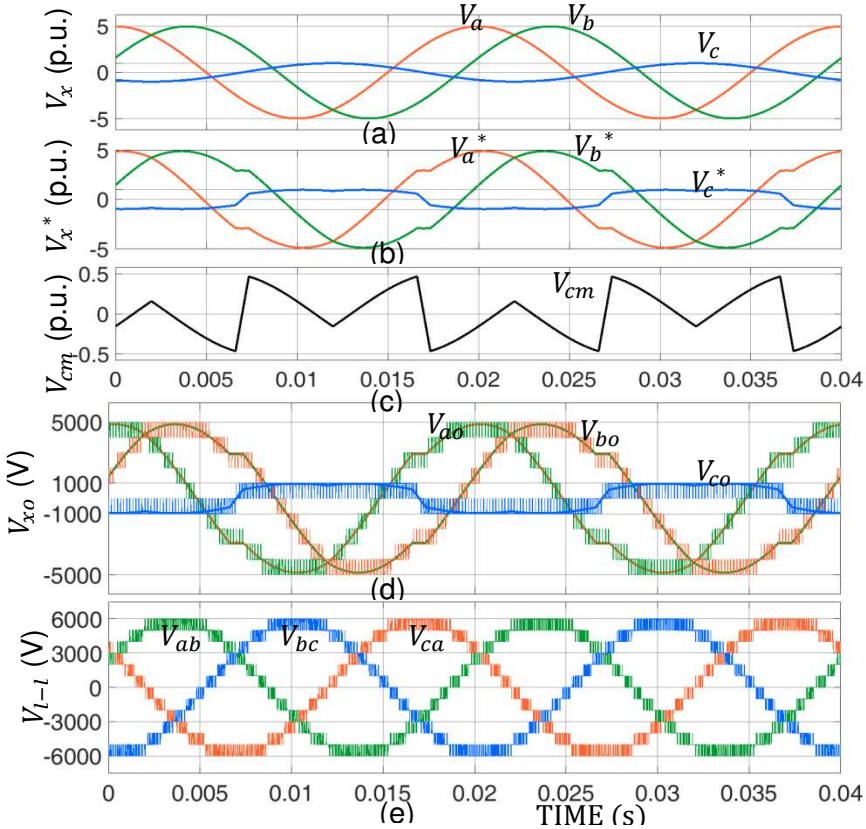

Fig. 10: Different waveforms for [5 5 1] configuration; (a) reference signals, (b) common mode voltage,(c) (a) reference signals after addition of common mode voltage, (d) output pole voltages and (e) balanced output line voltages.

Experimental Results

A prototype of the converter has been built in the lab. Results from cell configuration [3 3 1] is shown in Fig. 11 to Fig. 16. The DC bus voltage on each cell is maintained at 50 Volts. The modular H-Bridge converter is connected to a three phase induction motor. DAC output of the reference signal waveform of 'b' phase is shown in Fig. 11, after and before common mode addition. Fig. 12 shows the three unbalanced modulating waves from DAC of the DSP for the [3 3 1] configuration converter. The balanced line voltages of the reference signals (from DAC) can be seen from Fig. 13. Fig. 14 shows the output pole voltage V_{ao}, V_{bo} and V_{co} of CHB-MLC with 7, 7 and 3 voltage levels respectively. The RMS values are coming 106 V, 106 V and 41 V respectively. Fig. 15 shows the balanced line voltages V_{ab}, V_{bc} and V_{ca} which are 141 V, 140.6 V and 141 V (RMS) respectively. The balanced three line currents are shown in Fig. 16. All the experimental results are verifying the proposed strategy.

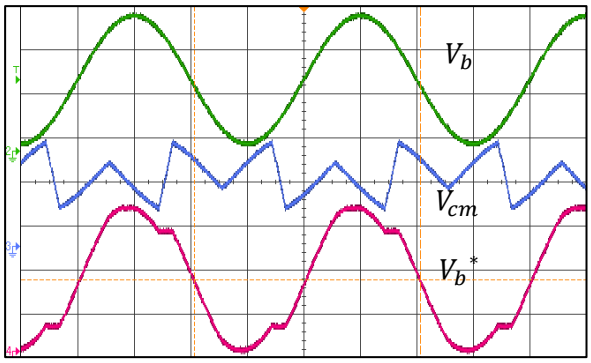

Fig. 11: DAC output of reference signals before and after addition of common mode voltage (2 V/div.)

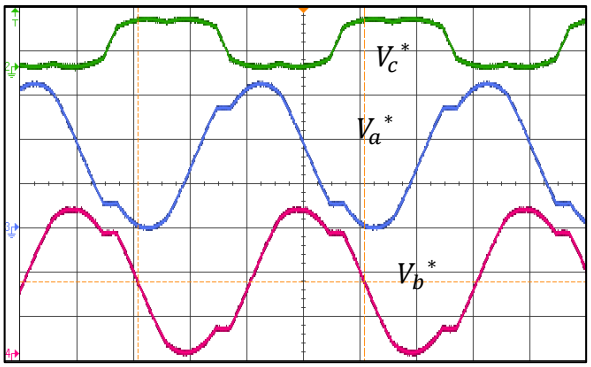

Fig. 12: DAC output of Modified reference signals (2V/div.)

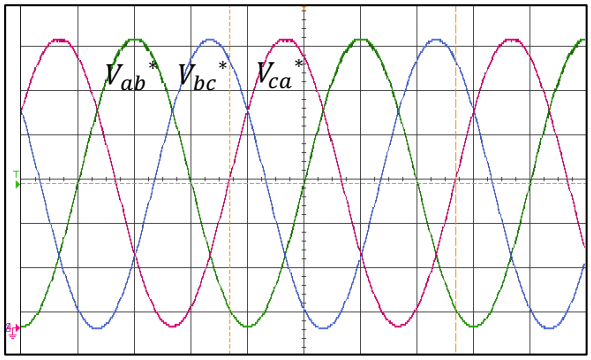

Fig. 13: DAC output of line voltage waveform for modified reference signals (1V/div.)

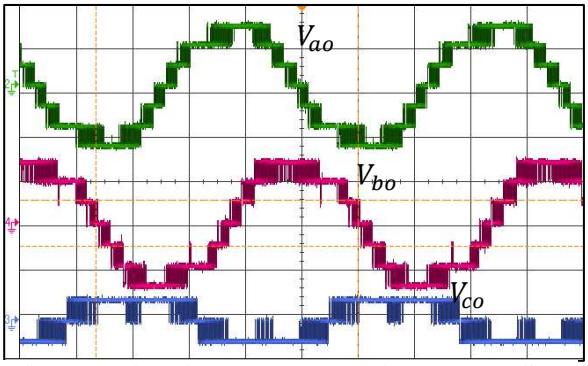

Fig. 14: Pole voltages V_{ao}, V_{bo} and V_{co} (100V/div.)

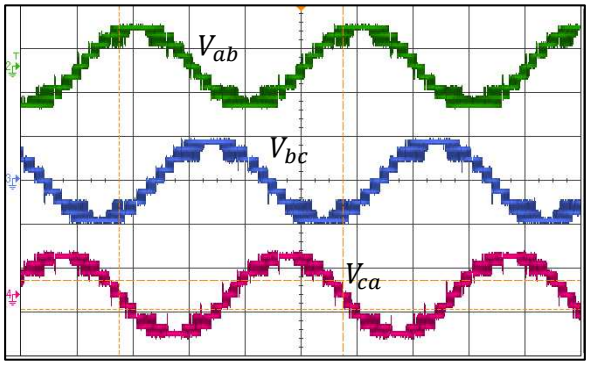

Fig. 15: Line voltages V_{ab}, V_{bc} and V_{ca} (200V/div.)

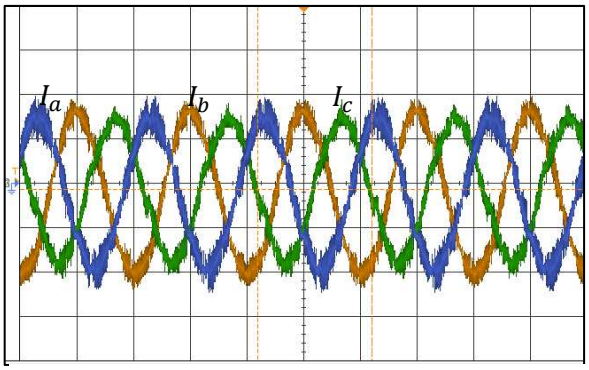

Fig. 16: Line currents I_a, I_b and I_c (200mA/div.)

Conclusion

This paper presents an analysis of the operation of Modular Cascaded H-Bridge Converter with bypassed cells during fault conditions. Geometrical analysis of the line voltage is undertaken for balancing the unbalanced pole voltages. The space vector diagram under unbalanced pole voltages is an irregular six sided polygon .The maximum modulation index is derived for all possible cases by inserting the biggest inscribed circle inside the six sided polygon. New general expression for common mode voltage is derived. Simulation results with Level Shifted Pulse Width Modulation are performed to operate the Modular Converter. Experimental results are also verified for this concept. The proposed analysis can be used for Cascaded H-Bridge converter feeding critical loads where service continuity is essential.

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