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Investigation on Shift in Threshold Voltages of 1.2kV GaN Polarization Superjunction (PSJ) HFETs

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***Abstract*—Shift in threshold voltages (V_{th}) of 1.2 kV P-GaN ohmic-gate Normally-on Polarization Superjunction (PSJ) HFETs are reported for the first time. Pulsed-mode measurement results of threshold voltage shifts under different gate stress biases are presented. A comprehensive analysis of threshold voltage shifts under different gate stress voltages and temperatures is discussed. Under positive gate stress voltages, hole trapping and accumulation processes in the u-GaN/AlGaN hetero-interface or the AlGaN layer induce more electrons, thereby causing negative shifts in threshold voltages. Conversely, under negative gate stress voltages, electrons captured by the buffer traps located in the GaN buffer or the traps in the AlGaN layer, cause positive shifts in threshold voltages. Moreover, recovery processes are observed under the positive and negative stress voltages. Temperature effects on the V_{th} are also evaluated through pulsed-mode measurements. Hole trapping processes are strengthened with temperature rise, causing more negative V_{th} shifts. However, thermally activated electrons from 2DEG and strengthened recovery processes result in positive V_{th} shifts at higher temperatures, compensating the influences from the increasing hole trapping processes. The results confirm that the current collapse is quite low in PSJ HFETs**

***Index Terms*—Gate stress, Polarization Superjunction (PSJ), holes injection, GaN ohmic gate, threshold voltages shift, power devices.**

I. Introduction

GALLIUM Nitride (GaN) is fast becoming one of the most promising wide bandgap semiconductor material candidates for power switching devices [1]. Due to the high density and mobility of 2-dimensional electron gas (2DEG) [2], GaN devices have low on-state resistance [3]. GaN Polarization Superjunction (PSJ) is a concept reported [4]. It is aimed to achieve charge balance between high-density 2-dimensional hole gas (2DHG) [5] and 2DEG coexisting at the respective interfaces of the GaN (000$\bar{1}$)/AlGaN (000$\bar{1}$)/GaN (0001) double heterostructures to achieve flat electric field distribution during the off-state, thereby maximizing breakdown voltage. Thus, PSJ is an ultra-high performance GaN technology [6–8], which can offer enhanced reliability due to its electric field profile.

Several studies have demonstrated and discussed V_{th} shifts mechanisms in the P-GaN gate HEMTs [9–12]. The main cause of the V_{th} shifts is the charge trapping/detrapping mechanism with typical acceptor trapping levels (Ea) in the GaN HEMTs reported in several studies. Bisi et.al [13] depicted a detailed summary of the catalogued deep levels for a range of activation energies, the list of the reference papers, the type of analyzed samples, and one or more hypothesis on the origin of these traps as reported by various authors at the time of its publication. The spectrum of these defects is rather large and vary depending on many factors, such as growth conditions etc [13]. And they also reported the typical trap levels of Ea from 0.14eV to 0.86eV[13].Moreover, Kuzuhara et.al [14](Ea=0.28eV to 0.64eV), Alberto M Angelotti et.al [15](Ea=0.36eV to 0.68eV) and Gaudenzio Meneghesso et.al[16](Ea=0.099 eV to 0.631eV) reported the very similar range of trap levels value.

This paper reports the V_{th} shift mechanisms in the normally-on 1.2kV P-GaN ohmic gate GaN PSJ HFETs through pulsed-mode measurements. V_{th} shifts caused by the charge trapping mechanisms under positive and negative gate stress voltages are discussed separately. Recovery processes are also presented with varying measuring times. Moreover, the current collapse

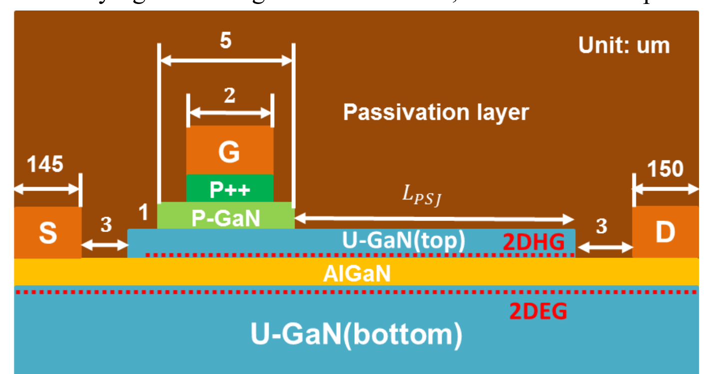

Figure 1. The Cross-section schematics of P-GaN ohmic gate PSJ HFETs.

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in PSJ HFETs is evaluated through the pulsed I_d-V_{ds} characteristics. Finally, the shifts in V_{th} as a function of temperature are also discussed.

II. Devices Structures and Parameters

The devices under test (DUTs) are 1.2 kV ohmic gate PSJ HFETs on Sapphire. The P-GaN ohmic gate is designed for charging/discharging 2DHG during the off-state/switching as well as depleting 2DEG under strong negative bias. Figure 1 shows a simplified cross-section of the GaN PSJ HFETs. The PSJ structures (u-GaN/AlGaN/u-GaN) are capped with the P^+ GaN ohmic gate contact. The doping concentration of Magnesium (Mg) is 1e20 cm^{-3} and 1e19 cm^{-3} in the P^+ GaN and P-GaN layers with their thicknesses of 43nm and 30nm, respectively. P+ GaN and P-GaN layers are only used under gate contacts. As shown in Figure 1, 2DEG and 2DHG are formed at the interface of the AlGaN/GaN and GaN/AlGaN, respectively. The thickness of the top and bottom u-GaN layers are 20nm and 800nm, respectively. The AlGaN thickness is 25nm with the Al mole fraction of 0.3. The cross-sectional dimensions are shown in Figure 1.

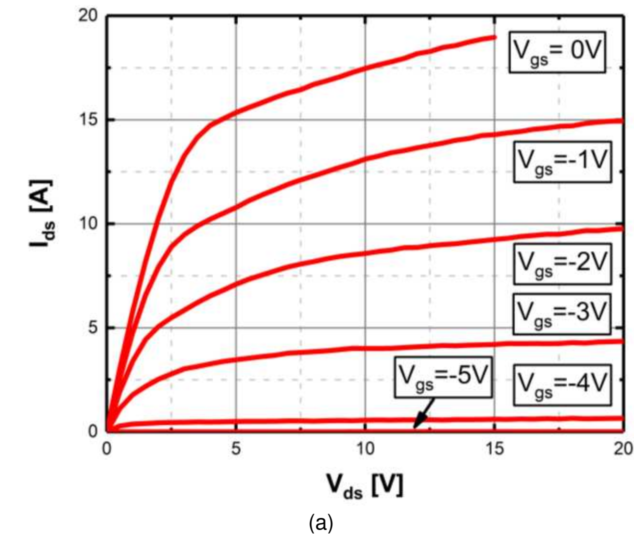
III. Results and Discussions

A. Basic breakdown and I_{ds}-V_{ds} characteristics of 1.2kV PSJ HFETs

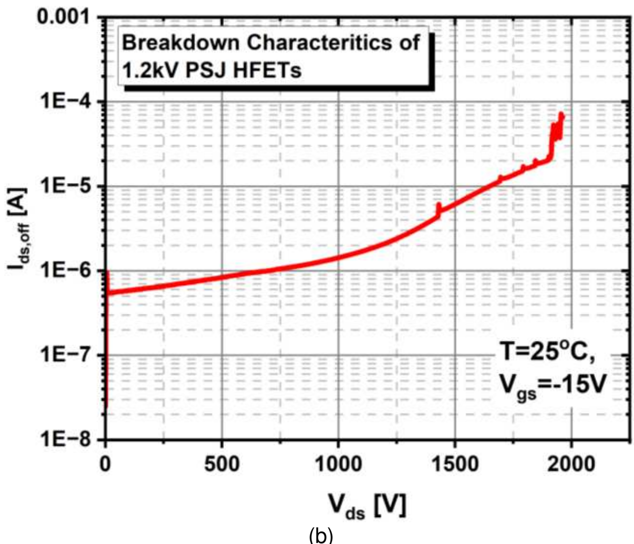
The basic I_{ds}-V_{ds} and breakdown characteristics of 1.2kV PSJ HFETs are presented in Figure 2(a) and (b), respectively. For the purpose of this study, we utilized the small devices with the similar dimensions (except in cases with different lengths of PSJ) to investigate V_{th} shift. The gate widths of them are 1mm.

B. Pulse-mode measurement setup and conditions

Pulse-mode I_d-V_{ds} and transfer measurements are carried out using the Keysight B1500A device curve tracer at room temperature and under dark conditions. In a typical pulsed transfer measurement, during the stressing period, a constant voltage is applied on the gate. During the measuring period, pulsed gate voltages of increasing magnitude (V_{gs}) are applied in sequence at the gate and the I_{ds}-V_{gs} curves are extracted during the measuring period. Under these conditions, applied drain voltages are pulsed voltages of fixed magnitude (V_{ds}). Typical test waveforms are shown in Figure 3(a). The pulse width is set at 0.5ms (limited by the equipment), the duty cycle

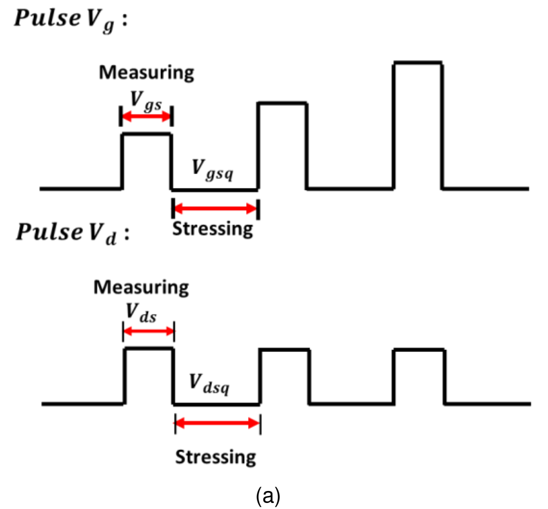


(a)

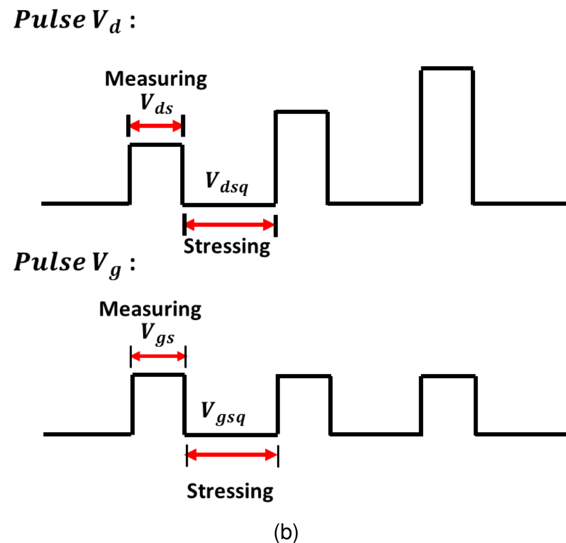


(b)

Figure 2. Typical (a) Ids-Vds and (b) breakdown characteristics of the 1.2kV PSJ HFETs



(a)



(b)

Figure 3.The measurement conditions and setup for (a) pulsed-transfer measurements; and (b) pulsed Ids-Vds characteristics for analyzing the Vth shifts in PSJ HFETs.

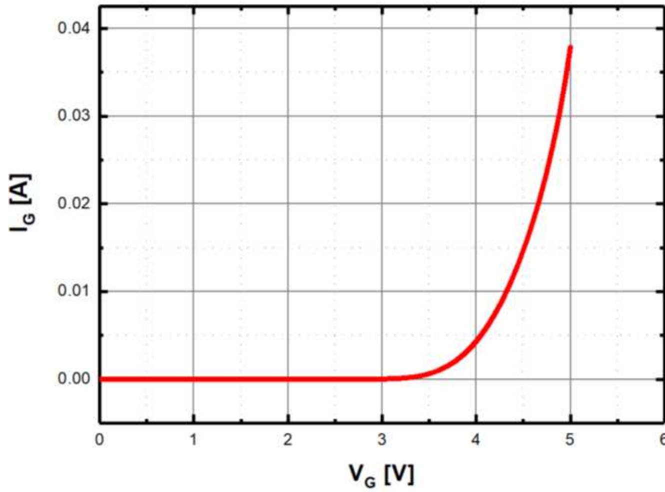
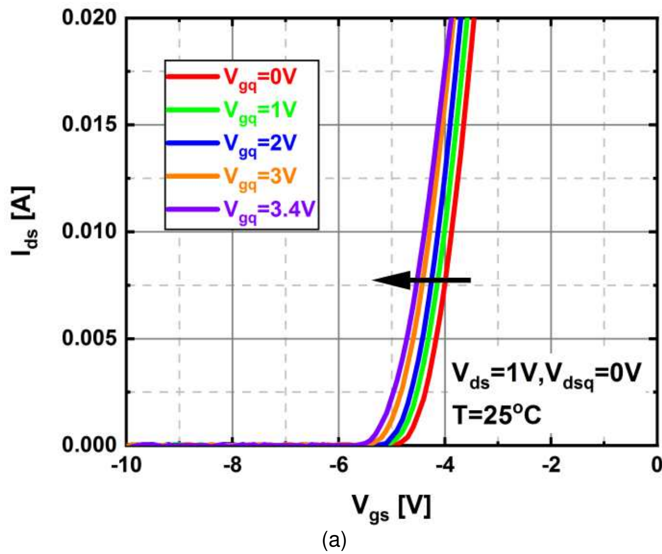
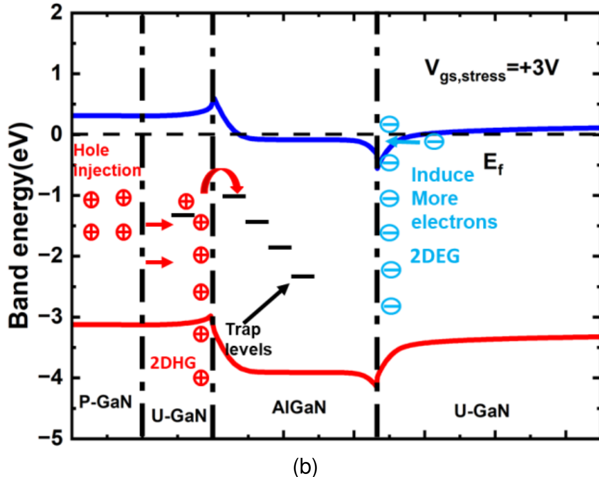


Figure 4.Typical Gate Current characteristics (Ig-Vg) of the PSJ HFETs.

is 0.1%, and the quiescent drain voltages (V_{dsq}) is held at 0V and V_{ds} is 1V, which minimizes the self-heating effects. The quiescent gate voltage (V_{gsq}) which is also defined as the stress voltage is varied. The pulsed transfer measurement setup and conditions are shown in Figure 3 (a).



(a)



(b)

Figure 5. (a)Typical pulsed transfer characteristics of PSJ HFETs measured at Vds=1V and quiescent Vdb=0V, under different stress gate bias Vgsq, ranging from 0V to 3.4V.(b) the trapping mechanisms under positive gate stress

C. V_{th} shift under positive gate stress voltages

Due to the nature of the field shaping and charge balance, PSJ HFETs with L_{PSJ} equal to 15um can achieve breakdown voltage over 1200V[6], [17]. For the purpose of this study, we utilized the small devices with the similar dimensions (except in cases with different lengths of PSJ) to investigate V_{th} shift. The gate leakage current is a typically observed reverse PiN junction current when the gate is negatively biased. Conversely, when the gate is positively biased, the current increases due to hole injection when the bias is higher than 3.4V, as shown in Figure 4.

We considered PSJ HFET with L_{PSJ}=15um and the measured V_{th} is -5V when no gate stress is applied. As shown in Figure 5(a), negative V_{th} shifts in the PSJ HFETs can be observed under positive stress gate voltages from 0V to +3.4V. The trapping mechanisms in the energy band diagram under the positive gate stress are illustrated in Figure 5(b). Holes are injected from the gate and P+GaN layer, some of the holes are captured by the traps located in the top u-GaN layer or accumulated at the heterointerface of U-GaN/AlGaN due to the low mobility of 2DHG. Some of these could potentially move across the GaN/AlGaN band barrier and enter into the AlGaN layer and can be trapped by the hole traps. Therefore, more electrons are induced for char neutrality, causing a rise in 2DEG. When the positive gate stress voltage is removed, the induced electrons are not reduced immediately, thus causing a negative Vth shift, in a manner similar to those from normally-off P-GaN gate AlGaN/GaN HEMTs [9–12].

The relationship between the V_{th} shift value(ΔV_{th}) and different L_{PSJ} (from 15um to 70um) is presented in Figure 6. The Vth shift mechanisms of them under positive gate stress is identical to the Lpsj=15um.Despite the fact that 2DHG exists at most of the drift regions, the heterointerface of top u-GaN/AlGaN along with the L_{PSJ}, the injected holes are mainly concentrated under the gate region and involved in the Vth shift, which is possibly due to the low mobility of 2DHG (lower than16 cm V^2/s)[18].

The recovery process is observed through varied measuring period time presented in Figure 7. In these tests, the stressing time is fixed at 500ms, which is adequate to ensure that the

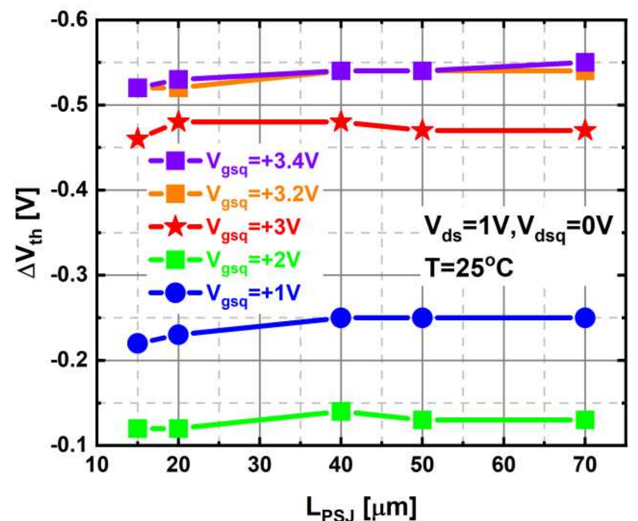


Figure 6. Vth shift value (ΔVth) with different LPSJ (=15um,20um,40um,50um and 70um).

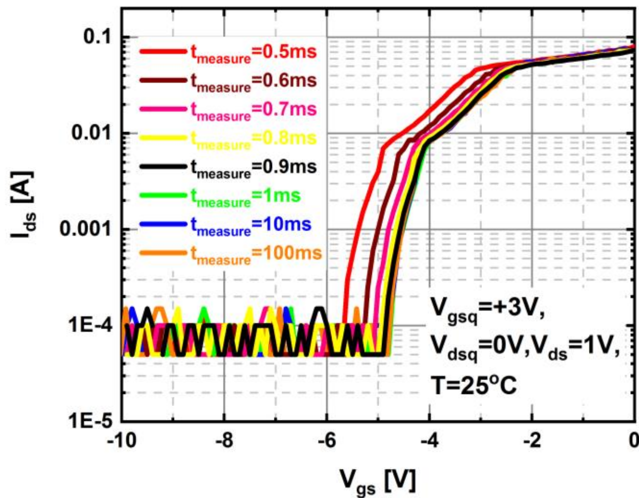


Figure 7. Typical pulsed transfer characteristics of PSJ HFETs were measured at Vds=1V and quiescent Vdb=0V. The measuring time ranges from 0.5ms to 100ms, and the stressing time is fixed at 500ms under gate stress voltages Vgsq =+3 V.

holes are completely trapped. It can be observed that, with the increase of the measuring times, the positive V_{th} shifts gradually saturate over time. The mechanisms during the recovery process can be explained as follows: the holes are injected and trapped in the AlGaN layer under the positive stress voltages during the stressing period. However, during the measuring period, the gate voltages transit from positive biases (the stressing period) to negative biases (the measuring period). Thus, the trapped and accumulated holes are de-trapped because of the applied reverse bias. Therefore, with the increase in measuring time, more holes are released from the AlGaN layer, inducing the decrease in the density of 2DEG. The positive V_{th} shifts gradually saturate because the trapped holes are fully de-trapped during the relatively long recovery period. Typical pulsed I_d-V_{ds} characteristics measured under different positive gate stress voltages to evaluate the current collapse, due to the V_{th} shift are as shown in Figure 8. In these tests, during the stressing period, gate stress voltages of varying magnitudes (V_{gsq}) are applied on the gate and the applied drain voltage V_{dsq} is zero. During the measuring period, the V_{gs} is fixed at a steady value, and pulsed drain voltages of increasing magnitude (V_{gs}) is applied on the drain and I_d-V_{ds} is extracted during the measuring period. The detailed measurement

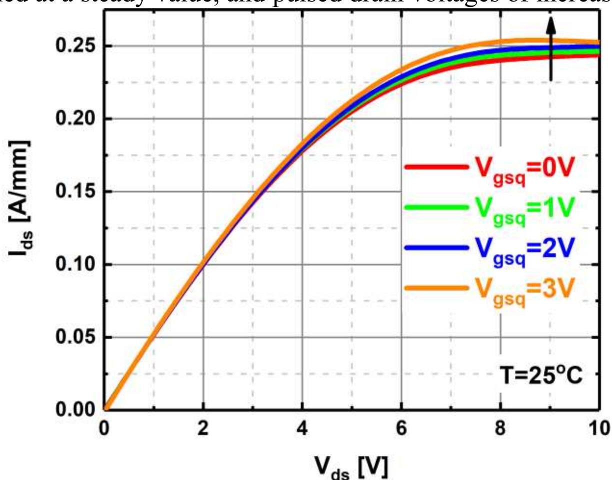
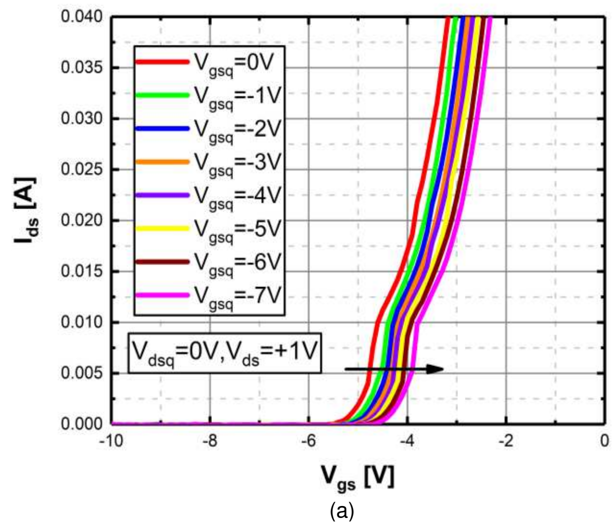
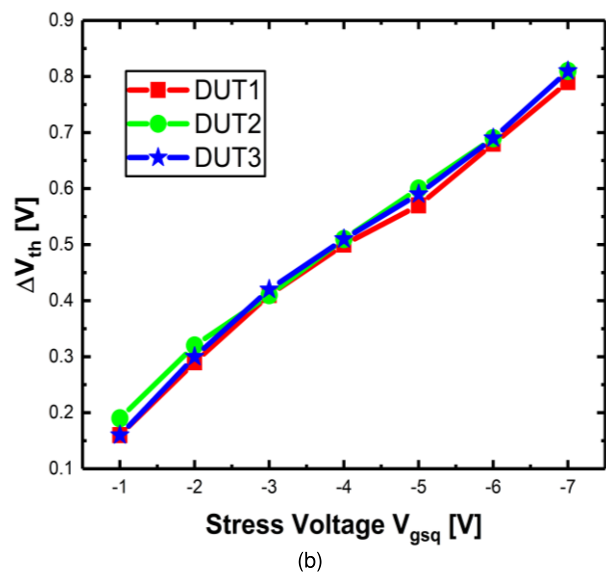


Figure 8. Typical pulsed Id-Vds characteristics of PSJ HFETs were measured at Vgs=3V with different stress gate voltages (Vgsq), ranging from 0V to 3V.



(a)



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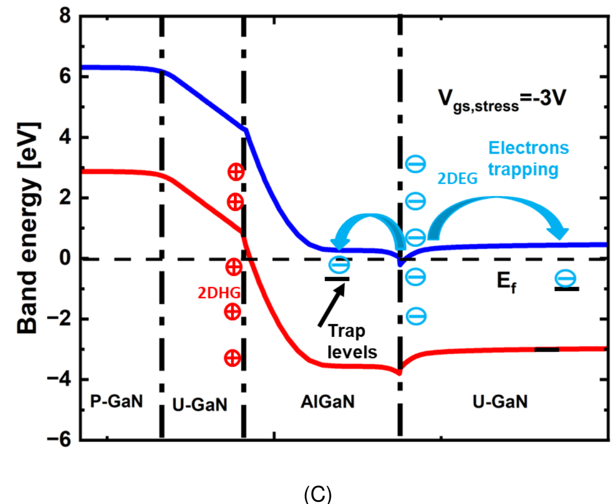

(C)

Figure 9. (a) Typical pulsed transfer characteristics of PSJ HFETs measured at Vds=1V and quiescent Vdb=0V, under different negative stress gate bias Vgb, ranging from 0V to -7V. (b) the Vth shifts as a function of varying gate stress voltages in PSJ HFETs;(C)The trapping mechanisms under negative gate stress.

conditions are shown in Figure 3(b): The V_{gs} maintains at 3V and the stress gate voltages (V_{gsq}) range from 0V to 3V. The quiescent drain voltages (V_{dsq}) are 0V.

The positive gate stress voltages have not induced any significant differences in the on-state resistances in the linear region. Under the low drain voltage, the trapping is difficult to occur laterally from gate to drain. However, under the positive gate stress, it is more possible to happen under the gate, causing holes injection, trapping effects and the negative V_{th} shifts. This is why no variation of on-state resistance, but a marginal increase on the saturation I_d is observed. This interpretation on this phenomenon is also reported in [9]. The Id variation at the saturation region is around 0.065A/mm in [9], but it is only 0.02A/mm of PSJ HFETs (both of them are measured at V_{ds}=6V and V_{gsq}=+3V) presented in Figure 8. Compared to the results of the P-GaN gate HEMTs in [9], PSJ HFETs show similar results but with much lower magnitudes. The marginal I_d increase is negligible in the PSJ HFETs, which is consistent with the results reported in [6], which show minimum current collapse.

D. V_{th} shift under negative gate stress voltages

V_{th} shifts are also analyzed under the same conditions on these devices but with negative gate stress voltages. In these tests, the negative gate stress voltages range from 0V to -7V and the step is -1V. Other measurements conditions are identical to the previous tests.

Pulsed transfer characteristics under different negative gate stress voltages are shown in Figure 9 (a). The positive V_{th} shifts with the increase in negative gate stress voltages (from -7V to 0V) show a reverse trend to the positive gate stress voltages test. The trapping mechanisms under the negative gate stress are illustrated in Figure 9(c). Similarly, the electron trapping process is also illustrated in the band diagram at Vgs,stress=-3V. Under the negative gate stress, some of the electrons are trapped by the GaN buffer traps. And some of electrons can potentially cross the AlGaN/GaN barrier and captured by the electron traps in the AlGaN layer. The electron trapping causes the reduction of the 2DEG, resulting in the positive Vth shift when the gate stress voltage is removed. The magnitude of the V_{th} shift value shows a linear relationship with the magnitude of the negatively increasing stress voltages as shown in Figure 9 (b).

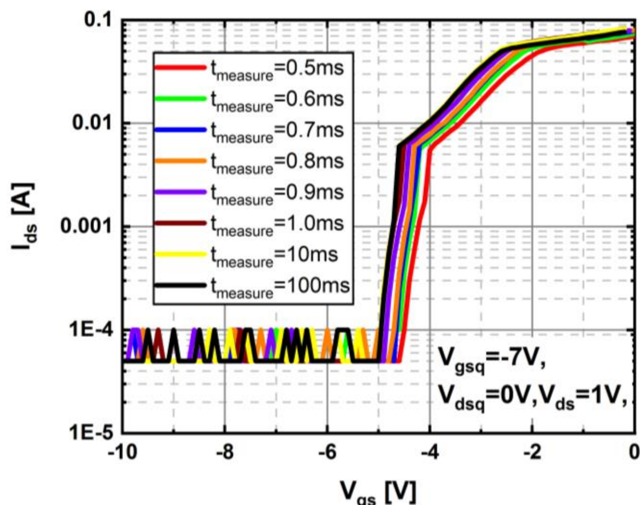

Figure 10. Typical pulsed transfer characteristics of PSJ HFETs measured at V_{ds}=1V and quiescent V_{dsq}=0V. The measuring time ranges from 0.5ms to 100ms, and the stressing time is fixed at 500ms under gate stress voltages V_{gsq}=-7V.

The recovery processes at the off-state (V_{gsq} below -5V) during the stress period, are presented in Figure 10.The measurement conditions are identical to the previous test shown in Figure 7, but with different gate stress voltages. As can be seen from Figure 10, negative V_{th} shifts gradually saturate when the measuring times increase from 0.5ms to 100ms at V_{gsq}= -7V. It can be explained as follows: During the negative stress period, electrons are captured by the traps in AlGaN or buffer layer. During the measurement, the gate voltages are less negative than V_{gsq}. Therefore, the electrons are de-trapped from the trap-states in the AlGaN or bottom u-GaN buffer layer. With the increase in the measuring time, more electrons are de-trapped from the AlGaN or buffer layer, causing an increase in electrons in the 2DEG channel and accompanying the negative V_{th} shift. With the measuring time increasing further, all the trapped electrons saturate, and as do the V_{th} shifts.

Similarly, pulsed I_d-V_{ds} characteristics are measured under negative gate stress voltages ranging from 0V to -4V shown in Figure 11. V_{dsq} is kept at 0V. The measurement conditions are shown in Figure 3(b). Like the positive gate stress tests, the negative stress gate voltages do not cause any variation in the on-state resistance in the linear region. Due to the current collapse, the I_d shows a slight downward trend in the saturation region with the negatively increasing gate stress voltages. And these marginal variations also confirm the current collapse is negligible in PSJ HFETs.

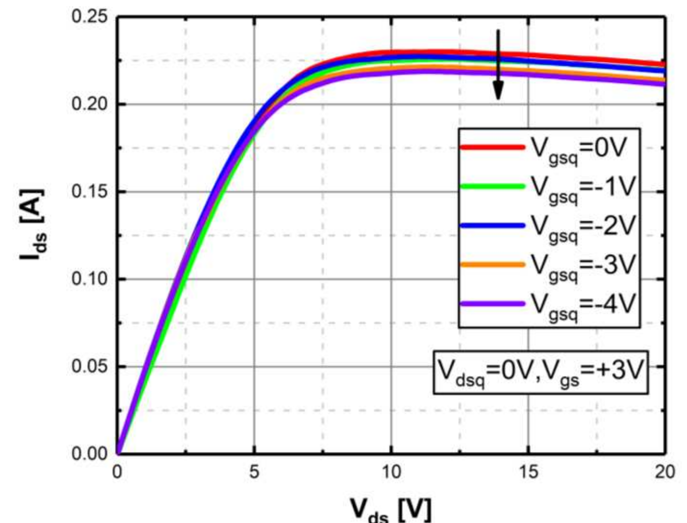

Figure 11. Typical pulsed Id-Vds characteristics of PSJ HFETs were measured at Vgs=3V with different stress gate voltages (Vgsq), ranging from 0V to -4V.

E. V_{th} shifts under positive stress voltages as a function of temperature

Pulsed transfer characteristics are measured under different temperatures, ranging from 20ºC to 150ºC. The gate stress voltages are set at 3V, and the steady V_{ds} is 1V (V_{dsq} is 0V). The V_{th} shifts values are extracted from each measurement of three

identical devices under different temperatures at a current density of 10mA/mm, as shown in Figure 12.

Initially, it can be observed that the magnitude of $|\Delta V_{th}|$ increases from 20ºC to 100ºC. However, with a further increase in temperature, $|\Delta V_{th}|$ gradually saturates [11,12]. These V_{th} shifts mechanisms in PSJ GaN HFETs can be explained as follows: at the start, an increase in temperature from 20ºC to 100ºC results in more holes being generated because of the rise in the activation of Mg. Thus, more holes are trapped and accumulated in the AlGaN layer, causing the negative V_{th} shifts at 100ºC. However, with the temperature increasing further, although the density of the holes increases, the recovery behaviour becomes more dominant, which compromises the further increase of V_{th} shift value.

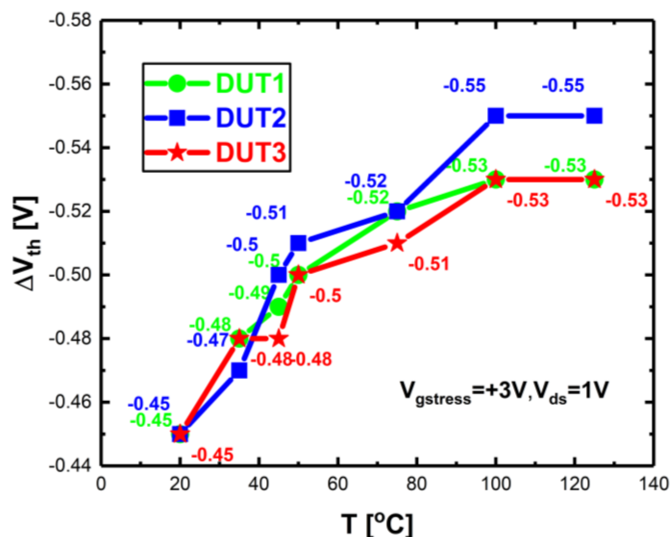

Figure 12. the Vth shifts as a function of different temperatures in PSJ HFETs, the gate stress voltages is +3V, and the steady Vds is 1V (Vdsq is 0V). The Vth is extracted at 1mA/mm.

Additionally, another thermal mechanism about the 2DEG that can be responsible for this trend is mentioned in [11]: more 2DEG electrons are thermally activated from the channel states into the AlGaN layer with the temperature rise. This mechanism causes the positive V_{th} shifts, compensating the negative V_{th} shifts caused by hole trapping and accumulation processes. Therefore, the $|\Delta V_{th}|$ saturates when temperature increases above 100ºC.

IV. Conclusions

V_{th} shift mechanisms in normally-on GaN PSJ HFETs through pulsed I_d-V_{ds} and transfer characteristics measurements under the positive and negative gate stress voltages are reported for the first time. Under positive gate stress voltage conditions, more holes are injected into the AlGaN layer or u-GaN/AlGaN hetero-interface and then get trapped and accumulated by the hole trap states. Thus, the trapped or accumulated holes cannot escape immediately when the reversed negative gate voltages are applied during the measuring period, inducing more electrons in the 2DEG channel, and causing negative V_{th} shifts. Despite the presence of the 2DHG extended beyond the gate, the injection of holes is restricted to the gate contact regions. When the negative gate stress voltages are applied, electrons are trapped by the electron trap states in the AlGaN layer or GaN buffer layer, causing the positive V_{th} shifts. The V_{th} shifts are also presented during the recovery processes by varying the measuring times. With the increase in the measuring times, more trapped electrons and holes will be released, causing the V_{th} shifts. Moreover, from the pulsed I_d-V_{ds} characteristics, positive and negative gate stress voltages cause a much lower magnitude of the differences on the saturation current than P-GaN gate HEMTs, indicating that current collapse is significantly reduced in PSJ HFETs.

Furthermore, the temperature effects on the V_{th} shifts under the positive gate stress voltages are also discussed. $|\Delta V_{th}|$ increases when the temperature rises from 20ºC to 100ºC. Thermally-activated holes and 2DEG electrons cause this phenomenon. As the temperature increases, more holes are trapped and accumulated in the AlGaN layer, causing the negative V_{th} shifts. However, the strengthened recovery processes cause the positive V_{th} shifts, which compensates for the negative V_{th} shifts caused by the enhanced holes injection and accumulation processes, which induces the saturation of the $|\Delta V_{th}|$.

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