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High-Efficiency WPT System for CC/CV Charging Based on Double-half-bridge Inverter Topology with Variable Inductors

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***Abstract*—Efficiency remains a key challenge in wireless charging in academia and industry. In this paper, a new wireless power transfer (WPT) system based on a double-half-bridge (DHB) inverter with two variable inductors (VIs) is proposed. Compared with conventional full-bridge (FB) inverters, the DHB inverter can reduce the current through the MOSFETs under the same output power and thus, reduce the conduction loss. Next, by adjusting the inductances of the VIs instead of using phase shift (PS) method, the output voltage or current can be controlled, while the circulating current can be eliminated and wide-range zero voltage switching (ZVS) operation can be achieved. Consequently, the power loss can be further reduced. Circuit analysis, VI design as well as hardware implementation are provided in detail. A laboratory prototype is built to verify the feasibility of the proposed method. Close agreement is obtained between simulation and experimental results. The maximum efficiency can reach 92.4%, which is 3.65% higher than traditional PS control.**

***Index Terms*—Wireless power transfer (WPT), double-half-bridge (DHB) inverter, variable inductor (VI), zero voltage switching (ZVS), output voltage or current.**

I. Introduction

WIRELESS power transfer (WPT) is an emerging technology that can deliver power without physical contact, which brings significant merits such as safety, convenience, etc. Up to now, this technology has been successfully used in some practical applications such as medical implantable devices [1], [2], consumer electronics [3], [4], and electric vehicles (EVs) [5], [6].

A. Current Problem

Despite many advantages of WPT technologies over traditional wired charging, there are still two critical problems that need to be solved before they can be widely deployed. First, a WPT system needs to provide stable output subject to parameter variations. Taking EV charging as an example, two operation modes, constant current (CC) charging and constant voltage (CV) charging, are preferred to improve life cycles and safety. However, the equivalent resistance of a battery varies in a nonlinear manner during charging. As a result, it is challenging for WPT systems to provide constant and load-independent output voltages/currents. Another requirement is high efficiency, which has been widely recognized as an important objective to design a WPT system. Particularly, the conduction loss and switching loss from high-frequency (HF) switching devices are attributed significantly to low efficiency of a WPT system [7]. In this sense, the reduction of these two power losses is necessary for HF switching devices, which is the key factor affecting the efficiency of the system.

B. Literature Review

To address the above two major problems, recently, many methods based on parameter adjustment on the primary side (transmitter) have been proposed to achieve stable outputs, which have the benefits of reducing volume and complexity on the secondary side (receiver).

For instance, in [8], an additional DC-DC converter is added between the DC power supply and the inverter to maintain a desired output by adjusting the duty cycle of the HF switching device. However, additional power loss and cost due to the DC-DC converter limit its feasibility in practice. In addition to the use of DC-DC converters, direct regulation of the driving signal of the full-bridge (FB) inverters seems to be an effective approach. By using pulse frequency modulation (PFM) methods, desired outputs can be obtained with the switching frequency as the control objective[9], [10]. Unfortunately, multiple frequencies that meet the requirements can lead to bifurcation phenomenon, degrading system performance and reliability. Thus, it is preferable for a system to operate at a fixed switching frequency. In phase-shift (PS) control [11], [12], by only adjusting the phase difference of the driving signals, a stable output can be obtained without changing the switching frequency. Nevertheless, the difference between zero crossing point (ZCP) of the inverter output voltage and current makes zero voltage switching (ZVS) operation difficult to achieve, especially under light-load conditions.

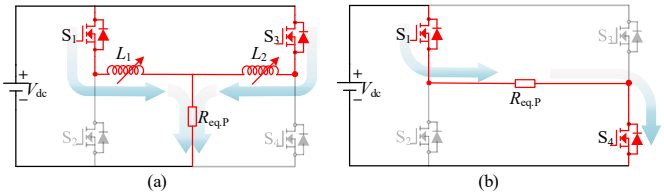

Fig. 1. The current paths of two inverters during half a period. (a) DHB inverter. (b) FB inverter.

The above methods are all based on FB inverters. However, double-half-bridge (DHB) inverters still lack sufficient research attention. Actually, thanks to the advantage of current distribution through MOSFETs shown in Fig. 1, DHB inverters can effectively improve efficiency and reliability, which shows promising potentials in WPT systems. [13] proposed to use DHB topology instead of FB topology to achieve induction heating (IH), and soft switching and current equalization operation are realized because of the series of two identical inductors. However, power regulation is addressed by adjusting the phase difference between two half bridges. As a result, one of them will inevitably change the working state from power supply to power consumption with the increase of the phase shift. This leads to circulating loss, thus dramatically restricting the application of DHB inverters in WPT.

C. Motivations and Contributions

Inspired by the merit of circulating current elimination, we propose to incorporate DHB inverters into WPT systems. Building on our previous efforts in extending ZVS range by using auxiliary variable inductors (VIs) [7], a control method based on two VIs instead of two fixed inductors on the output side of DHB inverters is developed for CC/CV charging. Specifically, the VIs are exploited as system's control degree of freedom to realize CC or CV, so as to avoid the PS control and circulating loss.

The main contribuitons of this paper are highlighted as follows.

(1) The DHB topology is used to reduce conducting loss due to the distribution of current in the primary side. Moreover, by designing two identical VIs in series at the inverter's output, the current distribution ratio can be optimized to minimize the conducting loss without affecting the system's output . Compared with PS control, the proposed method will not generate circulating current. Furthermore, a wide-range ZVS operation can be achieved due to the series of VIs even under light-load conditions.

(2) A cost-effective combination control method is utilized for VIs. Only one DC current source is used to adjust the inductance due to the same parameters and variation curve, thus reducing the loss and cost of VIs.

The proposed method takes the reduction of conducting loss, switching loss and elimination of circulating loss into consideration, which could dramatically improve the system's efficiency. These features have been verified by experimental results.

II. Proposed DHB Inverter Topology with Variable Inductors

In this paper, the SS compensation topology is adopted for analysis due to the independence of resonance on the primary side to the variation of load when the secondary side is resonant.

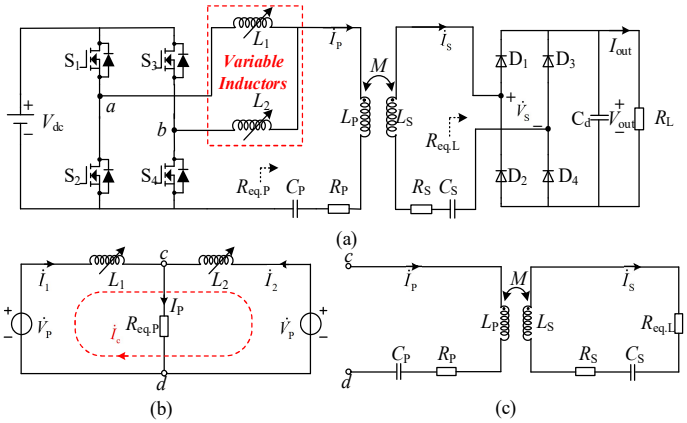

Fig. 2. Proposed circuit scheme of double-half-bridge inverter with two VIs. (a) the whole WPT system. (b) AC equivalent circuit of primary side. (c) AC equivalent circuit of secondary side.

The circuitry of the proposed WPT system is shown in Fig. 2 (a) with two additional VIs (L_1 and L_2) configured on the primary side. A DHB inverter is used to convert the direct current (DC) source V_{dc} to a high-frequency alternating current (AC) source to feed the primary coil, and the rectifier is employed on the secondary side to convert the induced AC power to DC power to supply the load R_L. L_P and L_S are the self-inductances of the primary and the secondary coils, respectively. C_P and C_S are the series resonant capacitors connected to the coils. M is the mutual inductance between the primary and the secondary coils. R_P is the equivalent series resistance (ESR) of the primary coil and variable inductors, and R_S is the ESR of the secondary coil. $R_{eq.L}$ is the equivalent resistance of the rectifier. $R_{eq.P}$ is the equivalent resistance of the transmitter. It is emphasized that the two half-bridge inverters are in parallel with identical control signal and hence, they are independent of each other.

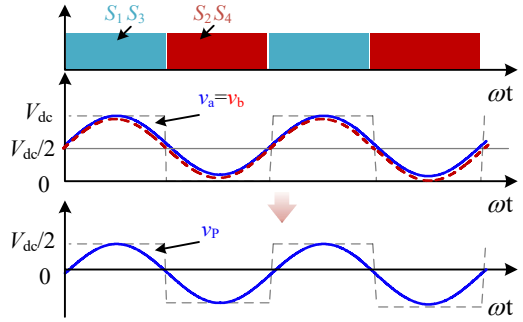

Fig. 3. Operation waveforms of the switching S_1-S_4 and output voltage of inverter.

In this paper, the inverter operates at a constant operating frequency, a fixed duty cycle, and a zero phase-shift angle, as shown in Fig. 3. As a result, a symmetrical square voltage output is generated. By using the fundamental harmonic approximation (FHA) method, the fundamental components of square wave v_a and v_b are plotted in Fig. 3. They are sine waves with an amplitude of $V_{dc}/2$ and a positive DC offset of $V_{dc}/2$. Due to the principle of electromagnetic induction, the DC component cannot produce an induced current on the secondary side. Thus, for the whole system load, the output voltage of a single half-bridge inverter can be equivalent to v_P, as shown in Fig. 3.

According to FHA, one can obtain

$$\dot{V}_P = V_P\angle 0^\circ = \frac{\sqrt{2}V_{dc}}{\pi}\angle 0^\circ \tag{1}$$

where V_P is the Root-Mean-Square (RMS) value of the voltage v_P.

For a diode rectifier, its equivalent resistance on the secondary side can be expressed as [5]

$$\begin{cases} V_S = \dfrac{2\sqrt{2}}{\pi}V_{out} \\ I_S = \dfrac{\pi}{2\sqrt{2}}I_{out} \\ R_{eq.L} = \dfrac{8R_L}{\pi^2} \end{cases} \tag{2}$$

where V_S, I_S, are the RMS value of rectifier input voltage and current. V_{out}, I_{out} are the output voltage and current of the rectifier, respectively.

To simplify the analysis, the AC equivalent circuit can be classified into two parts, as illustrated in Fig. 2 (b) and (c). According to Fig. 2 (b), by applying the Kirchhoff's Voltage Law (KVL), the following equation can be obtained

$$\begin{cases} \mathrm{j}\omega L_1 \dot{I}_1 = \mathrm{j}\omega L_2 \dot{I}_2 \\ \left(\dot{I}_1 + \dot{I}_2\right) R_{\mathrm{eq.P}} + \mathrm{j}\omega L_2 \dot{I}_2 = \dot{V}_{\mathrm{P}} \end{cases} \tag{3}$$

where $\dot{I}_1$, $\dot{I}_2$ are the output current of the half-bridge inverters respectively; $\omega = 2\pi f$ represents the system operating angular frequency; f is the system operating frequency.

By denoting $\lambda = L_1 / L_2$, $\dot{I}_1$, $\dot{I}_2$, $\dot{I}_{\mathrm{P}}$ can be solved as

$$\begin{cases} \dot{I}_1 = \dfrac{\dot{V}_{\mathrm{P}}}{R_{\mathrm{eq.P}}\left(1+\lambda\right) + \mathrm{j}\omega L_1} \\ \dot{I}_2 = \dfrac{\lambda \dot{V}_{\mathrm{P}}}{R_{\mathrm{eq.P}}\left(1+\lambda\right) + \mathrm{j}\omega L_1} \\ \dot{I}_{\mathrm{P}} = \dot{I}_1 + \dot{I}_2 = \dfrac{\left(1+\lambda\right)\dot{V}_{\mathrm{P}}}{R_{\mathrm{eq.P}}\left(1+\lambda\right) + \mathrm{j}\omega L_1} \end{cases} \tag{4}$$

where $\dot{I}_{\mathrm{P}}$ is the current through the primary coil.

Accordingly, the phasors of $\dot{I}_1$ and $\dot{I}_2$ can be expressed as

$$\begin{cases} \dot{I}_1 = \dfrac{V_{\mathrm{P}}}{\sqrt{\left[R_{\mathrm{eq.P}}\left(1+\lambda\right)\right]^2 + \left(\omega L_1\right)^2}} \angle \left[-\arctan\left(\dfrac{\omega L_1}{R_{\mathrm{eq.P}}\left(1+\lambda\right)} \right) \right] \\ \dot{I}_2 = \dfrac{\lambda V_{\mathrm{P}}}{\sqrt{\left[R_{\mathrm{eq.P}}\left(1+\lambda\right)\right]^2 + \left(\omega L_1\right)^2}} \angle \left[-\arctan\left(\dfrac{\omega L_1}{R_{\mathrm{eq.P}}\left(1+\lambda\right)} \right) \right] \end{cases} \tag{5}$$

According to (5), it is indicated that $\dot{I}_1$ and $\dot{I}_2$ have identical phases but different amplitudes. As a result, the circulating current $\dot{I}_{\mathrm{c}}$ between the DHB inverter shown in Fig. 2 (b) will not be generated. Moreover, $\dot{I}_{\mathrm{c}}$ can also be obtained by [13]

$$\dot{I}_{\mathrm{c}} = \frac{\dot{V}_{\mathrm{P}} - \dot{V}_{\mathrm{P}}}{\mathrm{j}\omega\left(L_1 + L_2\right)} = 0 \tag{6}$$

Obviously, the circulating current is equivalent to zero without using phase-shift control for the inverter.

From Fig. 2 (c), since C_{P} and C_{S} are used to compensate the primary coil and the secondary coil, they can be obtained by

$$\begin{cases} C_{\mathrm{P}} = \left(\omega^2 L_{\mathrm{P}}\right)^{-1} \\ C_{\mathrm{S}} = \left(\omega^2 L_{\mathrm{S}}\right)^{-1} \end{cases} \tag{7}$$

By using KVL, the following relationships can be obtained

$$\begin{cases} R_{\mathrm{eq.P}} = R_{\mathrm{P}} + \dfrac{\left(\omega M\right)^2}{R_{\mathrm{eq.L}} + R_{\mathrm{S}}} \\ \mathrm{j}\omega M \dot{I}_{\mathrm{P}} = \left(R_{\mathrm{S}} + R_{\mathrm{eq.L}}\right) \dot{I}_{\mathrm{S}} \end{cases} \tag{8}$$

Substituting (4) into (8), the secondary coil current $\dot{I}_{\mathrm{S}}$ can be expressed as

$$\dot{I}_{\mathrm{S}} = \frac{\left(1+\lambda\right)\dot{V}_{\mathrm{P}}}{R_{\mathrm{eq.P}}\left(1+\lambda\right) + \mathrm{j}\omega L_1} \cdot \frac{\mathrm{j}\omega M}{R_{\mathrm{eq.L}} + R_{\mathrm{S}}} \tag{9}$$

In the proposed topology, primary current distribution has been achieved due to the DHB inverter. From [7], the conduction loss of inverter can be calculated as

$$P_{\mathrm{Cond}} = \left(I_1^2 + I_2^2\right) r_{\mathrm{m}} \tag{10}$$

where P_{Cond} represents the MOSFETs' conducting loss; r_{m} is the drain-source on-state resistance.

Therefore, to minimize the conducting loss of MOSFETs, the optimal current relationship should be the average distribution, i.e.

$$\dot{I}_1 = \dot{I}_2 \tag{11}$$

Accordingly, substituting (4) into (11), one can simply obtain

$$\lambda = 1 \tag{12}$$

(12) suggests the optimization design is to manufacture two VIs with the same parameters to have the identical variation curve of inductance. Furthermore, the output currents of the half-bridge inverters $\dot{I}_1$, $\dot{I}_2$ and the coil current $\dot{I}_{\mathrm{P}}$, $\dot{I}_{\mathrm{S}}$ can be simplified as

$$\begin{cases} \dot{I}_1 = \dot{I}_2 = \dfrac{\dot{V}_{\mathrm{P}}}{2R_{\mathrm{eq.P}} + \mathrm{j}\omega L_1} \\ \dot{I}_{\mathrm{P}} = \dfrac{2\dot{V}_{\mathrm{P}}}{2R_{\mathrm{eq.P}} + \mathrm{j}\omega L_1} \\ \dot{I}_{\mathrm{S}} = \dfrac{2\dot{V}_{\mathrm{P}}}{2R_{\mathrm{eq.P}} + \mathrm{j}\omega L_1} \cdot \dfrac{\mathrm{j}\omega M}{R_{\mathrm{eq.L}} + R_{\mathrm{S}}} \end{cases} \tag{13}$$

As can be seen from (13), L_1 is the only degree of control freedom for the secondary side current in this system, thus the stable output can be realized by adjusting it.

III. Realization of Battery Charging

In battery charging, generally, two operation modes, i.e., CC mode and CV mode, are preferred in order to increase the life cycle and safety. In this paper, a sealed Lead-Acid battery is used as the load to emulate EV charging. TABLE I shows the battery parameters and charging requirements obtained from the datasheet in [14]. In the system, the required current gain G_{I}=0.02 and voltage gain G_{V}=0.48 with the parameters listed in TABLE I.

TABLE I
Key Parameters For Theoretical Analysis

Symbol	Quantity	Value
V_{out}	Charging voltage of battery	72 V
I_{out}	Charging current of battery	3 A
V_{dc}	DC input voltage	150 V
ω	Operating angular frequency	$1.7\pi\times10^5$
$L_{\mathrm{P}}/L_{\mathrm{S}}$	Inductance of $L_{\mathrm{P}}/L_{\mathrm{S}}$	200 μH
$R_{\mathrm{P}}/R_{\mathrm{S}}$	ESR of $L_{\mathrm{P}}/L_{\mathrm{S}}$	0.2 Ω
M	Mutual inductance of coupler	30 μH
R_{L}	Equivalent load resistance of the battery packs	10 Ω-24 Ω (CC) 24 Ω-72 Ω (CV)

1) CC mode: Substituting (1), (2) and (8) into (13), the output current of system can be obtained by

$$I_{\mathrm{out}} = \frac{8}{\pi^2} \frac{\omega M V_{\mathrm{dc}}}{\left(R_{\mathrm{eq.L}} + R_{\mathrm{S}}\right)\sqrt{4\left(R_{\mathrm{P}} + \dfrac{\left(\omega M\right)^2}{R_{\mathrm{eq.L}} + R_{\mathrm{S}}}\right)^2 + \left(\omega L_1\right)^2}} \tag{14}$$

It is obvious that I_{out} can be described as a function of L_1 and $R_{eq.L}$ when the DC voltage V_{dc} and mutual inductance M are constant, that means, the CC charging can be achieved by adjusting the value of L_1. To further analyze the output characteristic of the system, the current gain could be defined as

$$G_I = \frac{I_{out}}{V_{dc}} = \frac{8}{\pi^2} \frac{\omega M}{\left(R_{eq.L}+R_S\right)\sqrt{4\left(R_P+\frac{(\omega M)^2}{R_{eq.L}+R_S}\right)^2+(\omega L_1)^2}} \quad (15)$$

Therefore, with the parameters listed in TABLE I, G_I as a function of L_1 and R_L could be plotted in Fig. 4 according to (2) and (15). For clear and direct illustration, the curve of L_1 varied with R_L at G_I=0.02 is also plotted to demonstrate the feasibility for CC charging.

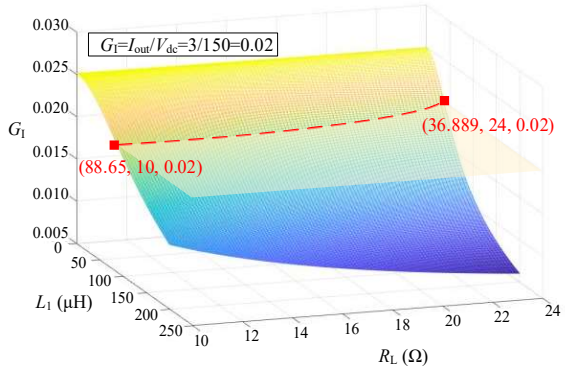

Fig. 4. G_I as a function of L_1 and R_L with its boundary coordinates when G_I=0.02.

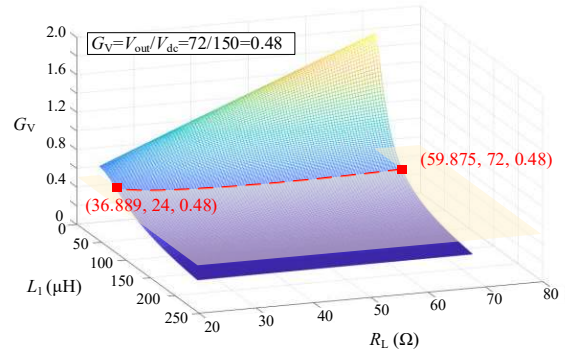

Fig. 5. G_V as a function of L_1 and R_L with its boundary coordinates when G_V=0.48.

2) CV mode: From (14), the output voltage can be calculated as

$$V_{out} = \frac{8}{\pi^2} \frac{\omega M R_L V_{dc}}{\left(R_{eq.L}+R_S\right)\sqrt{4\left(R_P+\frac{(\omega M)^2}{R_{eq.L}+R_S}\right)^2+(\omega L_1)^2}} \quad (16)$$

Accordingly, the voltage gain could be defined as

$$G_V = \frac{V_{out}}{V_{dc}} = \frac{8}{\pi^2} \frac{\omega M R_L}{\left(R_{eq.L}+R_S\right)\sqrt{4\left(R_P+\frac{(\omega M)^2}{R_{eq.L}+R_S}\right)^2+(\omega L_1)^2}} \quad (17)$$

Similarly, G_V as a function of L_1 and R_L is plotted in Fig. 5, and the curve of L_1 varied with R_L is also plotted in Fig. 5 when G_V=0.48 to show the feasibility for CV charging more directly.

IV. Design of Variable Inductors

According to (15) and (17), the desired inductance value of L_1 can be obtained as

$$L_{1-CC} = \frac{1}{\omega}\sqrt{\left(\frac{8}{\pi^2}\frac{\omega M}{\left(R_{eq.L}+R_S\right)G_I}\right)^2-4\left(R_P+\frac{(\omega M)^2}{R_{eq.L}+R_S}\right)^2} \quad (18)$$

$$L_{1-CV} = \frac{1}{\omega}\sqrt{\left(\frac{8}{\pi^2}\frac{\omega M R_L}{\left(R_{eq.L}+R_S\right)G_V}\right)^2-4\left(R_P+\frac{(\omega M)^2}{R_{eq.L}+R_S}\right)^2} \quad (19)$$

From (18) and (19), the whole dimming range of the variable inductor can be calculated and plotted in Fig. 6. As a result, a theoretical operation range is from 36.889 μH to 88.65 μH. Considering the overmeasure of range, the desired dimming range can be designed from 25 μH to 100 μH, i.e., $L_{1\text{-}min}$=25 μH, $L_{1\text{-}max}$=100 μH.

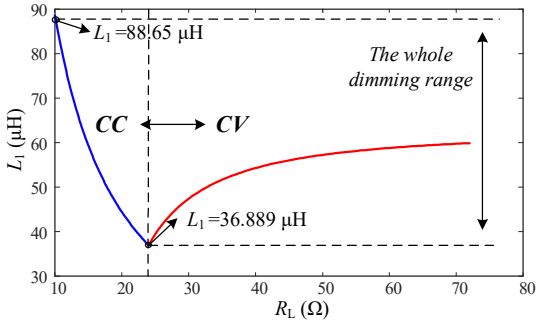

Fig. 6. The required value of VI and its whole dimming range.

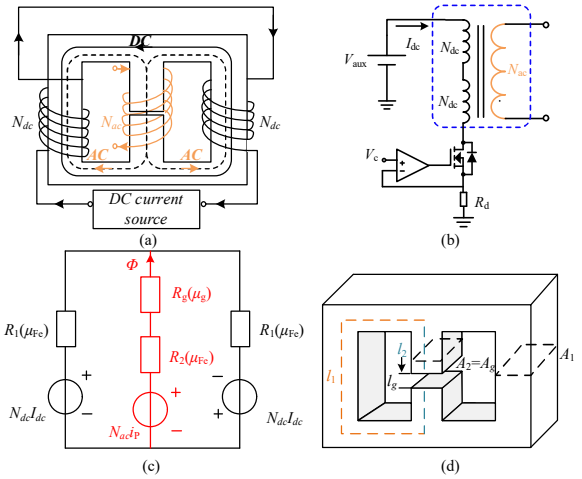

Fig. 7. A current-controlled VI. (a) working mode, (b) implementation of DC current source, (c) equivalent magnetic circuit, (d) structure and size.

A current-controlled VI using two gapped E cores is shown in Fig. 7 (a). The main winding is an AC coil that is connected in series with the system. The auxiliary winding is a DC coil controlled by a DC current source. When VI is in a normal operation, the current in the auxiliary winding is controlled by the DC current source to change the permeability of the magnetic core and thus, the inductance of the main winding will change with respect to the variation of permeability. It is worth emphasizing that the auxiliary winding of two legs should be serially connected in opposite polarity to cancel the induced AC voltage in the auxiliary winding [15]-[17].

The implementation of the DC current source is described in Fig. 7 (b). The DC circuit is supplied by an auxiliary DC voltage

V_{dc}. By adjusting the reference voltage V_c to control the state of MOSFET, a desired DC current I_{dc} can be achieved.

By using N27 [18] material (a ferrite core material), the equivalent reluctance model of the current-controlled VI is shown in Fig. 7 (c). Moreover, the reluctance values can be obtained as [19]

$$R_i(\mu_{Fe}) = \frac{l_i}{\mu_{Fe} A_i}, R_g(\mu_0) = \frac{l_g}{\mu_0 A_g}, (i = 1,2) \tag{20}$$

where l_i, l_g represent the effective length of the magnetic circuit, and A_i, A_g represent the cross-sectional area of the magnetic material shown in Fig. 7 (d); μ_{Fe}, μ_0 denote the permeability of ferrite core and vacuum respectively.

Given a coil with a magnetic material core, its inductance can be determined by [19]

$$L_1 = \frac{\psi}{i_P} = \frac{N_{ac}\phi}{i_P} \tag{21}$$

As can be seen from Fig. 7 (c), the magnetic flow can be calculated by using KVL

$$\phi = \frac{N_{ac} i_P}{\frac{1}{2}R_1(\mu_{Fe}) + R_2(\mu_{Fe}) + R_g(\mu_0)} \tag{22}$$

Substituting (22) into (21), the value of VI can be calculated by

$$L_1 = \frac{N_{ac}^2}{\frac{1}{2}R_1(\mu_{Fe}) + R_2(\mu_{Fe}) + R_g(\mu_0)} \tag{23}$$

1) Design of main winding turns N_{ac}: As the permeability of magnetic material decreases with increasing saturation, the following relationships can be satisfied when the control current I_{dc} is set to zero.

$$\begin{cases} \mu_{Fe} \gg \mu_0 \\ R_g(\mu_0) \gg R_{Fe}(\mu_{Fe}) \end{cases} \tag{24}$$

Therefore, the maximum inductance of VI can be simplified as

$$L_{1-max} = \frac{N_{ac}^2}{R_g(\mu_0)} = \frac{N_{ac}^2 \mu_0 A_g}{l_g} \tag{25}$$

From (25), the main winding turns can be expressed as

$$N_{ac} = \sqrt{\frac{L_{1-max} l_g}{\mu_0 A_g}} \tag{26}$$

2) Design of auxiliary winding turns N_{dc}: Substituting $L_{1\text{-}min}$ and (26) into (23), the minimum permeability $\mu_{Fe\text{-}min}$ satisfies

$$L_{1-min} = \frac{L_{1-max} l_g}{\left[\frac{1}{2}R_1(\mu_{Fe\text{-}min}) + R_2(\mu_{Fe\text{-}min}) + R_g(\mu_0)\right]\mu_0 A_g} \tag{27}$$

Substituting (20) into (27), $\mu_{Fe\text{-}min}$ can be expressed as

$$\mu_{Fe-min} = \frac{L_{1-min}}{L_{1-max} - L_{1-min}}\left[\frac{1}{2A_1} + \frac{1}{A_2}\right]\frac{1}{R_g(\mu_0)} \tag{28}$$

As can be required from [18], since the permeability is an inverse function of the magnetic density, the minimum permeability $\mu_{Fe\text{-}min}$ must correspond to the maximum magnetic density H_{max}. Considering the loss of the DC current source, the maximum control current in this paper is designed as I_{max}=2A. Furthermore, the auxiliary winding turns can be obtained by

$$N_{dc} = \frac{H_{max} l_1}{I_{max}} \tag{29}$$

For better illustration, the proposed optimization procedure of winding turns is depicted in Fig. 8.

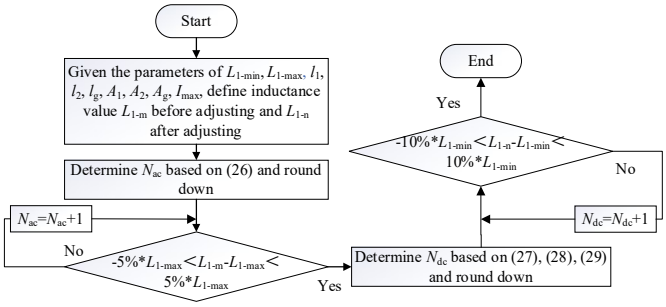

Fig. 8. design flow chart of VI.

Taking the VI's volume and circuit parameters into consideration, ferrite core E B66329 with 0.5mm gap is used to implement VI. Furthermore, the specific parameters of a single VI are listed in TABLE II.

TABLE II
KEY PARAMETERS OF A SINGLE VI

Symbol	Quantity	Value
n	Number of E cores	2
l_1	Length of magnetic path for auxiliary winding	71.6 mm
l_2	Length of magnetic path for main winding	36 mm
l_g	Gap length of VI	1 mm
A_1	Effective area of ferrite core for auxiliary winding	128 mm^2
A_2/ A_g	Effective area of ferrite core for main winding and air gap	244 mm^2
N_{ac}	Turns of main winding	18
N_{dc}	Turns of auxiliary winding	36

Two mock-ups of the VI are constructed by using the parameters shown in TABLE II, and their self-inductance L as the function of DC control current I_{dc} is depicted in Fig. 9. From Fig. 9, two phenomena can be illustrated: 1) The variational trends of two VIs are approximately the same with the same control current I_{dc}. 2) The maximum and minimum values of the experimental results are approximately equal to the design values, which verifies the correctness of the theory discussed in this Section.

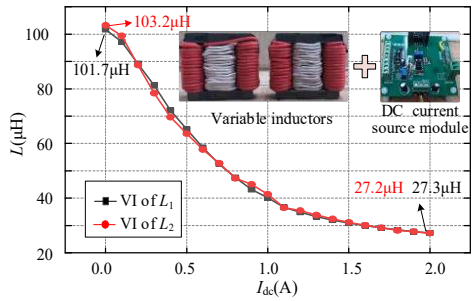

Fig. 9. Experimental results of two designed VI.

V. Efficiency Analysis

A. ZVS Achievement

Generally, ZVS operation can be achieved when the zero-crossing phase of the current (the input impedance angle θ) is larger than the phase of the triggering signal S_4 (the phase-shift angle). Fortunately, the phase-shift angle in the proposed method is zero. This means ZVS can be well maintained as long as the impedance of the inverter output side is inductive.

According to (13), the output impedance of each half-bridge inverter can be calculated by

$$\begin{cases} Z_1 = Z_2 = \dfrac{\dot{V}_P}{\dot{I}_1} = 2R_{eq.P} + j\omega L_1 \\ \theta = \text{ac tan}\left(\dfrac{\omega L_1}{2R_{eq.P}}\right) \end{cases} \tag{30}$$

where Z_1 and Z_2 are the impedance of inverter's output side respectively; θ is the impedance angle of Z_1 and Z_2.

Obviously, the MOSFETs S_1-S_4 can achieve ZVS operation due to the series of VI.

B. Power Loss and Efficiency Analysis

To further evaluate the effectiveness of the proposed method, power loss and efficiency analysis are necessary.

1) Inverter

$$\begin{aligned} P_{inverter} &= P_{Cond} + P_{SW} \\ &= 2I_1^2 r_m + 4\sqrt{2}V_{dc}I_1\left|\sin\theta\right|\left(\frac{E_{off}}{V_{DD}I_D} + \frac{Q_{DD}}{I_{R_D}}\right)f \end{aligned} \tag{31}$$

where P_{SW} represents the MOSFETs' switching loss; E_{off} is the turn-off energy loss of MOSFET; V_{DD} and I_D are the reference drain-source voltage and source current of MOSFET; Q_{DD} and I_{R_D} are the reverse recovery charge and the reference current of the diode, respectively [20], [21].

2) Rectifier

$$\begin{aligned} P_{rectifier} &= \frac{4}{T}\int_0^{\pi}\left(V_f + r_d i_S\right)i_S \mathrm{d}(\omega t) \\ &= \frac{4\sqrt{2}}{\pi}V_f I_S + 2r_d I_S^2 \end{aligned} \tag{32}$$

where V_f is the diode forward voltage; r_d is the equivalent on-state resistance of the anti-parallel diodes [20], [21].

3) Passive elements

$$P_{elements} = R_P I_P^{\,2} + R_S I_S^{\,2} \tag{33}$$

4) Variable inductors

$$P_{VI} = V_{aux} I_{dc} \tag{34}$$

where V_{aux} is the DC voltage in the auxiliary linear circuit of the VI.

Therefore, the system efficiency can be obtained by

$$\eta = \frac{P_{out}}{P_{in}} = \frac{P_{out}}{P_{out} + P_{inverter} + P_{rectifier} + P_{elements} + P_{VI}} \tag{35}$$

To verify the correctness of the equation above, a simulation circuit based on LTSPICE has been built, and the type of MOSFETs and diodes are rebuilt referred to C2M0080120D and DSEI2X61-06C, respectively. Furthermore, the calculation results are listed in TABLE III, which are approximately the same as the simulated results shown in Fig. 10. As can be seen, the inverter loss is relatively lower compared with others, and thus, the overall efficiency is pretty high.

TABLE III
Output and Losses of System

	P_{out}	$P_{inverter}$	$P_{rectifier}$	$P_{elements}$	P_{VI}	η
12 Ω	108 W	0.52 W	7.34 W	3.1 W	0.57 W	90.35%
24 Ω	216 W	1.91 W	7.34 W	6.0 W	1.80 W	92.68%
36 Ω	144 W	1.90 W	4.71 W	4.4 W	1.08 W	92.25%
48 Ω	108 W	1.94 W	3.55 W	4.0 W	0.82 W	91.29%
60 Ω	86.4 W	1.95 W	2.85 W	3.8 W	0.72 W	90.26%
72 Ω	72 W	1.91 W	2.35 W	3.6 W	0.61 W	89.47%

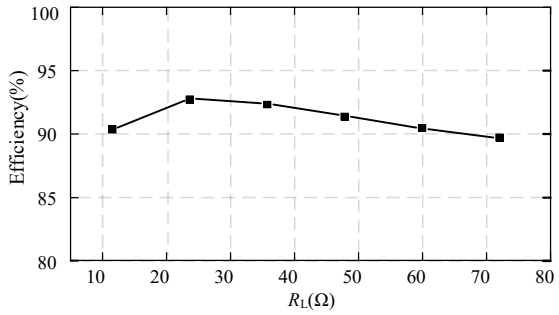

Fig. 10. Simulated results of efficiency by using LTSPICE.

VI. Experimental Verifications

A. Laboratory Prototype

A laboratory prototype is built to validate the proposed topology and the control method, as shown in Fig. 11. The actual circuit parameters of the prototype are listed in TABLE IV. MOSFETs (C2M0080120D) are used as the switches S1-S4 of the inverter, and their drive PWM signals are generated by a digital signal processor (DSP, TMS320F28335). A DC current source module is utilized for VI control. All waveforms were recorded using an Agilent DSO-X 4034A oscilloscope.

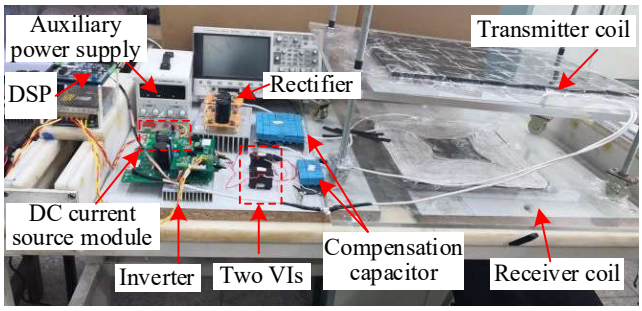

Fig. 11. Laboratory prototype.

TABLE IV
Circuit Parameters of Prototype

Symbol	Quantity	Value
V_{out}	Charging voltage of battery	72 V
I_{out}	Charging current of battery	3 A
V_{dc}	DC input voltage	150 V
ω	Operating angular frequency	$1.7\pi\times10^5$
L_P/ L_S	Self-inductance of primary coil / secondary coil	247.8/ 301.62 μH

R_P/ R_S	ESR of primary coil/ secondary coil	0.26/ 0.34 Ω
C_P/ C_S	Resonant capacitance of primary coil / secondary coil	14.15/ 11.62 nF
M	Mutual inductance of coupler	30.42 μH
R_L	Equivalent load resistance of the battery packs	10 Ω-24 Ω (CC) 24 Ω-72 Ω (CV)

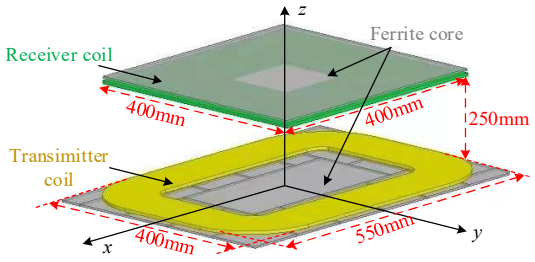

Fig. 12. Size of coil structure.

The finite element analysis software Maxwell is used to design the coupler and its structure, which is shown in Fig. 12 with specifications in length, width, and air gap. In this experimental prototype, coils are made of 1300-strand litz-wires with a diameter of 5mm. The primary and secondary coils are set as 15 turns and 24 turns, respectively. As shown in Fig. 12, the distance of the air gap is designed as 25 cm, and the mutual inductance is 30.42 μH.

B. *Experimental Results*

To demonstrate the versatility of the proposed DHB topology and the VI control method, the conventional PS control is selected as a benchmark to compare the efficiency between the two methods when the same outputs are achieved. The waveforms of the inverter output voltage v_P, output current i_P, and rectifier output voltage V_{out}, output current I_{out} under two control methods are shown in Fig. 13. As can be seen from Fig. 13 (a) and (b), when R_L=12 Ω, both control methods can stabilize the output current at the desired value I_{out}=3 A. Similarly, constant output voltage V_{out}=72 V can also be achieved when R_L=48 Ω by two methods shown in Fig. 13 (c) and (d).

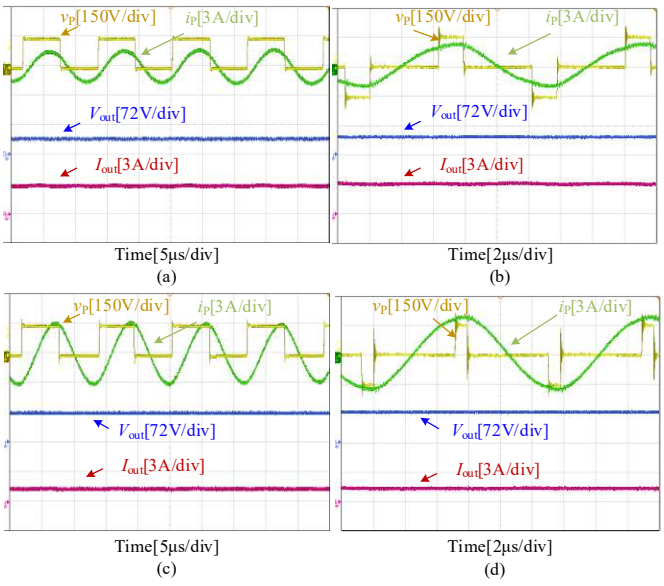

Fig. 13. Waveforms of inverter's output voltage v_P, output current i_P and rectifier's output voltage V_{out}, output current I_{out} under two control methods. (a) when R_L=12 Ω with VI control method, (b) when R_L=12 Ω with PS control method. (c) when R_L=48 Ω with VI control method. (d) when R_L=48 Ω with PS control method.

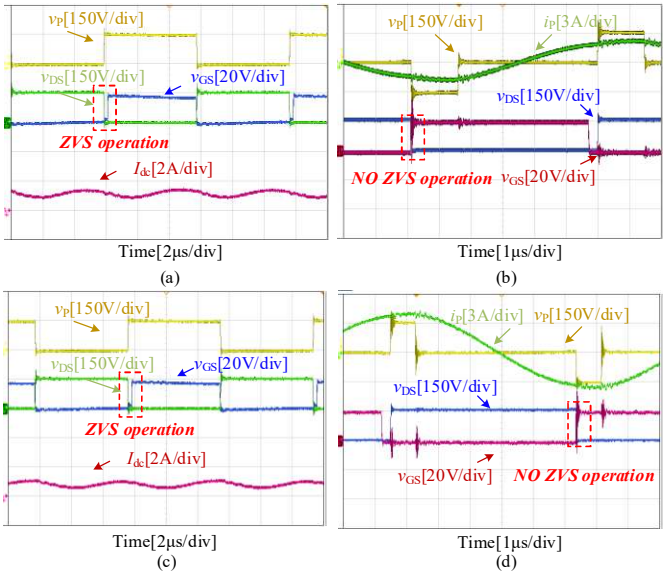

Fig. 14. Waveforms of drain-source voltage v_{DS} and gate-to-source voltage v_{GS}. (a) when R_L=12 Ω with VI control method, (b) when R_L=12 Ω with PS control method. (c) when R_L=48 Ω with VI control method. (d) when R_L=48 Ω with PS control method.

Generally, the drain-source voltage v_{DS} and gate-to-source voltage v_{GS} are used to prove the implementation of ZVS operation [22]. Specifically, ZVS is well realized if v_{DS} reaches zero before v_{GS} arrives. By observing the MOSFET S_1 of the DHB inverter with VI control and the MOSFET S_4 of the FB inverter with PS control, the waveforms in Fig. 14 compares the results of ZVS for both control methods. Fig. 14 (a) and (c) corresponds to the proposed method, and Fig. 14 (b) and (d) corresponds to the conventional method. As shown in Fig. 14 (a) and (c), the drain-source voltage v_{DS} drops to zero before the gate-to-source voltage v_{GS} rises regardless of load variations. This proves the DHB inverter realizes ZVS and the switching loss can be reduced. By contrast, ZVS is difficult to achieve with PS control method because of the change in the initial phase of the inverter output voltage, as verified in Fig. 14 (b) and (d).

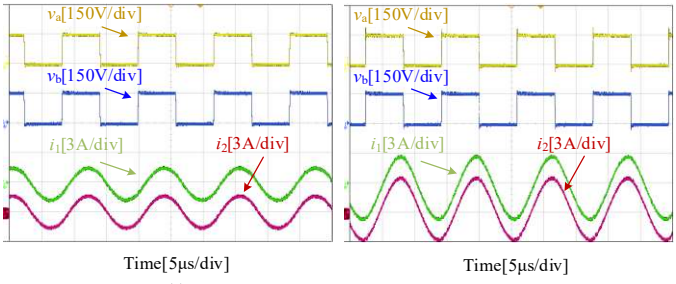

Fig. 15. Waveforms of two half-bridge inverter's output voltage v_a, v_b and output current i_1, i_2 (a) when R_L=12 Ω, (b) when R_L=48 Ω.

Furthermore, Fig. 15 shows the waveforms of the output voltage v_a, v_b and current i_1, i_2 of two half-bridge inverters at different value of loads by using the proposed topology and control method. It can be seen that the waveform of i_1 is the same as that of i_2, which means there is no circulation current between these two inverters, i.e., the circulation losses will not

exist. Moreover, due to the equal distribution of the primary coil current, the current through every MOSFET is reduced by half so that the conduction loss is reduced by a quarter, which further improve the system efficiency. These results are in line with our theoretical analysis in Section. II.

C. *Efficiency Comparison*

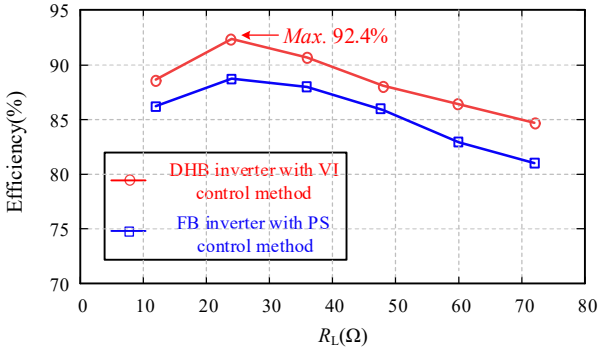

Fig. 16. Efficiency comparison between the proposed method and conventional method.

Fig. 16 shows the efficiency comparison between the proposed method and the conventional method when the load varies from 12 Ω to 72 Ω. An obvious improvement of system efficiency can be observed in Fig. 16 with the maximum efficiency of 92.4% using the proposed control method. Specifically, the efficiency difference between two methods reaches the maximum value of 3.69% when the load is 72 Ω.

VII. Conclusion

In this paper, a method regulating the output power of a WPT system based on DHB inverter topology with variable inductance is proposed. The method could reduce the conduction loss and switching loss at the same time. Based on the detailed theoretical analysis, an experimental prototype was built to verify the charging process of the battery. The experimental results prove that the system's output can be maintained at the desired value when the load varies. Besides, the elimination of the inverter's circulation current is also verified in the experiment. As a result, the efficiency of the system is significantly improved compared with the traditional PS control with a maximum efficiency of 92.4%.

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