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Optimization of normally-off β-Ga_2O_3 MOSFET with high I_{on} and BFOM: A TCAD study

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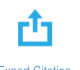
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ABSTRACT

A combination of recessed-gate and gate-field plate in lateral β-Ga_2O_3 metal–oxide–semiconductor field-effect transistor (MOSFET) is proposed in the Technology Computer Aided Design study to improve its ON resistance (R_{ON}) and breakdown voltage. Enhancement-mode (E-mode) is achieved by controlling the thickness of the recessed-gate. Lateral E-mode β-Ga_2O_3 MOSFET achieves a saturation current density near 120 mA/mm, I_{ON}/I_{OFF} ratio ~10^9, R_{ON} ~91 Ω mm, and breakdown voltage of 1543 V. The optimized structure results in a prediction of a power figure-of-merit of 261 MW/cm^2 in a horizontal E-mode β-Ga_2O_3 MOSFET.

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I. INTRODUCTION

Beta-gallium oxide (β-Ga_2O_3) is a promising wide bandgap semiconductor for power electronic devices, solar-blind UV photodetectors, photocatalysts, gas sensors, solar cells, phosphors, and transparent conducting films for electrodes in a variety of optoelectronic devices.[1–5] An ultrawide bandgap of 4.5–4.9 eV and a consequent high theoretical breakdown electric field strength (E_C) of 6–9 MV/cm[6] lead β-Ga_2O_3 experimentally to surpass other materials, such as GaN and SiC.[7] Baliga's figure of merit ($BFOM = \varepsilon\mu E_C^3 = V_{br}^2/R_{on,sp}$) of 3444 for β-Ga_2O_3 is ~3 × GaN and ~8 × 4H–SiC, making Ga_2O_3 a potential candidate in low-lost power switch applications.[8] The possibility of high-quality low-cost wafers ranging from semi-insulating to moderate or highly n-doped via a melt growth method, such as Czochralski (CZ),[9] or edge-defined film-fed growth (EFG),[10] is its other advantage. It is known that a challenge in improving Baliga's Figure of Merit (BFOM) of Ga_2O_3 metal-oxide semiconductor devices is from the dielectric breakdown ($E_{ox,br}$) governed by a practical maximum surface electric field, $E_{SURF\ max} = \varepsilon_{ox} \times E_{ox,br}/\varepsilon_s$.[11] Using $\varepsilon_{SiO2} = 3.9$, a critical field of 40 MV/cm for SiO_2, and $\varepsilon_{HfO2} = 20$, a critical field of 13 MV/cm for HfO_2,[12] $E_{SURF\ max}$ is estimated to be 1.56 and 2.60 MV/cm for SiO_2 and HfO_2, respectively. Recently, V_{br} and $R_{on,sp}$ have been improved to achieve high BFOM for a vertical β-Ga_2O_3 transistor. Jena *et al.* reported a vertical enhanced-mode Ga_2O_3 transistor with a high V_{br} of 0.96 kV and an output current of 1.0 kA/cm^2. Higashiwaki *et al.* employed an $(AlGa)_2O_3$ layer as a barrier to confine electrons in a channel layer, obtaining the threshold voltage (V_{th}) of +8 V with the subthreshold voltage (SS) of 129 mV/decade, three times smaller as compared to a non-back-barrier counterpart.[13] However, comparing the vertical and the lateral designs in terms of integrability into the CMOS processes, required in smart power devices, clearly favors the lateral field effect transistor. Depletion-mode β-Ga_2O_3 metal–oxide–semiconductor field-effect transistors (MOSFETs) have been initially studied[1419] after the first demonstration of lateral β-Ga_2O_3 MOSFETs by Higashiwaki *et al.*,[20] which limits the enhancement-mode (E-mode) of operation. Several configurations, such as wrap-gate fin arrays,[21] unintentional doping (UID) channel,[22] back gate structure with p + -doped Si,[16] source-field plate,[23] gate-field plate,[24] a variation lateral-doping (VLD),[25] and recessed-gate (RG),[5,26] have been investigated to realize the normally off β-Ga_2O_3 MOSFET. Although many attempts to improve BFOM via increasing V_{br} and reducing R_{on}, the values of BFOM of lateral devices remain much smaller as compared to vertical configuration. In detail, BFOM has been optimized to 11.4–276.7 MW/cm^2, corresponding to a breakdown voltage of 0.7–3.0 kV.[17,18,23,24,26,27]

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The main disadvantage in terms of increasing ($BFOM = V_{br}^2/R_{on,sp}$) is from their lateral structures, where V_{br} and $R_{on,sp}$ are both proportional to the drain–source distance (L_{SD}). This relationship explains why a low BFOM of 55.4 MW/cm^2 was obtained with high V_{br} ~ 3 kV.[24] To improve V_{br} of lateral Ga_2O_3 MOSFETs, source-field plates[28] and gate-field-plate MOSFETs have also been employed[18] for D-mode Ga_2O_3 MOSFETs, obtaining BFOM of 355 and 277 MW/cm^2, respectively. However, E-mode operation is more preferred for integration. Recessed-gate MOSFETs[26] and ferroelectric charge storage gate MOSFETs (FMOSFETs)[24] have also been recently reported for E-mode operation with BFOM of 11.8 and 192.5 MW/cm^2, respectively. The saturation current of recessed-gate Ga_2O_3 MOSFET is twice that of FMOSFETs (at V_D = 15 V, V_{DS} = 7.5 V), so the recessed-gate Ga_2O_3 MOSFET should be a potential candidate for the next E-mode power devices due to the lack of p-type Ga_2O_3 for turning off the gate. However, systematic studies of a recessed-gate Ga_2O_3 MOSFET have not been thoroughly conducted in terms of recessed-thickness, high-k dielectric layers.

This work contributes toward the challenge of developing normally off β-Ga_2O_3 MOSFET. The simulated device is calibrated against experiment,[26] considering the effects of interface traps, and the lateral recessed-gate β-Ga_2O_3 MOSFET is optimized to obtain an E-mode device. The breakdown voltage of recessed-gate β-Ga_2O_3 MOSFET is improved by combining the advantage of the recessed-gate structure by using high-k material and a gate-field plate structure. The best-in-class predicted to date of a power figure-of-merit (PFOM) is obtained for a horizontal E-mode β-Ga_2O_3 MOSFET.

II. METHODOLOGY AND SETTINGS

The β-Ga_2O_3 MOSFETs were simulated using the Silvaco Atlas 2-D device simulation tool.[29] Two structures, namely, recessed-gate (without field plate) and field-plate recessed-gate (double gate), shown in Figs. 1(a) and 1(b), respectively, were simulated. Both devices consist of a channel layer of 200 nm Si-doped β-Ga_2O_3 on a semi-insulating Fe-doped Ga_2O_3 substrate. The bandgap of 4.8 eV and electron affinity of β-Ga_2O_3 of 4.0 eV is adopted. A typical recessed-gate Ga_2O_3 MOSFET with gate oxide and passivation oxide SiO_2 is shown in Fig. 1(a) by following the typical dimensions in the previous report.[26] The work-function of the gate-electrode is fixed at 4.33 eV, corresponding to the work function of Ti.[30] The metal/Ga_2O_3 contact is assumed Ohmic with the resistance of 25 Ω mm.[26] Both a gate-length (L_G) and a source-to-gate distance (L_{SG}) are fixed at 1 μm, while a source-to-drain distance (L_{SD}) is varied from 3 to 10 μm. The field-plate recessed-gate Ga_2O_3 MOSFET, shown in Fig. 1(b), is constructed based on the device in Fig. 1(a) where gate oxide SiO_2 is replaced by HfO_2, and a field-plate gate with the gate length L_{G2} of 4 μm is added on the passivation oxide SiO_2 layer. To consider the effects of the high field on mobility and carrier concentration on carrier lifetime, a high field model and a concentration-dependent lifetime model were included. The Auger recombination model was utilized to count the effect of high electron concentration (N_e), and a thermal model was employed to consider the self-heating effect. An impact ionization model was employed only for the breakdown voltage simulation using a transient method. TCAD parameters are calibrated against device structure in Fig. 1(a) through experimental I_DV_D, I_DV_G, breakdown voltage (V_{br}), and density of interface traps (D_{it}).[26,31] Electron low field mobility is set to be 106 cm^2/Vs. Because of the damage of etching, the recessed-channel should have worse quality as compared to other regions, its low field mobility is kept at 31 cm^2/Vs, which gives the best fit for experiment.[26] A channel carrier-concentration (N_D) of 5.5×10^{17} cm^{-3} and the acceptor traps of 5.0×10^{17} cm^{-3} in semi-insulating Ga_2O_3 substrate are found to be the best fit for experiments.[32] The simulated V_{br} of 504.91 V fits well with the experimental result,[26] connected with a peak of E_C of ~21.8 MV/cm on the SiO_2 side, which is in agreement with the experimental E_C of SiO_2.[33] Multi-level interface traps are added to the model to fit I_DV_G and I_DV_D, where the peak of interface trap density (D_{it}) of 7.82×10^{11} cm^{-2} eV^{-1} at 0.3 eV from the conduction band is consistent with experimental reports.[31]

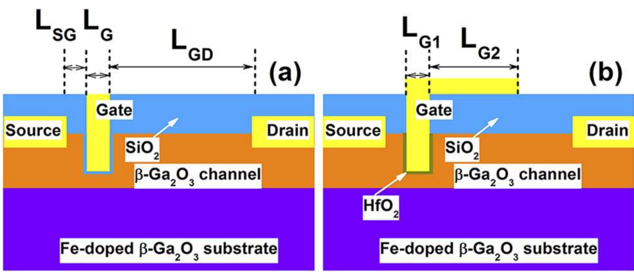

FIG. 1. Schematic cross section of (a) the recessed-gate Ga_2O_3 MOSFET without field plate and (b) the recessed-gate Ga_2O_3 MOSFET with field-plate.

III. RESULTS AND DISCUSSIONS

A. Effect of recess-thickness on threshold voltage (V_{th})

Because of a lack of a p-type channel, Ga_2O_3 MOSFET is a junctionless device, controlled by depletion layer modulation under the gate bias. In this simulation, the effect of t_{rc} on V_{th} is investigated by simulating recessed-gate Ga_2O_3 MOSFETs in Fig. 1(a) with t_{rc} varied from 50 to 100 nm. Figure 2(a) shows a band-diagram of RG Ga_2O_3 MOSFETs at V_G = 0, extracted from the cutline at the center of the gate. The device is found to operate in E-mode when the channel thickness is less than 70 nm, reaching $E_C - E_F = 0.38$ eV and $V_{Th} = 2.3$ eV at t_c = 60 nm, shown in Fig. 2(b). At t_{rc} larger than 75 nm, the effect of channel thickness on $(E_C - E_F)$ is small; however, this effect is evident for t_{rc} less than 75 nm. The results agree well with a previous report[21] where the device operation in E-mode for t_{rc} of 60 nm. The position of the Fermi-level in Fig. 2(a) can be determined from following equation:[34]

$$E_C - E_F = -k_0 T ln\left(\frac{N_e}{N_C}\right), \tag{1}$$

where k_0 is Boltzmann constant, T is temperature, N_e is an electron concentration in a recessed channel, and N_C is conduction band effective state density of 3.72×10^{18} cm^{-3}.[29] Equation (1) also

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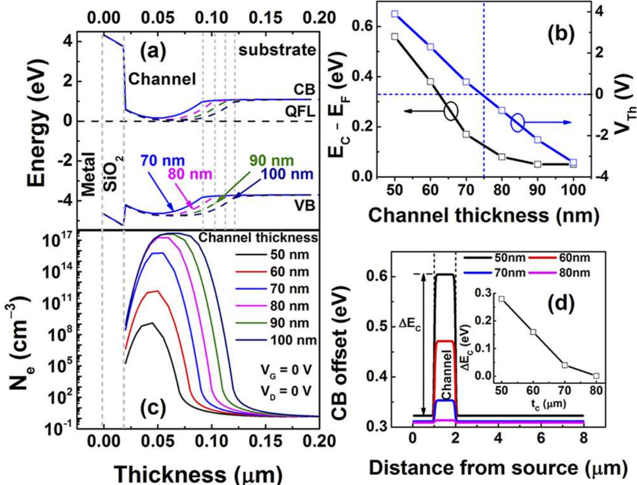

FIG. 2. (a) Band-diagram of recessed-gate Ga_2O_3 MOSFETs as a function of t_{rc} at V_G = 0 V. (b) The relationship between the position of Fermi-level, threshold voltage, and channel thicknesses. (c) Electron concentration (N_e) from gate to the substrate of the structure of Fig. 1(a). (d) The relationship between conduction band offset and channel thickness from source to recessed channel to drain at 20 nm above the β-Ga_2O_3/substrate interface.

explains well N_e in a recessed-channel shown in Fig. 2(c), where N_e decreases significantly when the t_{rc} decreases, from 5.5×10^{17} cm^{-3} at t_{rc} of 100 nm to 1.3×10^9 cm^{-3} at t_{rc} of 50 nm. A strong reduction of N_e leads to a notable drop in output current (64%), which is attributed to the formation of a barrier ~0.3 eV between source and drain shown in Fig. 2(d), high enough to approach a normally off state. The results are in agreement with the report of Wong *et al.*, where positive threshold voltage (V_{th}) was obtained at t_{rc} less than 100 nm; however, a significant reduction of I_{ON} (~97%) was observed.[35]

To see the advantage of recessed gate β-Ga_2O_3 MOSFET, un-recessed gate β-Ga_2O_3 MOSFETs with different channel thicknesses are simulated in Fig. 3. Figures 3(a) and 3(b) show a shift of threshold voltage from negative to positive when channel thickness decreases from 100 to 60 nm. However, the current obtained is very small, as shown in Fig. 3(a), due to a depletion region formed at the channel/substrate interface, as shown in Fig. 3(c). At tc = 60 nm, electron concentration in the channel is less than 1×10^{15} cm^{-3} although the $N_D = 5.5 \times 10^{17}$ cm^{-3}. This disadvantage can be eliminated with the recessed gate in Fig. 3(d), where a depletion region dominates only in the recessed region, below the gate, and charge concentration in other regions is un-changed due to the thick un-recessed region. Figure 3(e) indicates that the ON current of the recessed device is 4 orders larger than that of an un-recessed device. It means that a recessed structure keeps V_{th} positive as well as prevents a collapse of the ON current when the channel thickness is reduced.

B. Effect of field-plate and recessed-gate on device performance

To improve the performance of RG Ga_2O_3 MOSFETs, a combination of gate-field plate and recessed-gate (double gate) is studied

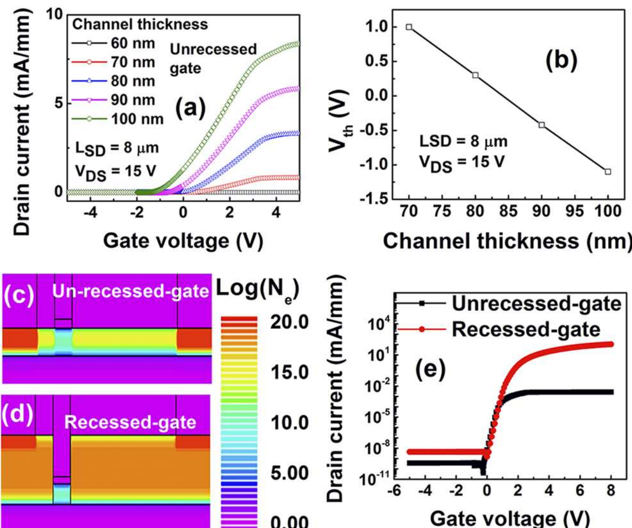

FIG. 3. (a) IDVG characteristics of an un-recessed gate β-Ga_2O_3 MOSFET with a range of channel thicknesses from 60 to 100 nm. (b) The variation of threshold voltage as channel thickness increases from 70 to 100 nm, the threshold voltage of a device with 60 nm cannot be extracted because the maximum current is less than 0.1 mA/mm. Electron concentration in the channel of (c) an un-recessed gate β-Ga_2O_3 MOSFET with a channel thickness of 60 nm and (d) recessed gate β-Ga_2O_3 MOSFET with a channel thickness of 200 nm and recessed-channel of 60 nm. (e) IDVG characteristics in the semi-log scale of structures (a) and (b) in Fig. 1.

in Fig. 1(b). The parameters used in this simulation are the same as those used in Fig. 1(a), but HfO_2 with a thickness of 20 nm is utilized as a gate oxide. The D_{it} profile is assumed to be the same as that used in Fig. 1(a). SiO_2 remains as oxide passivation on the Ga_2O_3 surface. Power figure-of-merit ($PFOM = V_{br}^2/R_{ON,sp}$) is extracted from the devices with the source–drain distance from 3 to 10 μm, where $R_{ON,sp}$ is a specific resistance ($R_{ON,sp} = R_{ON} \times L_{SD}$) and compared with Ga_2O_3 MOSFETs without gate-field plate (single gate). It is seen that both single and double gated devices have the same V_{th} (+1.43 V) and the I_{ON}/I_{OFF} ratio $>10^9$. R_{ON} of gate field plate device, shown in Fig. 4(a), is smaller as compared to that of without

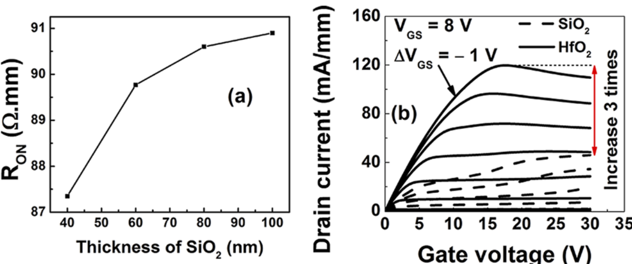

FIG. 4. (a) On resistance of gate field plate MOSFETs as a function of SiO_2 passivation layer below the field plate; HfO_2 is used as a dielectric material. (b) Comparison of IDVD characteristics of the single gate and gate-field plate devices using SiO_2 and HfO_2 as the gate oxides.

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gate field plate device (R_{ON} = 92.1 Ω mm) because of the redistribution of charge concentration of a channel below the field plate. Figure 4(a) indicates that ON resistance of gate field plate device is a function of the thickness of SiO_2 passivation layer, decreasing as t_{SiO2} decreases, reaching 87.35 Ω mm at t_{SiO2} = 40 nm. Figure 4(b) shows the IDVD characteristics of gate field plate and without gate field plate devices. It is found that the saturation current density of the gate field plate device with HfO_2 gate oxide increases three times as compared to that without field plate device with SiO_2 gate oxide, due to a smaller capacitance oxide thickness (CET).[12] The low value of R_{ON} of gate field plate device as compared to that without gate field plate device should be from the double effect of the recessed-gate and a high permittivity of HfO_2, resulting in more flexible control of semiconductor Fermi-level. Figure 5 illustrates that the breakdown voltage of a double gate device is twofold larger as compared to that of a single gate device. The breakdown voltage of 1543 V, in this study, is the highest to date value predicted for E-mode RG β-Ga_2O_3 MOSFETs. For comparison, Feng *et al.* reported the V_{br} of 670 V and low subthreshold voltage (SS) of 72 mV/dec by using ferroelectric oxide in the gate stack. Zhou *et al.* predicted a high breakdown voltage of 1832 V in a TCAD study of VLD β-Ga_2O_3 MOSFETs.[25] However, the lack of a clear physical picture of negative capacitance MOSFETs[36] and a complex fabrication-process of VLD devices leave a challenge in realizing these devices.

To explain the improvement of breakdown voltage in the double gate device, a simulation of electric field (E-field) distribution is conducted at V_{DS} = 600 V and V_G = 0 V shown in Fig. 6. The peak of E-field in a single gate device appears at the edge of the gate electrode shown in Fig. 6(a), while that in a double gate device was observed at the edge of the gate-field-plate/SiO_2 interface shown in Fig. 6(b). The E_C ~ 40 MV/cm of SiO_2[37] and a re-distribution of E-field in Fig. 6(c), where E_C drops by 50% at the HfO_2/β-Ga_2O_3 interface, explains the improvement of V_{br} of the double gate device. Figure 7 shows the benchmark plot of R_{ON} vs V_{br}, illustrating an increase of ~20 times of PFOM during a period of 5 years, from 11 MV/cm^2 (D-mode β-Ga_2O_3 MOSFETs) to 293 MV/cm^2 (VLD β-Ga_2O_3 MOSFETs).[17,18,23–26,38] Despite having low $R_{ON,sp}$ and fast switching speed, obtaining high V_{br} for E-mode RG β-Ga_2O_3 MOSFET remains to be a challenge due to its

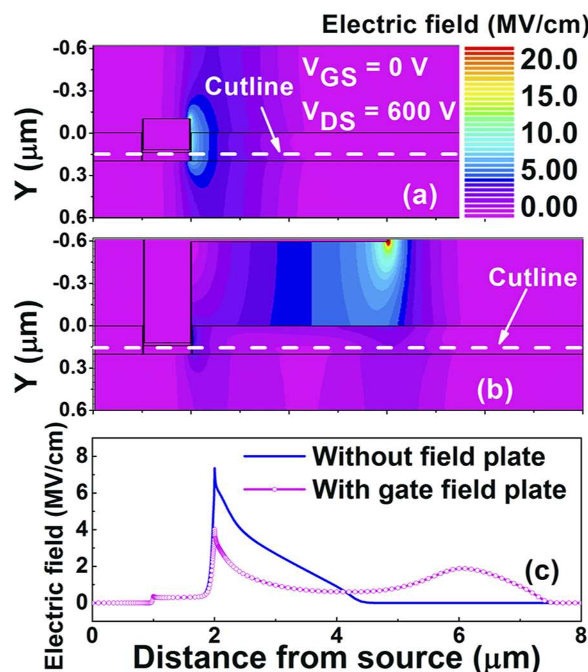

FIG. 6. Electric field distribution at V_{GS} = 0 and V_{DS} = 600 V of (a) single gate device, (b) gate-field plate device, and (c) cutlines along HfO_2/Ga_2O_3 interface from source to drain.

thin t_{rc}. The up-to-date PFOM of 193 MV/cm^2 was experimentally reported by Feng *et al.* for this configuration[24] by using ferroelectric dielectric $Al_2O_3/Hf_{0.5}Zr_{0.5}O_2$ as a gate oxide. Recently, a record high PFOM of 0.65 GW/cm^2 was reported for the NiO/β-Ga_2O_3 pn diode. The simulated PFOM of 261 MW/cm^2 obtained in this study is the highest value for E-mode RG β-Ga_2O_3 MOSFET. A combination of recessed-gate structure (low R_{ON}), high permittivity dielectric, and the re-distribution of E-field (high V_{br}) increases PFOM by 21 times as compared to RG β-Ga_2O_3 MOSFET with SiO_2 gate oxide.[26]

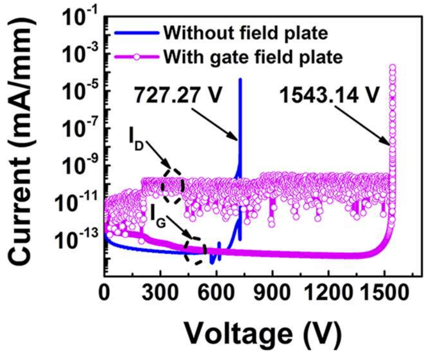

FIG. 5. Simulation results of breakdown voltage for without field plate device and with gate field plate devices. HfO_2 is used as a high-k material for both devices.

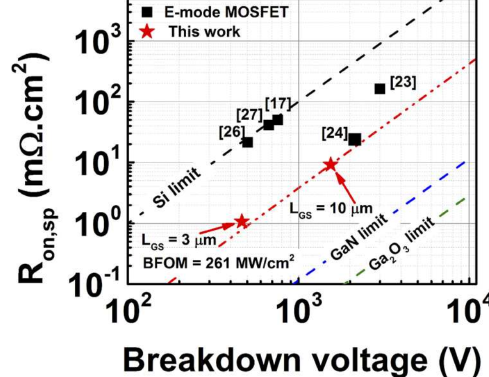

FIG. 7. Benchmark plot of specific resistance vs breakdown voltage compared to the relative theoretical limits of Si, GaN, and β-Ga_2O_3.[23,24,26,17,26]

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IV. CONCLUSION

In summary, we systematically study β-Ga_2O_3 MOSFET using TCAD simulation. High performance normally off recessed gate-field plate β-Ga_2O_3 MOSFET is predicted using TCAD simulation. All parameters are calibrated against published experimental data of recessed gate β-Ga_2O_3 MOSFET. The impact of recessed-gate thickness is investigated. The output current of E-mode recessed gate-field plate β-Ga_2O_3 MOSFET is obtained to be 120 mA/mm with I_{ON}/I_{OFF} ratio > 10^9 and $R_{ON,sp}$ of 9.1 mΩ cm^2. The simulations suggest a promise of a PFOM of 261 MW/cm^2 in recessed gate-field plate β-Ga_2O_3 MOSFET with potential for advanced power electronics.

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AUTHOR DECLARATIONS

Conflict of Interest

The authors have no conflicts to disclose.

Author Contributions

Huy-Binh Do: Conceptualization (lead); Formal analysis (lead); Investigation (lead); Methodology (lead); Project administration (lead); Writing – original draft (equal); Writing – review & editing (equal). **Anh-Vu Phan-Gia:** Data curation (equal); Investigation (equal). **Van Quy Nguyen:** Investigation (supporting). **Maria Merlyne De Souza:** Software (equal); Supervision (equal); Writing – review & editing (equal).

DATA AVAILABILITY

The data that support the findings of this study are available from the corresponding author upon reasonable request.

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