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Resonant current estimation and voltage regulation for piezoelectric transformer-based power supply

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Abstract

This paper proposes an output voltage regulation approach for a piezoelectric transformer (PT)-based power converter. The inductorless half-bridge configuration is employed to achieve zero-voltage switching. A resonant current estimation circuit is implemented at the output section of the PT, and it is used by a phase-locked loop (PLL) zero voltage switching (ZVS) controller to synchronise MOSFET switching to the zero crossings of the resonant current. Burst-mode control is employed to provide output voltage regulation of the DC/DC converter. Both experimental and simulation results demonstrate the operation of the system.

1. Introduction

Piezoelectric transformer (PT) based resonant converters have been utilised for many applications [1][2][3], and they are considered as a desirable replacement for traditional magnetic transformers. PTs provides high efficiency, high power density, minimal electromagnetic interference and reduced size. PTs are generally constructed from hard piezoelectric materials such as lead-zirconate titanate (PZT), therefore they exhibit high quality factor and low loss.

PT transfers energy between input and output sections using mechanical vibrations. Its input and output capacitance are relatively large because of geometry of the device and thus difficult to achieve zero voltage switching due to insufficient deadtime or charge provided by resonant current, especially without using a series inductor. A critical criteria was developed in [4], which shows that ZVS is guaranteed if the input to output capacitance ratio is below a certain level with $\pi/2$ deadtime, and the circuit operates at resonance at matched load condition.

Since the resonant current is internal to a PT and cannot be measured directly, the resonant current should be estimated in order to generate a feedback signal. Traditional current estimation methods reported in the literature show good effective sign detection for the resonant current, these methods use either anti-parallel diodes or a voltage differentiator [5][6]. However, they exhibit one or more of the drawbacks: 1) primary estimator implementation could increase total effective capacitance presented at PT input section, making ZVS even more difficult to achieve, 2) the estimated current is sensitive to system noise and could be affected by MOSFET switching events.

Burst-mode modulation has been shown to provide superior performance when compared with pulse-frequency modulation (PFM) and pulse width modulation (PWM) since it provides a higher efficiency and lower harmonics [7][8]. However, traditional burst mode modulation uses a fixed switching frequency, and this is not desirable for PT-based converter since: 1) load variation is limited due to the narrow control bandwidth, 2) the resonant frequency of the PT will shift due to variations in temperature and load. Therefore, additional compensation is necessary to maximise overall efficiency.

In this work, we propose a phase-locked loop (PLL) controller and burst mode controller with a secondary-side resonant current estimator, to regulate the output voltage while maintaining ZVS operation. By estimating the resonant using only secondary side measurements interference from the MOSFET switching events are avoided improving robustness to noise. The PLL locks onto the estimated resonant current providing a synchronised square wave from which the MOSFET gate signals are derived. Adherence to the critical criterion described in [4] ensures that a particular design can achieve ZVS. The output voltage is regulated through a burst mode controller by adjusting the on/off periods of the switches. The proposed control system is implemented and experimentally validated using a ring dot radial mode PT.

2. Description of piezoelectric transformer-based inductorless resonant converter

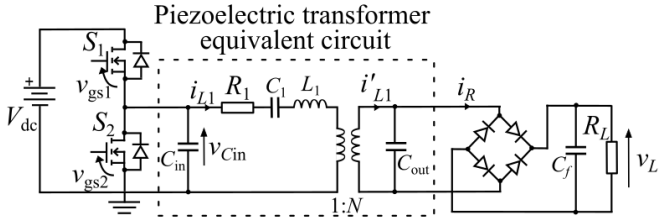


Fig. 1: The inductorless half-bridge driven PT-based converter

Piezoelectric transformers are typically constructed from PZT material and couple energy electromechanically from the input to the output electrodes via mechanical vibrations. High electrical efficiency can be achieved when a PT operates close to its primary resonant frequency due to its high Q factor

nature. The electrical behaviour of a PT can be characterised by the Mason equivalent circuit, as shown in Fig. 1.

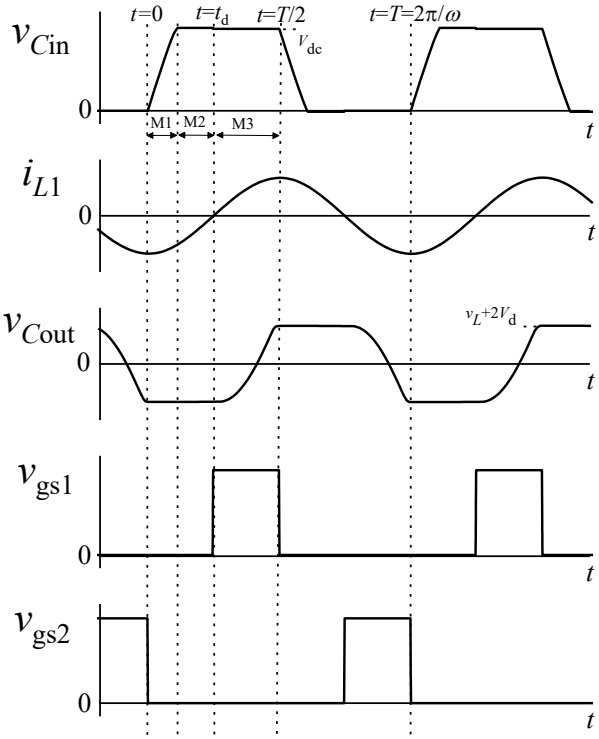


Fig. 2: Switching waveforms of the PT-based converter

During a half-cycle period, the inductorless PT-based converter exhibits three modes of operation (M1, M2 and M3), as shown in Fig. **2**. The resonant current is assumed to be sinusoidal since the PT is generally constructed from high Q-factor material. t_{d} corresponds to the deadtime. The gate drive signals are represented as v_{gs1} and v_{gs2}. $\grave{i_{L1}}$ is the current flow at the PT output section and is related to the resonant current i_{L1} through the ideal transformer which has a ratio 1:*N*. As can be seen from Fig. **2**, ZVS operation is obtained with the following mode sequence M1-M2-M3.

- M1: Both S_1 and S_2 are off. The PT input capacitance-voltage $v_{C\mathrm{in}}$ is charged by resonant current. $v_{C\mathrm{in}}$ is being charged towards V_{dc} (or heading towards 0V for the negative half-cycle).
- M2: $v_{C\mathrm{in}}$ has exceeded DC link voltage (or fallen below 0V) and the body diode of S_1 (or S_2) conducts such that $v_{C\mathrm{in}} = V_{\mathrm{f}}+V_{\mathrm{dc}}$ (or $v_{C\mathrm{in}} = -V_{\mathrm{f}}$), where V_{f} is the forward voltage drop of the body diode.
- M3: S_1 (or S_2) is on and $v_{C\mathrm{in}}$ is maintained at V_{dc} (or 0V).

To provide a DC output voltage, a capacitively smoothed full-bridge rectifier is used in this work, since it reduces both geometric constraints of the PT design and conversion ratio requirement for a given output power [9].

To achieve ZVS for an inductorless PT-based converter, both deadtime t_{d} and resonant current i_{L1} should be sufficient to guarantee $v_{C\mathrm{in}}$ charged from 0 to V_{dc}. In [4], we developed a design criterion to ensure ZVS can always be achieved if the input-to-output capacitance ratio satisfies $C_{\mathrm{in}}/(N^2 C_{\mathrm{out}}) \leq 2/\pi$ with $\pi/2$ deadtime angle, thereby guaranteeing the deadtime begins at the negative peak of i_{L1} thereby providing the maximum current to change $v_{C\mathrm{in}}$.

3. Operation of the proposed control system

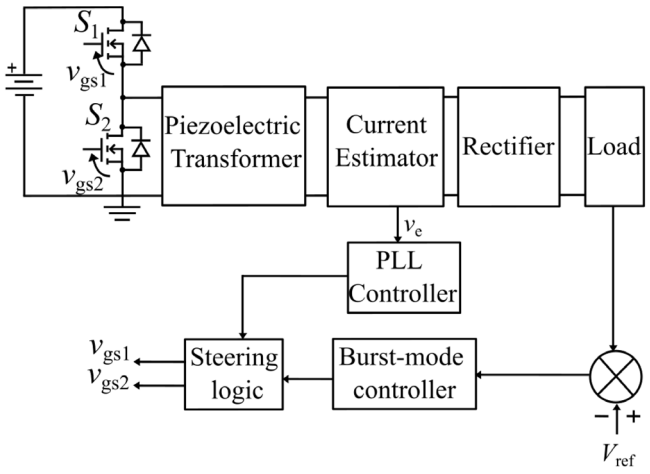


Fig. 3: Circuit block diagram of the proposed control system

The proposed control system includes a resonant estimator, a burst-mode controller and a PLL controller, as shown in Fig. **3**. Since the resonant current is internal to the PT and cannot be measured directly, a resonant current estimator is employed after the PT output section, to reconstruct i_{L1} for the PLL controller. Therefore, the resonant current is locked on by the PLL controller and in-phase gate drive signals are generated through steering logic. Subsequently, the output voltage is rectified and regulated through burst-mode modulation. Finally, the on/off periods of the MOSFETs are dynamically adjusted from the burst-mode signal generated by a hysteresis window with voltage regulation limit.

3.1. Resonant current estimation

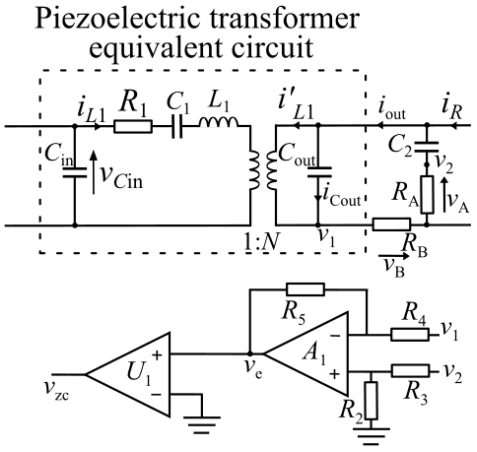


Fig. 4: Resonant current estimation circuit

Since $\grave{i_{L1}}$ is a scaled version of the resonant current i_{L1}, they exhibit the same polarity and, therefore, $\grave{i_{L1}}$ can be estimated by combining measurements of output capacitor current $i_{C\mathrm{out}}$ and PT output current i_{out}. The two current signals are combined using a differential amplifier A_1, to provide the current estimate signal v_e. Comparator U_1 detects the zero-crossing of current estimate which is then provided to the PLL as voltage v_{zc} for simultaneous phase and frequency

locking. As can be seen from Fig. 4, R_A senses the PT output capacitor current while R_B senses the PT output current. Therefore, a scaled version of i_{Cout} and i_{out} can be generated (if R_AC_2<<T and R_BC_{in}<<T, where T is the switching period) to reconstruct the resonant current i_{L1}.

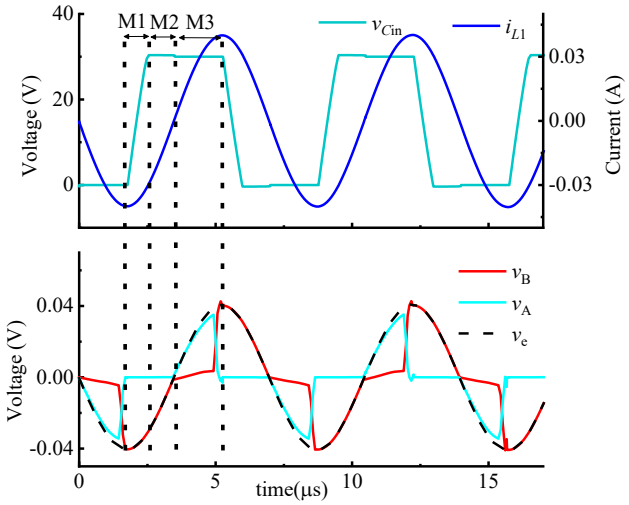


Fig. 5: Switching waveforms of the current estimator

$$i_{L1} = \frac{1}{N}\left(\frac{v_2 C_{out}}{C_2 R_A} - \frac{v_1}{R_B}\right) \quad (1)$$

Therefore, resonant current is estimated as

$$v_e = v_2 \frac{R_2/(R_3+R_2)}{R_4/(R_4+R_5)} - v_1 \frac{R_5}{R_4} \quad (2)$$

From equation (1) and (2), it is indicated that with careful component selection, $v_e \propto i_{L1}$

Fig. 5 shows the SPICE simulation waveforms of current estimator under ZVS. During M1 and M2, the bridge rectifier is conducting and so the PT output is clamped to the load voltage v_L and, therefore, i_{Cout} and its derivative signal v_A are zero, while PT output current i_{out} and its scaled version v_B is dominated by the resonant current. In M3, the rectifier switches off and C_{out} is being charged, and so i_{Cout} and its scaled version v_A increase accordingly. v_A and v_B are combined to reconstruct the estimated current v_e, and are used to generate the feedback signal v_{ZC} for the PLL controller.

3.2. *ZVS PLL controller*

The PLL controller is implemented by a CMOS CD4046 to lock-on to the resonant current and generate in-phase gate signals to achieve ZVS. The CD4046 circuit contains a voltage-controlled oscillator (VCO) and a phase comparator and requires an external low-pass filter (LPF), as shown in Fig. 6. The operating frequency range of the VCO is controlled by an external timing capacitor and two timing resistors. The type II phase comparator of CD4046 is used to synchronise both phase and frequency of the input signals and generate an error signal for the LPF. In most PLL circuits, when locked the phase and frequency of VCO output should be matched to the input signal. In this application, however, a frequency divider is employed within the phase detector loop so that the VCO is actually locked to twice the resonant current frequency. With appropriate logic the f_{lock} (A) and $f_{lock/2}$ (B) signals allow a complete cycle to be divided into four equal sections of duration 90° or $\pi/2$ radians. The Boolean equations (3) and (4) show how the signals A and B may be decoded to provide the necessary gate drive to meet the critical criterion. Switching waveforms shown in Fig. 7 demonstrate successful operation of the PLL controller for achieving ZVS as resonant current is locked on and gate drive signals are phase- and frequency-matched to i_{L1}.

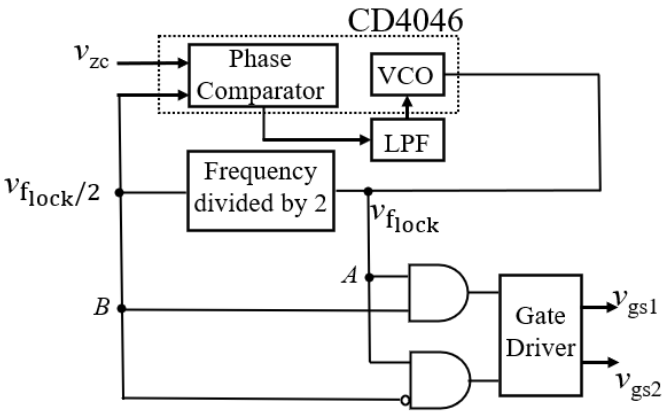


Fig. 6: Block diagram of the proposed ZVS PLL controller

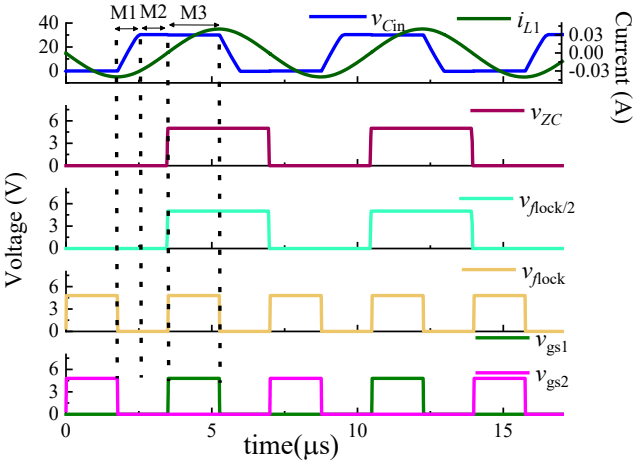


Fig. 7: Operating waveforms of ZVS PLL controller

$$v_{gs1} = A \cdot B \quad (3)$$

$$v_{gs2} = A \cdot \bar{B} \quad (4)$$

3.3. *Burst-mode control*

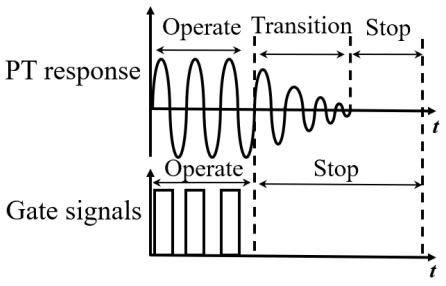


Fig. 8: Gate signals and PT response with burst mode modulation

To regulate the output voltage, the power supply operates in burst mode by controlling the on/off periods of MOSFETs according to regulation requirement. A typical PT response in burst-mode modulation is shown in Fig. 8. As can be seen, the

PT doesn't stop instantly when the switches are turned-off due to its mechanical vibration. Therefore, a transition period occurs and introduces a time delay in the control.

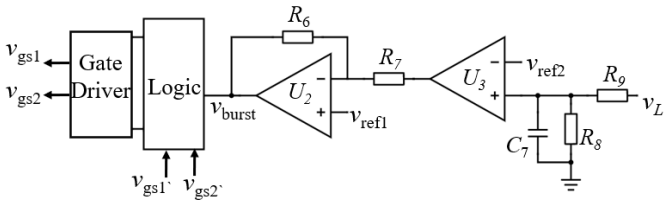


Fig. 9: Circuit diagram of burst-mode hysteresis operation

The burst-mode operation is accomplished by the hysteresis window through a burst signal v_{burst} to obtain a good converter dynamic response. The burst signal v_{burst} is generated from a hysteresis window with upper and lower voltage regulation limits. Thus, PT drive stops when v_L meet the upper limit and it starts to operate again at the lower boundary. As shown in Fig. 9, a Schmitt trigger comparator U_2 is used to implement the hysteresis window, and the window size is determined by R_6, R_7 and reference signal v_{ref1}. The output voltage v_L is adjusted and filtered before applied to the hysteresis comparator.

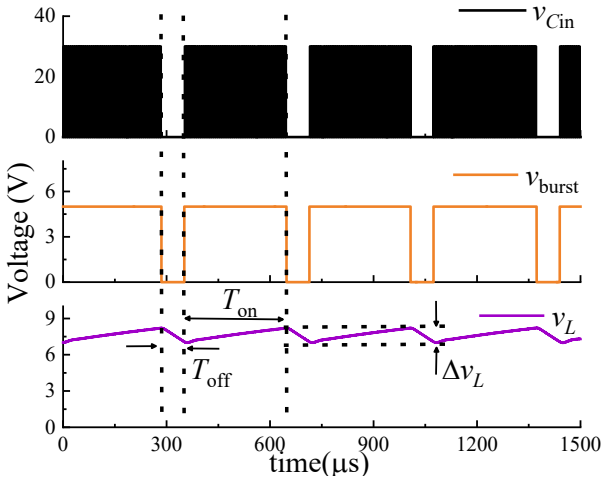


Fig. 10: Operating waveforms of the burst-mode control

Fig. 10 Shows the switching waveforms of the resonant converter under burst-mode operation. During burst mode operation, the piezoelectric transformer is considered to be a current source I_{piezo} that charges the filter capacitor C_f until v_L reaches the upper regulation limit and the load discharges C_f until v_L reaches the lower boundary. As can be seen from Fig. 10, Δv_L is the voltage ripple and is controlled by the on/off periods of the switches through hysteresis window. The on and off time of burst-mode operation are indicated as

$$T_{\text{on}} = \frac{C_f \Delta v_L}{I_{\text{piezo}} - I_L} \tag{5}$$

$$T_{\text{off}} = \frac{C_f \Delta v_L}{I_L} \tag{6}$$

where I_L is the load current. When PT operates continuously without burst mode modulation, I_{piezo} equals to I_L. Therefore, the burst frequency f_{burst} can be found from equation (5) and (6)

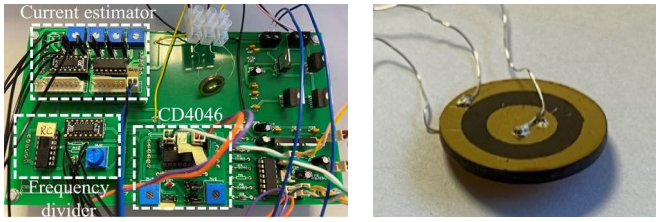
$$f_{\text{burst}} = \frac{(I_{\text{piezo}} - I_L) I_L}{C_f \Delta v_L I_{\text{piezo}}} \tag{7}$$

As can be seen from equation (7), for a given PT and filter capacitor, the voltage ripple Δv_L is inversely proportional to f_{burst}. Therefore, the burst frequency should be increased if a smaller Δv_L is required or a large value for C_f must be used.

4. Experimental results

To validate the proposed control method, a prototype half-bridge PT-based resonant converter is implemented and tested as shown in Fig. 11(a). A ring-dot radial-mode PT with a natural frequency of 140 kHz is used for the test, as shown in Fig. 11(b), with the extracted equivalent circuit component values given in table I.

The experimental waveforms of the proposed control circuit are shown in Fig. 12. To ensure adequate lock range with acceptable component tolerance, the PLL is restricted to operate between 270kHz to 290kHz (i.e. in the range of twice the resonant frequency of the PT). A 810 Ω load (corresponds to 1 kΩ matched load at PT output) is used to validate the proposed controller, since this is the worst operating condition for achieving ZVS.



(a) (b)

Fig. 11: Experimental set-up of the proposed control system. (a) prototype PT-based inductorless converter with proposed control circuit and (b) PT under test.

Table 1: PT equivalent circuit parameters

C_{in}	C_{out}	L_1	C_1	R_1	N	Q
0.43nF	1.14nF	17.2mH	77.8pF	12.5Ω	0.94	1190

As can be seen from Fig. 12(a), the phase comparator input signals v_{zc} and v_{flock} are frequency- and phase-matched, demonstrating a PLL locked-on condition. The resonant current is estimated by v_{A} and v_{B}, reconstructed as v_{e} and modified to v_{zc}, clearly indicating the zero crossings for ZVS operation. The gate drive signals are generated through steering logic with $\pi/2$ deadtime and align with the feedback signal v_{zc}. ZVS is clearly achievable since v_{Cin} reaches V_{dc} during the deadtime period.

Fig. 12(b) shows the circuit output voltage regulation performance. A 3kHz burst signal v_{burst} is set by the hysteresis window to achieve 7.5V output with 300mV voltage ripple. According to the experimental measurement, the transition time for PT starts and stops are 5 and 12 PT resonant periods, respectively. The transition times are measured between the burst signal switching instant and v_{Cin} reaches steady state.

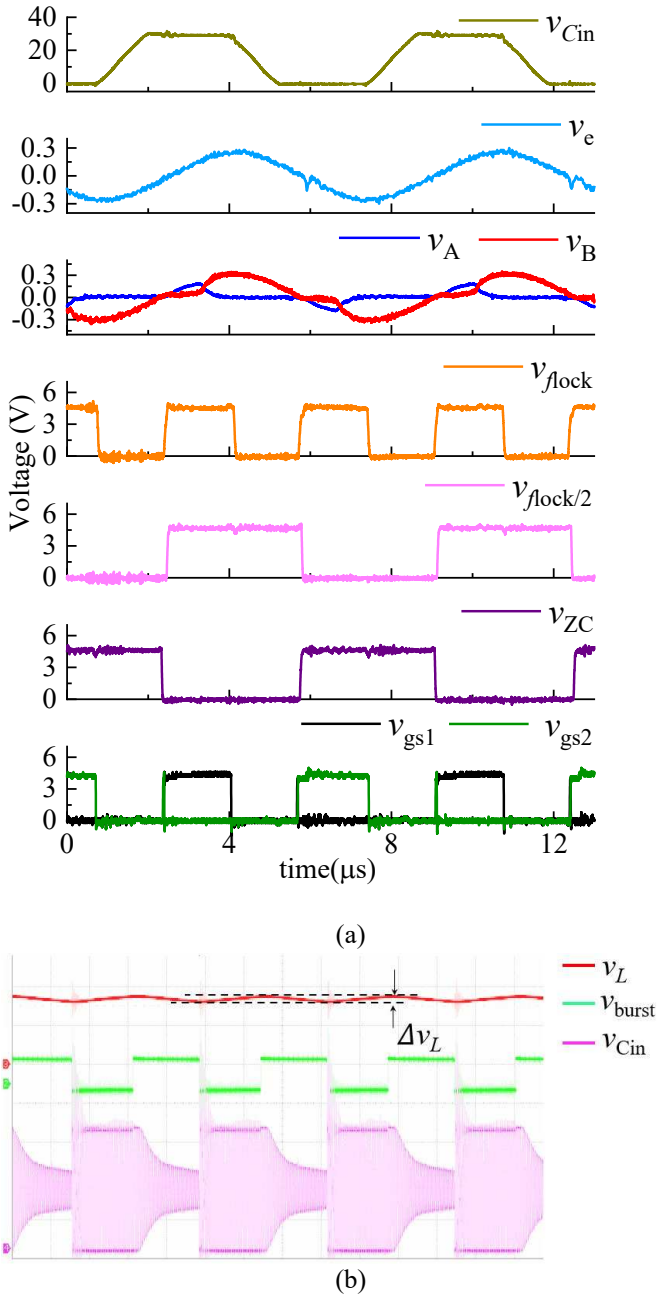


Fig. 12: Experimental measurements of the prototype converter and control circuit. (a) PLL controller associated with frequency divider under ZVS operation and (b) output voltage regulation by burst-mode hysteresis control at the matched load condition. (PT input capacitance voltage v_{Cin} 10V/div, burst signal v_{burst} 5V/div and output voltage v_L 5V/div).

5. Conclusion

Output voltage regulation and ZVS operation of a PT-based inductorless half-bridge converter is presented in this paper. A ring dot radial mode PT is used verify the proposed control circuit at matched load condition. A secondary-side resonant current estimator has been demonstrated to accurately reconstruct an unmeasurable signal and ZVS is achieved by using a PLL to lock onto this signal. Voltage regulation has been accomplished by burst mode control through a hysteresis window. The output voltage is restricted by the window size and the gate signals are modulated by the corresponding burst signal via PLL controller and logic circuit. Therefore, the MOSFETs are periodically switched on/off to satisfy regulation requirements.

6. References

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