**Monocrystalline silicon photovoltaic mitigation of potential-induced degradation using SiO2 thin film and +1000 V biasing**

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**Abstract**

Potential-induced degradation (PID) of photovoltaic (PV) modules is a severe form of degradation in PV modules, where power losses depend on the strength of the electric field, the relative humidity, and temperature. Therefore, understanding how PID influence the performance of PV modules is fundamental to reducing problems caused by such degradation. Previous studies have only considered single effects of PID; however, this work investigates the power losses and the development of hotspots in two different monocrystalline silicon PV modules. The origin of the hotpots is when the examined modules are being affected by severe PID, which results in cracks and materials deterioration. The first module is SiO2-free, and the second module contains this thin film layer. In addition, a PID mitigation procedure of +1000 V has been applied and its effect examined on the modules. The modules were examined under electroluminescence (EL) and thermal imaging. Following these PID experiments, it was found that the SiO2 layer is suitable for deploying commercial PV modules to prevent hotspots and PID. However, applying +1000 V PID mitigation does not necessarily improve the modules' performance after being affected by PID.

**Keywords:** Potential-induced degradation, photovoltaics degradation, electroluminescent imaging, performance analysis.

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1. **Introduction**

One of the many valuable factors of photovoltaic (PV) technology is its high stability, with potential operational lifetimes of over 25 years. Ongoing progress from industrial and academic researchers to advance PV efficiency and overcome manufacturing costs has contributed immensely to PV’s advancement. In the wake of the accelerated germination of the PV industry, solar cell’s reliability has recently caught significant attention from researchers, manufacturers, and investors. Although it is believed that PV modules are reliable under field conditions with low degradation and failure rates, recent studies have shown that they are likely to be influenced by diverse degradation mechanisms, which collectively reduce the PV output power over time. One of the critical degradation mechanisms is potential-induced-degradation (PID) [1-3]. The PID occurs due to the high voltage between the front surface/glass of the PV module and the encapsulation, which is typically grounded using the module frame or substructure [4].

PID becomes more prevailing when the PV modules age, and whilst it usually does not impact all the solar cells in the module, the PID contributes can have significant consequences as it cannot be repaired [5]. For example, in recent studies [1, 6], PV modules with different types of structure (poly/monocrystalline silicon) were subjected to PID stresses under the IEC61215 standard [7]. As a result, they show 8-30% power losses under standard test conditions. Nevertheless, these studies did not consider evaluating the effect of varying the solar irradiance on the performance of the PID modules or analyzing the thermal behaviour of the affected PID modules.

Other experimenters [8, 9] have shown that cracks in solar cells can accelerate PID due to the localized heat. This phenomenon happens when a crack is initiated in the cell; thus, nonuniform distribution of the current in the fingers and busbars transpires. Accordingly, localized heating has been developed, commonly known as hotspots. In contrast, there are undersized details on the correlation between PID and the development of hotspots. From research papers such as [10, 11], it is suggested that hotspots are likely to occur in PV installation. Yet, there is no complete understanding of whether PV modules impacted by PID have hotspots and the potential increase in their surface temperature.

Other types of PV failure, including failure in the bypass diodes [12], permanent shading [13], or shunting [14], are recognised not to accelerate PID. In practice, these failure modes are usually mitigated by utilising state-of-the-art power electronics devices.

Electroluminescence (EL) imaging is usually performed [15-18] to inspect the PID effect on PV modules. For example, in Figure 1, the EL image is shown for two different solar cells before and after the PID experiment was completed. The darker exhibition of the cells under EL testing corresponds to less efficiency, with an estimated power loss of -17% and -22%, respectively. However, other researchers [19-23] have proposed using photoluminescence (PL) imaging to consider the effects of PID on cells. PL imaging is more practical for inspecting large-scale PV modules. However, PL imaging cannot determinate inactive areas in the cells, and the interconnection failure, whereas an EL imaging setup can identify both failure modes [24].

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Figure 1. EL images were taken before and after the PID test, the EL images were captured using Brightspot EL imaging setup, and the power loss (Ploss) was estimated under STC conditions.

This paper presents the results of testing two monocrystalline silicon modules. The first module is SiO2-free, and the second module includes the SiO2 thin film layer deposited on the top surface of the glass substrate. Both modules were newly fabricated at the initial stage of the experiment, and no PID was detected; then, following the IEC62804 standard, both modules were subjected to PID. The considered investigations are different from those already presented in the literature because, in this paper, the analysis incorporates (i) the output power losses under varying solar irradiance, (ii) thermal behaviour and hotspots development, and (iii) performance of the PV modules after performing a PID mitigation procedure by applying +1000 V biasing. These results lead to understanding how PID can severely impact the performance of PV modules and, in contrast, whether SiO2 can mitigate this event. In addition, the correlation between PID and hotspots will help explain why some aged modules are affected by hotspots.

The rest of the paper is structured as follows: Section 2 provides details of the proposed methods used in this work. Section 3 presents result from experiments performed and an informed discussion leading from these results. In addition, Section 4 offers a comparative evaluation of the results presented in this paper against those recently published in the literature. Finally, the article finishes with conclusions in Section 4.

1. **Methods**

For experimental work presented in this paper, two flexible PV modules, p-type monocrystalline silicon were tested. The second PV module includes the SiO2 layer which have 5 µm thickness deposited on the top surface of the glass substrate (Figure. 2(a)), therefore, there is a marginal drop (0.28±0.3 W) in its output power compared with the first PV module that do not include the same thin film layer. Both modules are newly manufactured, and their electrical parameters are presented in Table 1, taken at standard test conditions (STC), where the solar irradiance is 1000 W/m2, and PV cell temperature is 25°C. The electrical parameters were averaged over five cycles to ensure the readings' stability. This has been done using the PVA-1500V3 PV analyzer; the instrument output current measurements accuracy is ±40 mA, and the output voltage accuracy of ±0.25 V. The measurements calibration/sweep time is 250 ms, and the maximum PV voltage and current is 1500 V and 30 A, respectively.

The modules were placed in a damp heat test chamber (Figure. 2(b)) at 80% relative humidity and 85°C and biased with a voltage of -1000 V. The positive and negative module contacts were shorted and connected to the negative terminal of a high-voltage power source. Following the IEC62804 standard, the EL images and current-voltage (I-V) curves were measured at 0, 48, 96 hours. The BrightSpot Automation EL imaging setup (Figure. 2(c)) was used to capture the EL images of the PV modules.

Table 1 Parameters of the tested PV modules at STC conditions.

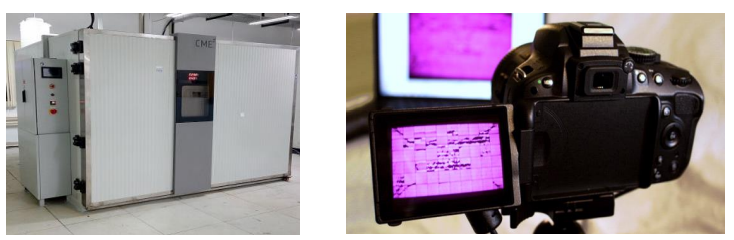
|  |  |  |
| --- | --- | --- |
| Parameter | Value (PV #1) | Value (PV #2) |
| Power at maximum power point () | 100±0.3 W | 99.72±0.3 W |
| Current at maximum power point () | 5.56±0.04 A | 5.54±0.04 A |
| Voltage at maximum power point () | 18±0.25 V | 18±0.25 V |
| Short circuit current () | 6.06±0.04 A | 6.06±0.04 A |
| Open circuit voltage () | 21.6±0.25 V | 21.6±0.25 V |
| Number of cells | 36 | 36 |
| Dimension | 1200×550×2 mm | 1200×550×2 mm |
| SiO2 thin film | Not included | Included |

This study performed the EL imaging while biasing the PV modules at a short circuit current () to give the optimum image resolution. Likewise, thermal images of the modules were taken at the same condition using FLIR E54 thermal camera with thermal sensitivity of ±0.1°C. This procedure would help identify the correlation between hotspots and PID affecting the modules by comparing the EL and the thermal images at an identical operational state. The relative power loss due to PID is then calculated as,

(1)

where is the module maximum output power at the end of the PID testing, whereas is the module initial maximum output power.

Graphical user interface

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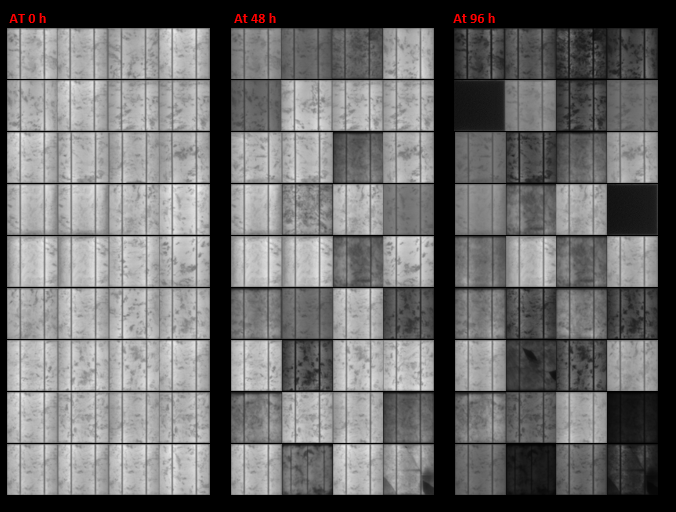
1. (b) (c)

Figure 2. (a) Cross-section scanning electron microscope photograph of the solar cell samples with SiO2 coating, (b) Damp heat test chamber, (c) EL imaging camera.

1. **Results and Discussions**
   1. **PID Testing and PV Module Thermal Cycle**

The PID test was performed on the two tested PV modules described in the previous section, following the IEC 62804. Considering Figure 3(a), the first examined PV module, at 0 h, there were no cracks, damages, or blackout regions in the solar cells. In contrast, as time progresses, the module exhibits more extended blackout cells corresponding to PID. For example, at the end of the PID experiment, at 96 h, the module had approximately 20 cells affected by severe PID conditions. In contrast, in the second PV module, which is coated with a SiO2 thin film layer, it can be observed that only minor effects of the PID test on the cells during the first 48 hours (Figure 3(b)). However, at the end of the PID test, 96 h, the PV module has been affected across eight cells that manifest severe PID shapes.

From these results it can be concluded that PID is less likely to affect a PV module coated with a SiO2 thin film layer. This is because this layer has low reflectance and high transmittance, and it can prevent the Na particles from passing into the depletion layer [25]. Therefore, it can prevent, or in better explanation, it can serve as a pure resistance against the PID. In addition, Figure 3(a) shows that the PID started to affect the cells after 48 hours; these results also suggest that the SiO2 layer delays the impact of the PID. Compared with Figure 3(b), the module without the SiO2 layer, PID affected the cells as soon as the PID test started.



(a)



(b)

Figure 3. EL images of the examined PV modules during PID test at 0, 48, and 96 h. (a) First PV module, (b) Second PV module.

After the PID test was completed, the power losses of both modules under varying solar irradiance while the temperature was maintained at 25°C was measured; the results are shown in Figure 4. It can be concluded from Figure 4 that the first PV module has a significant drop in the output power compared with the second PV module.

The first PV module, the power loss at a high irradiance level (above 750 W/m2) is varied between 8% to 20%. However, at a low irradiance level (below 200 W/m2), the module's average power loss is 45%. This is because the shunt resistance increases while decreasing the irradiance [26, 27].

In contrast, in the second PV module, which includes the SiO2 layer, the average power loss of 5% is relatively stable over the irradiance spectrum (300 W/m2 and above). However, at low irradiance conditions (below 300 W/m2), the average power losses increased to nearly 10%. Again, this is due to the increase in the shunt resistance in the cells.

These observations lead to understanding that the previously EL images (Figure 3) evidence an accurate representation of the impact of PID. Significant power loss in the first module compared with the second is observed, strongly correlating with the number of cells that have been affected by the severe PID. In addition, from Figure 4 it can be observed that almost all measured power losses for the first PV module are below the baseline 10%; the opposite conclusion is found to be true for the second PV module.

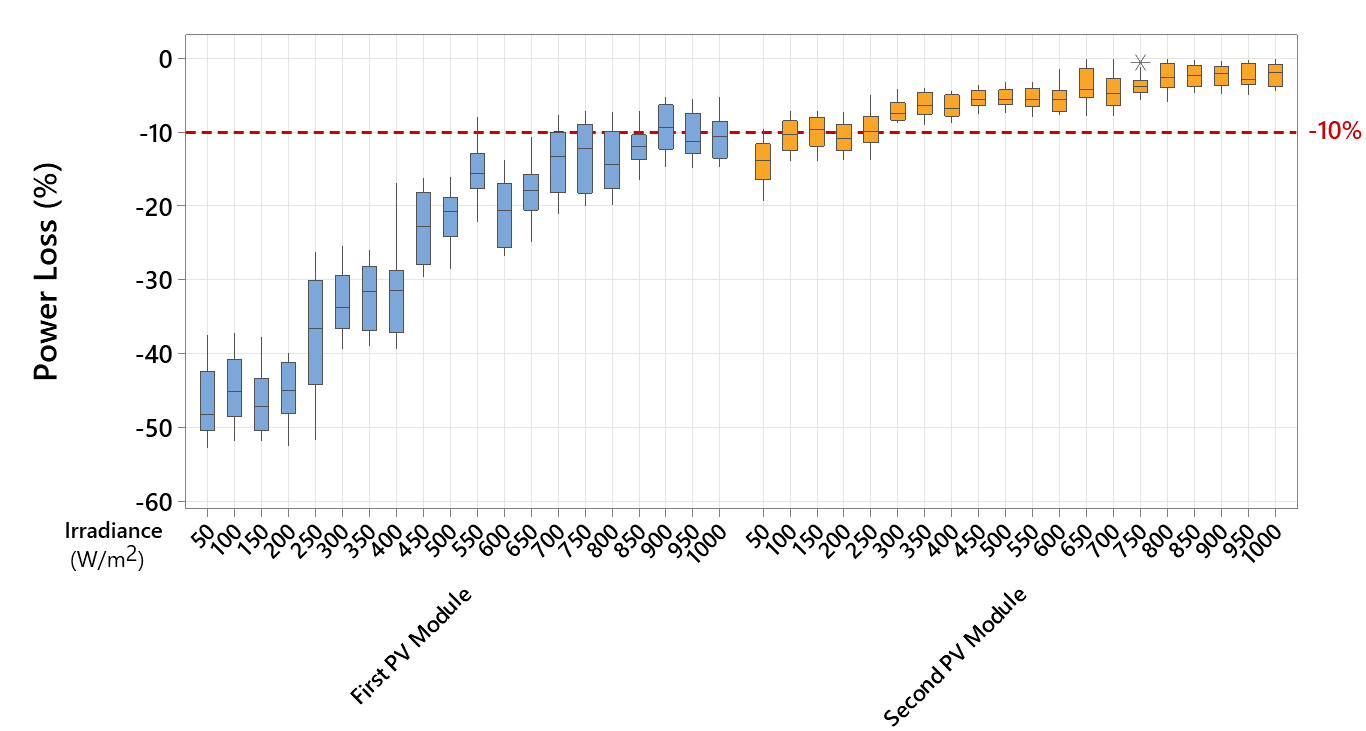
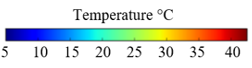


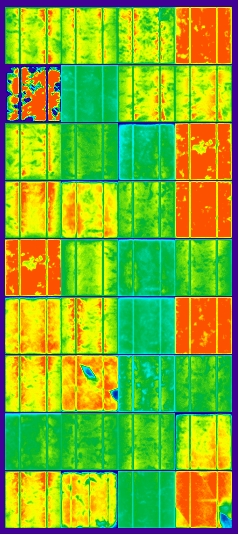
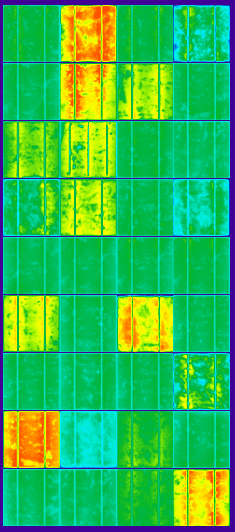
Figure 4. The power loss of the tested PV modules after the PID test was completed under varying solar irradiance levels.

Next, the thermal impact of the PID on both examined PV modules is investigated. Consider the thermal images in Figure 5. The test was performed while solar irradiance is 1000 W/m2, and solar cell surface temperature is 25°C.

In the first PV module, Figure 5(a), nearly 16 cells developed a hotspot, with an approximate increase in their temperature from 25°C to 45°C. In contrast, in the second PV module, Figure 5(b), only 6 cells had an increase in their temperature. There is almost (only 1) no development of a complete enclosure of a hotspot, where the cell's entire surface is affected by the same increase in temperature.

This result confirms that SiO2 layer can improve the overall performance of the PV module when affected by PID. Nevertheless, hotspots and power loss are likely the occur even when SiO2 is coated in the module.



(a) (b)

Figure 5. Thermal images of the examined PV modules were taken under STC conditions. (a) First PV module, (b) Second PV module.

* 1. **PID Mitigation Testing**

Previous research, such as [31, 32], demonstrate that the PID can be mitigated when applying +1000 V on the terminals of the affected PV modules. This is possible if the modules are recently affected by PID, where severe PID is not prominent. This condition can be applied in the experiments reported in this paper because both tested modules are newly manufactured, and the PID test has been executed for only one cycle to avoid severe PID or breakdown in the solar cells.

The actual schematics diagram of the PID mitigation test schematic is shown in Figure 6(a). First, the PV module leads/connectors are shortened and connected to a high-voltage power source (0 V, negative terminal). Next, the module frame is connected to the positive terminal, +1000 V, and the actual setup of the test with a PV module is shown in Figure 6(b). This is typically the reversed schematics of inducing a PID to a PV module, where the PV connectors are supported to be connected with +1000 V, and the frame is grounded.

Diagram

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(a)

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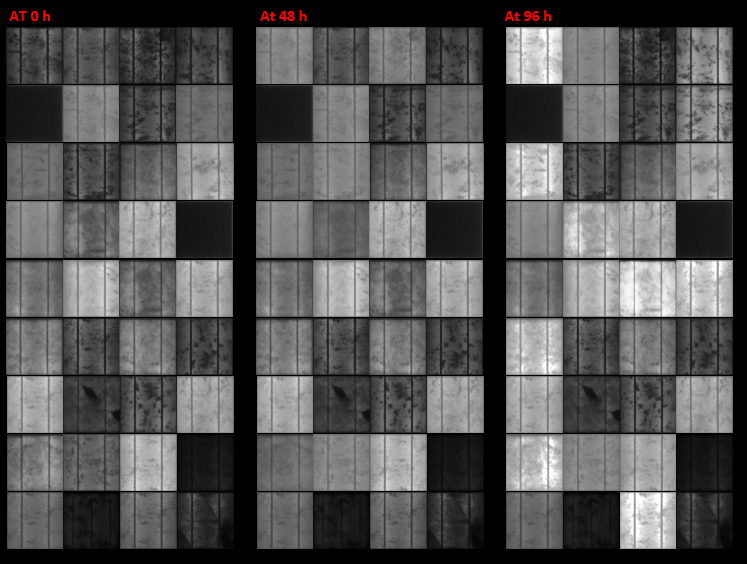
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(b)

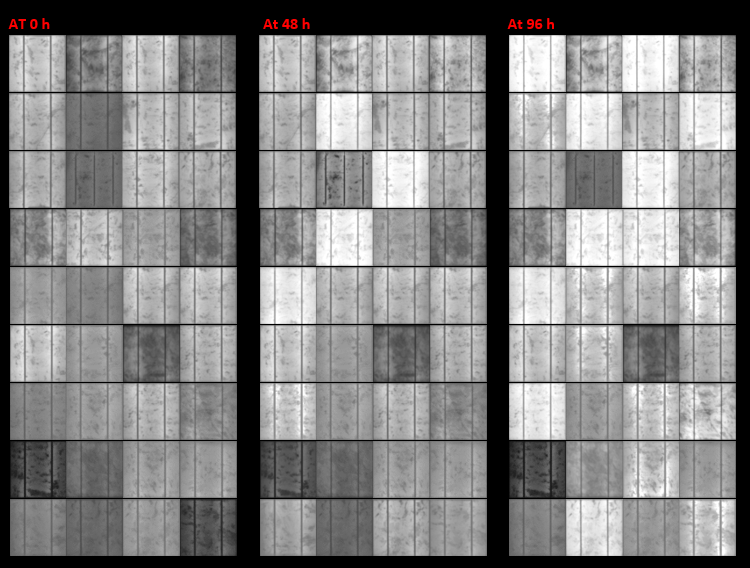
Figure 6. (a) Schematic diagram of the PID mitigation test. (b) Actual connection with a PV module.

Following the IEC 62804, EL images are captured at 0, 48 and 96 hours, as shown in Figure 7. The first PV module (Figure 7(a)) still exhibited a severe PID even when PID mitigation was performed. In addition, the PID mitigation for the second PV module appears to be more efficient. As can be observed in Figure 7(b), there is a suitable transformation of the light exhibited in the PID affected cells as time advances (the images of the cells are brighter).

This result suggests that SiO2 layer protects PV modules from being affected by severe PID and can help improve the recombination’s of the carries (electroluminescence) when a PID mitigation test is conducted.



(a)



(b)

Figure 7. EL images of the examined PV modules during the PID mitigation test at 0, 48, and 96 h. (a) First PV module, (b) Second PV module.

For both PV modules, after the PID mitigation was completed, they were placed back in the damp heat test chamber. The output power losses at varying irradiance are presented in Figure 8; here, the temperature was fixed at 25°C. There is a notable decrease in the output power losses for both PV modules. According to the first PV module, the power has not been significantly improved at high and medium irradiance conditions. However, under low irradiance conditions (<200 W/m2), the module's average power loss is 30%, compared with 45% before the PID mitigation.

Remarkably, all measured power loss from the second PV module are below the baseline of 10%, confirming that utilizing +1000 V biasing to the module with SiO2 thin film layer has a conspicuous impact on mitigating possible PID affected cells.

Additionally, the PID mitigation procedure has impacted both modules in terms of the restoration from hotspots. As presented in Figure 9, the first PV module is now only affected by eight hotspots, compared with 16 before the PID mitigation. The second PV module has no hotspots; there is a slight increase in the temperature of some parts of three different solar cells, but this cannot be classified as complete hotspots. These events confirm that applying +1000 V as a PID mitigation is worthwhile for any already PID affected modules.

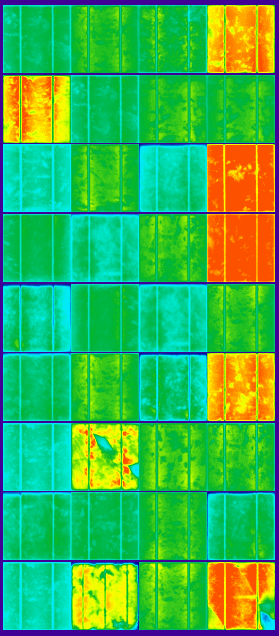
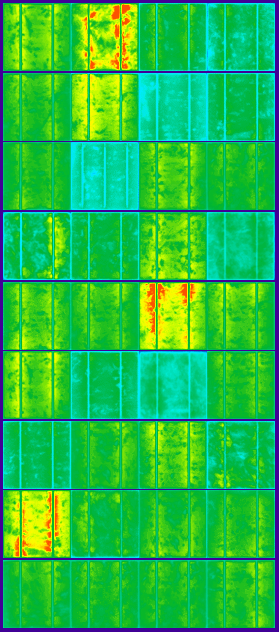


Figure 8. Power loss of the tested PV modules after the mitigation PID test was completed under varying solar irradiance levels.

* 1. **Results Summary**

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(a) (b)

Figure 9. Thermal images of the examined PV modules were taken under STC conditions after the PID mitigation test was completed. (a) First PV module, (b) Second PV module.

In Table 2, summarize all the results presented in this paper. The results We demonstrate that for the first PV module, SiO2-free, the PID experiment had a severe impact on its performance. Even when applying the PID mitigation procedure, the power loss varied from 8% to 30%. In addition, a considerable decrease in the number of hotspots occurred, from 16 to 8; nevertheless, eight hotspots can still critically impact the thermal cycle of the module. The second PV module, including the SiO2 layer, has a marginal power loss (2% to 7%), and there were no outstanding hotspots after the PID mitigation was completed. This result suggests that the SiO2 layer is suitable for integrating with commercial PV modules to prevent hotspots and PID.

An additional compelling outcome was found while performing the PID experiment, that the first PV module developed three cells with partial breakdown areas, as shown in Figure 10. These breakdown regions cannot be fixed even if PID mitigation is planned [28]. In comparison, this effect of the PID was not observed on any of the cells in the second tested PV module.

Table 2 Comparative study of all obtained results

|  |  |  |  |  |
| --- | --- | --- | --- | --- |
|  | PV #1 before PID | PV #1 after PID mitigation | PV #2 before PID | PV #2 after PID mitigation |
| Average Power Loss at High Irradiance Levels (>750 W/m2) | 10±1.8% W | 8±1.2% W | 3±0.3% W | 2±0.3% W |
| Average Power Loss at Medium Irradiance Levels (750≥G≥250 W/m2) | 27±2.9% W | 18±2.6% W | 5±0.3% W | 4±0.3% W |
| Average Power Loss at Low Irradiance Levels (<250 W/m2) | 45±3.5% W | 30±3.1% W | 10±0.5% W | 7±0.5% W |
| Number of Developed Hotspots | 16 | 8 | 1 | 0 |

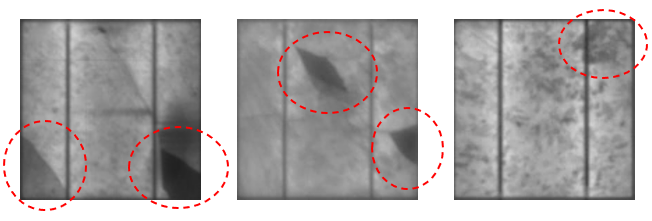


Figure 10. Observed backdown areas in the first PV module after the PID experiment was completed.

The current-voltage (I-V), and power-voltage (P-V) curves for both tested PV modules after completing 96 hours of PID stress and after the PID mitigation were analysed. The tests were carried out under STC conditions, and the PVA-1500V3 PV analyzer took the measurements.

The I-V and P-V curves for the module after the PID stress was completed is presented in Figure 11(a). There is no significant difference in the because the bypass diodes in the modules allow an alternative current path to the strings that the PID impacts. However, the for the first module dropped by 2.1 V compared with the second module; this also results in a considerable difference (13.93 W) in the , 81.8 W and 95.7 W for the first and second module, respectively.

Figure 11(b) shows that the PID mitigation moderately improved the for both modules, 97.8 W and 90.5 W for the first and second modules, respectively. Yet the first module has still a reduction in the , approximately 0.8 V which cannot be fully recovered. This result suggests that when employing +1000 V for PID affected modules, it is expected to improve the output power. Nevertheless, this mitigation procedure cannot entirely recover the PID effect.

Chart, line chart, scatter chart

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(a)

Chart, line chart, scatter chart

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(b)

Figure 11. I-V and P-V curves of the tested PV modules under STC conditions. (a) After PID stress of 96 hours, (b) After PID mitigation.

1. **Comparative Evaluation**

To establish the new findings of this work, the results illustrated in this article have been compared with recently published work, including [29-32]. The summary of the comparative evaluation is presented in Table 3.

All former work has used EL imaging to observe PID. However, only this work and [31, 32] use a thermal inspection to demonstrate further how PID can affect the temperature of the affected PID solar cells. Furthermore, the power loss analysis is usually measured at specific environmental conditions, generally at STC conditions [29, 31], or calculated over a long-term period [30]. In comparison, this investigation not only considered the power loss at STC condition and IV curve, but also, how the power loss increases as the irradiance level reduce due to increased shunt resistance in the PV modules has been presented.

According to [31, 32], they have identified the locations of the hotspots of the PV modules affected by PID. However, they have not been discussed thoroughly by comparing the surface temperature of the hotspots solar cells before and after applying the PID mitigation. In this article, it is illustrated that using +1000 V for PID mitigation can result in a 50% reduction in the number of hotspots. It is also highlighted in this work that almost no hotspots developed for the module contained the SiO2 thin film layer.

To date, there are two prominent techniques to mitigate the effect of PID on PV modules. The first technique, which is the most popular, is to apply +1000 V on the terminals of the PV module so that acting as reverse PID. The second approach is to manufacture the PV modules with dielectric films such as SiO2; the SiO2 can be deposited on the inside surface cover glass or the cell front surface or inserted between n+ emitters and SiNx antireflection layers. For example, in [31, 32], the first technique enabled PID mitigation. In contrast, in this paper, both methods have been used and the differences in power losses, hotspots development are investigated, and it is shown that when the SiO2 is deposited on the top surface of the glass substrate yields better PV performance compared with the mitigation using +1000 V biasing.

Table 3 Comparative evaluation of the results obtained in this article and the one presented in [29-32].

|  |  |  |  |  |  |
| --- | --- | --- | --- | --- | --- |
| Ref. | Year of the study | Technique used to detect PID | Power loss investigation | PV hotspots investigation | Technique used to mitigate PID |
| [29] | 2020 | EL image after 96 hours of PID stress | The power dropped from 12.6% to 18.7% | n/a | n/a |
| [30] | 2020 | EL images were obtained in 2014 and 2018 | The degradation rate was approximately 0.5%/year | n/a | n/a |
| [31] | 2021 | EL and thermal image after 75 and 150 hours of PID stress | Average loss in the power is about 79% after 72 hours of PID stress | Identified by the thermal image but not thoroughly discussed | PID recovery applying +1000 V |
| [32] | 2021 | EL image after 96 hours of PID stress | The power dropped from 15% to 35% | Several hotspots were identified, but no clear link between PID and hotspots development | Automatic night period PID recovery board using +1000 V |
| This paper | 2022 | EL and thermal image after 96 hours of PID stress | Power loss dropped from 10% to 50%, but considering varying the solar irradiance from 50 to 1000 W/m2 | Hotspots were identified and compared with the EL images. The hotspots were also investigated after PID recovery was applied. | (i) Applying +1000 V  (ii) SiO2 layer deposited on the top surface of the glass substrate |

1. **Conclusions**

In conclusion, this work reports the effect of PID on the performance of monocrystalline silicon PV modules. First, the PID test are applied on two modules, including a SiO2-free module and the second containing SiO2 coating deposited on the top surface of the glass substrate. Initially, it was discovered that after 96 hours of PID stress, the averaged power loss of the first PV module is approximately 30% across all irradiance levels, while the second has only 5% power losses. Next, a PID mitigation was applied by utilizing +1000 V biasing on both modules and found that the power loss varies from 8%-30% and 2%-7% for the first and second modules, respectively. In addition, it was found that even after the PID mitigation, 25% of the cells are impacted by hotspots in the first module, while the second module has no hotspot solar cells. These findings imply that the SiO2 layer is suitable for integrating with commercial PV modules to prevent hotspots and PID. Consequently, utilizing +1000 V as a recovery for PID is a practical solution for monocrystalline silicon-based modules.

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**Data availability:** The dataset generated and analysed in this study may be available from the corresponding author (M.D.) on reasonable request.

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