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Reducing the Computational Complexity of Wide-Area Backup Protection in Power Systems

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***Abstract*—Wide-area backup protection (WABP) refers to the identification of the faulted line amongst candidate lines by using sparse PMU measurements. This letter proposes a technique for reducing the computational complexity of WABP methods that employ the superimposed-circuit concept. A proposition is presented and proved to justify that the system of equations pertaining to every candidate line can be directly obtained from the bus impedance matrix of the pre-fault power system. This is in contrast with existing WABP methods requiring the establishment of as many distinct bus impedance matrices as the number of candidate lines in the power system. The applicability and effectiveness of the proposed technique are verified by conducting more than 20,000 simulations on the IEEE 39-bus test system.**

***Index Terms*—Bus impedance matrix, nodal injections, superimposed circuit, wide area backup protection (WABP).**

I. Introduction

INADEQUACY of local data in providing a holistic picture of the system state along with measurement inaccuracies due to transient responses of instrument transformers are root causes of local protection failures [1]. The proliferation of phasor measurement units (PMUs) has paved the way for wide-area backup protection (WABP) as a complementary means for addressing shortcomings of local protections [2]. This enhances the protection system's reliability, thus facilitating the operation of the power system against faults.

A prerequisite for applying superimposed-based WABP methods is that the pre-fault and post-fault circuits have the same bus impedance matrix [2-4]. This can easily be realized by removing the faulted line from the circuit and replacing it by suitable current sources before and after the fault onset. To identify the faulted line, the replacement procedure is carried out for all candidate lines. A system of equations is derived for each case relating the measurements to the candidate line under study. The sum of squared residuals (*SoSR*) is calculated for the developed system of equations. The candidate line with the least *SoSR* is identified as the faulted line [2-4].

If l denotes the number of lines in a power system, WABP methods introduced in [2-4] require the calculation of l distinct bus impedance matrices upon any changes in the power system's topology/operating point. Given the dynamic nature of power systems, this translates to a continuous need for calculating and updating of l coefficient matrices, which can be highly demanding for large-scale power systems.

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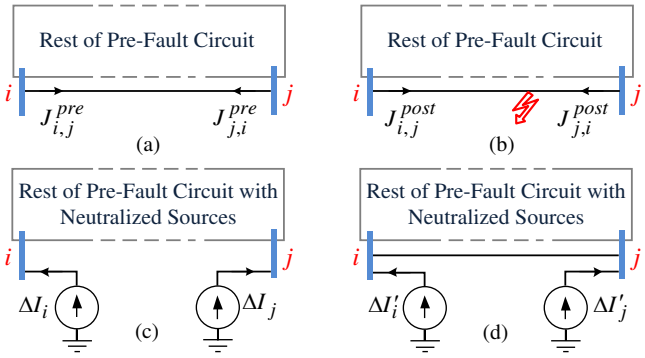

Fig. 1. (a) Pre-fault circuit. (b) Post-fault circuit. (c) Superimposed circuit with line *i-j* removed. (c) Superimposed circuit with line *i-j* connected.

This letter asserts that the coefficient matrix corresponding to every candidate line can be directly calculated from the bus impedance matrix of the pre-fault power system, irrespective of the faulted line, fault type, and fault location. A proposition is presented with analytical proof justifying the validity of the proposed technique. This removes the need for numerous modifications of the bus impedance matrix w.r.t the candidate lines under study. Extensive simulations are conducted to confirm that the proposed technique reduces the computational burden without impacting the success rate of WABP.

II. WABP Based on the Superimposed Circuit Concept

Let us assume line *i-j* in a power system is faulted. Figs 1(a) and 1(b) show the pre-fault and post-fault circuits of this power system with N buses. The differences between the voltage and current phasors following the fault can be attributed to the corresponding voltages and currents in the superimposed circuit shown in Fig. 1(c). The topology of the superimposed circuit is independent of the fault location on the line, yet different from that of the pre-fault circuit as line *i-j* is excluded from the former. Let ΔI_i and ΔI_j refer to the superimposed nodal injections at buses i and j, respectively, as the only non-zero injections in the superimposed circuit of Fig. 1(c). Thus, the superimposed voltage at an arbitrary bus q can be obtained from

$$\Delta V_q = Z_{qi}\Delta I_i + Z_{qj}\Delta I_j \tag{1}$$

where Z_{qi} is the entry in the q-th row and i-th column of the bus impedance matrix. Let ΔJ_{uw} denote the sending-end superimposed current of line *u-w*. It can be easily shown that

$$\Delta J_{uw} = C_{uw,i}\Delta I_i + C_{uw,j}\Delta I_j \tag{2}$$

where the derivation of $C_{uw,k}$ is detailed in [3]. Every voltage and current measurements provided by PMUs can be

substituted in (1) and (2), respectively, to form an equation in ΔI_i and ΔI_j. These equations together form an overdetermined system of equations as below

$$\boldsymbol{m} = \boldsymbol{H}\begin{bmatrix}\Delta I_i \\ \Delta I_j\end{bmatrix} + \boldsymbol{\varepsilon} \tag{3}$$

where $\boldsymbol{m}$ and $\boldsymbol{H}$ are the measurement vector and the coefficient matrix [4]. The vector $\boldsymbol{\varepsilon}$ also stands for measurement errors.

The residuals of a system of equations are defined as the discrepancy between the measured quantities and their corresponding estimations [5]. The sum of squared residuals for (3) can be calculated from the closed-form solution below

$$SoSR = \boldsymbol{m}^*\boldsymbol{S}^*\boldsymbol{S}\boldsymbol{m} \tag{4}$$

where $\boldsymbol{S} = (\boldsymbol{I} - (\boldsymbol{H}^*\boldsymbol{R^{-1}}\boldsymbol{H})^{-1}\boldsymbol{H}^*\boldsymbol{R^{-1}})$ [5]. The asterisk refers to the conjugate transpose of the matrix/vector. Besides, $\boldsymbol{R}$ and $\boldsymbol{I}$ denote the covariance matrix of measurement errors and the identity matrix of appropriate size, respectively.

To form (3), it is assumed that line *i-j* is the faulted line; a hypothesis whose truth is unknown upon receiving PMU data. Nonetheless, if this hypothesis is true, the *SoSR* corresponding to (3) will be quite negligible (ideally zero if measurements were error-free). This feature has been employed in several research works to identify the faulted line [2-4]. In doing so, (3) is built for every candidate line and (4) is calculated for each. The line corresponding to the smallest *SoSR* is identified as the faulted line. It is worth noting that (3) remains functional even if the faulted line is a double-circuit line. The reason is that the whole faulted line can still be modelled by proper current sources from the viewpoint of the remainder of the power system. As a result, the *SoSR* index can still pinpoint the faulted line regardless of whether it is single- or double-circuit. However, a PMU at one of the faulted line terminals is necessary if we are to determine which of the two circuits is faulted [6].

III. Reducing Computational Complexity

To determine which candidate line is faulted, (3) is built for every candidate line to obtain the associated *SoSR* [3]. This requires the removal of the candidate line from the pre-fault circuit to calculate the entities of the corresponding coefficient matrix $\boldsymbol{H}$. If there are l candidate lines in the system, $\boldsymbol{H}$ must be obtained for l different circuits that differ from one another in the presence/absence of the candidate line. This letter asserts that $\boldsymbol{H}$ can be directly built from the pre-fault circuit for all candidate lines, with no modifications w.r.t the candidate line under study. The argument follows from the proposition below (proof in Appendix A):

Proposition: *Consider the response of the circuit of Fig. 1(c) for given nodal injections ΔI_i and ΔI_j at buses i and j, respectively. There are unique injections $\Delta I_i'$ and $\Delta I_j'$ that produce the same response in the circuit of Fig. 1(d) if applied respectively at buses i and j of that circuit.*

The converse of the above proposition is also true. For any response in the circuit of Fig. 1(d) resulting from non-zero injections $\Delta I_i'$ and $\Delta I_j'$, there are unique ΔI_i and ΔI_j that will produce the same response in the circuit of Fig. 1(c).

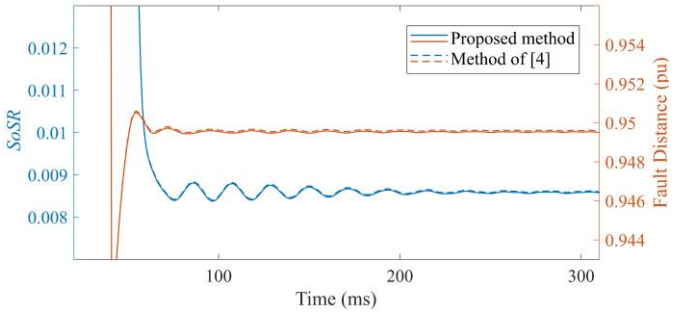

Fig. 2. *SoSR* and estimated fault distance using different methods.

TABLE I
COMPARISON BETWEEN DIFFERENT WABP METHODS

Error Type		Measurement Error			Line Parameter Error		
Error Range (%)		±0	±4	±8	±0	±4	±8
FLISR (%)	Proposed	99.88	99.03	98.49	99.88	97.29	94.22
	[3]	99.93	99.15	98.47	99.93	97.59	93.75
	[4]	99.43	99.26	98.83	99.43	97.73	92.92
AFLE (%)	Proposed	0.63	0.96	1.21	0.63	1.41	2.11
	[3]	0.65	1.00	1.11	0.65	1.11	2.01
	[4]	0.67	1.01	1.48	0.67	1.02	3.23

It can be concluded from the above proposition and its converse that any response that can be achieved for either of the two circuits is achievable for the other one. A conditional statement that follows from this is that if the *SoSR* for the circuit of Fig. 1(c) is zero, the *SoSR* for the circuit of Fig. 1(d) will be zero, as well. The converse of this conditional statement is also true. The reason is that the *SoSR* being zero means the observed measurements could be the response of the superimposed circuit for which (3) has been built [4]. Therefore, we assert that building $\boldsymbol{H}$ based upon the pre-fault circuit can reduce the computational complexity while maintaining the capability of indicating the faulted line.

IV. Performance Evaluation

The performance of the proposed technique is evaluated by conducting extensive simulations on the IEEE 39-bus test system. Buses 3, 5, 8, 11, 14, 16, 19, 23, 25, 27, 29 and 39 are equipped with PMUs. The real PMU model of [7] is used to extract the phasors of generated time-domain waveforms in PowerFactory following a wide variety of short-circuit faults.

To validate the capability of the proposed technique in identifying the faulted line, an arbitrary 1-ph-g fault at 95% of line 17-18 is investigated for up to 300 ms following the fault onset. The fault distance is also estimated using the closed-form solution proposed in [4] by obtaining the superimposed currents and voltages of the faulted line from (3), (A2), and (A3). Fig. 2 shows the *SoSRs* calculated for the faulted line, and the fault distance estimation using the proposed technique and the method proposed in [4]. As expected, the *SoSRs* calculated by both methods are quite similar with a difference in the order of 10^{-6}, which correctly identify the faulted line. The estimated fault distance on the line is practically the same.

Now, the general performance of the proposed technique is examined and compared with that of other methods for various fault types and locations on every line. To compare the sensitivity of WABP methods to measurement and parameter

TABLE II
SENSITIVITY OF THE PROPOSED METHOD TO FAULT RESISTANCE

Fault Resistance	0 Ω	5 Ω	10 Ω	15 Ω	25 Ω
FLISR (%)	99.88	99.82	99.63	99.47	99.34
AFLE (%)	0.63	0.65	0.67	0.71	0.74

errors, these quantities are assumed to have errors with normal distribution with mean zero. Measurement errors account for different sources of errors such as instrument transformers error, phasor estimation, and measurement noises [8]. The error ranges are reported based upon the three-sigma criterion [4]. Table I summarizes the results obtained from 20,000 simulated cases, in terms of faulted-line identification success rate (FLISR) and average fault location error (AFLE). Table II shows the method's performance for different fault resistances. The minor difference in *SoSR*s and estimated nodal currents in the presence of parameter/measurement error and different fault resistances do not noticeably affect WABP's success rate nor the accuracy of fault location.

The computational burden of WABP by the methods investigated can be divided into two parts, namely building $\boldsymbol{H}$ and (3) for different candidate lines and calculating the *SoSR*s for the developed systems of equations. On average, the first part takes around 25 ms by the methods in [3-4], which is reduced to 12 ms using the proposed technique. The second part is identical in all methods and takes around 5 ms for the IEEE 39-bus system with 34 candidate lines. Thus, the proposed technique in this paper reduces the whole computational burden by about 40%. As detailed in Appendix B, the computation time of WABP by the proposed technique can be presented by "Big O Notation" as $\boldsymbol{O}(5{N_m}^2)$, where N_m is the number of measurements. The constant scalar 5 can be dropped in big O notation for a very large N_m.

V. CONCLUSION

This letter proposes a technique to reduce the computational complexity of wide-area backup protection (WABP) methods that are based upon the superimposed circuit concept. A proposition is put forward and proved to demonstrate that there is a one-to-one equivalence between the responses of the superimposed circuit with and without the faulted line. This removes the need for calculating as many bus impedance matrices as the number of candidate lines in the system to identify the faulted line. The proposed technique limits the foregoing requirement to merely calculating the bus impedance matrix of the pre-fault power system. Extensive simulations conducted confirm that the proposed technique can reduce the computational burden without impacting the success rate of WABP. The reduced computational burden offered by the proposed technique, along with other merits of superimposed-circuit-based WABP methods such as adaptability with the sparsity of PMUs and communication latencies, increase the chances of the uptake of such methods by system operators.

APPENDIX A: MATHEMATICAL PROOF OF THE PROPOSITION

Let us assume that the two non-zero nodal injections ΔI_i and ΔI_j result in superimposed voltages $\Delta V_1, \Delta V_2, \dots, \Delta V_N$ in the circuit of Fig. 1(c). Now, let us reorder buses as *i*, *j*, 1, …, *N*. The admittance matrix of the circuit of Fig. 1(c) after this reordering is denoted by $\boldsymbol{Y}$. By partitioning $\boldsymbol{Y}$, the nodal equations for this circuit can be written as below

$$\begin{bmatrix} \Delta I_i \\ \Delta I_j \\ \hline 0 \\ \vdots \\ 0 \end{bmatrix} = \overbrace{\left[\begin{array}{c|c} \boldsymbol{A}_{2\times 2} & \boldsymbol{B}_{2\times(N-2)} \\ \hline \boldsymbol{C}_{(N-2)\times 2} & \boldsymbol{D}_{(N-2)\times(N-2)} \end{array}\right]}^{\boldsymbol{Y}} \begin{bmatrix} \Delta V_i \\ \Delta V_j \\ \hline \Delta V_1 \\ \vdots \\ \Delta V_N \end{bmatrix} \tag{A1}$$

In virtue of the invertibility of the nodal admittance matrix [9], the superimposed voltages ΔV_i and ΔV_j can be uniquely calculated from (1) as follows

$$\begin{bmatrix} \Delta V_i \\ \Delta V_j \end{bmatrix} = \begin{bmatrix} Z_{ii} & Z_{ij} \\ Z_{ij} & Z_{jj} \end{bmatrix} \begin{bmatrix} \Delta I_i \\ \Delta I_j \end{bmatrix} \tag{A2}$$

Let z_l and y_l denote the series impedance and shunt admittance of line *i*-*j*, which can be accurately calculated from the distributed parameter model of line *i*-*j*. Now let us define nodal injections $\Delta I_i'$ and $\Delta I_j'$ as below

$$\begin{bmatrix} \Delta I_i' \\ \Delta I_j' \end{bmatrix} = \begin{bmatrix} \frac{1}{z_l} + \frac{y_l}{2} & \frac{-1}{z_l} \\ \frac{-1}{z_l} & \frac{1}{z_l} + \frac{y_l}{2} \end{bmatrix} \begin{bmatrix} Z_{ii} & Z_{ij} \\ Z_{ij} & Z_{jj} \end{bmatrix} \begin{bmatrix} \Delta I_i \\ \Delta I_j \end{bmatrix} + \begin{bmatrix} \Delta I_i \\ \Delta I_j \end{bmatrix} \tag{A3}$$

One can conclude from (A1)-(A3) that

$$\begin{bmatrix} \Delta I_i' \\ \Delta I_j' \end{bmatrix} = \overbrace{\left(\begin{bmatrix} \frac{1}{z_l} + \frac{y_l}{2} & \frac{-1}{z_l} \\ \frac{-1}{z_l} & \frac{1}{z_l} + \frac{y_l}{2} \end{bmatrix} + \boldsymbol{A} \right)}^{\boldsymbol{A'}} \begin{bmatrix} \Delta V_i \\ \Delta V_j \end{bmatrix} + \boldsymbol{B} \begin{bmatrix} \Delta V_1 \\ \vdots \\ \Delta V_N \end{bmatrix} \tag{A4}$$

Combining (A4) with the lower part of (A1) gives

$$\begin{bmatrix} \Delta I_i' \\ \Delta I_j' \\ \hline 0 \\ \vdots \\ 0 \end{bmatrix} = \overbrace{\left[\begin{array}{c|c} \boldsymbol{A'}_{2\times 2} & \boldsymbol{B}_{2\times(N-2)} \\ \hline \boldsymbol{C}_{(N-2)\times 2} & \boldsymbol{D}_{(N-2)\times(N-2)} \end{array}\right]}^{\boldsymbol{Y'}} \begin{bmatrix} \Delta V_i \\ \Delta V_j \\ \hline \Delta V_1 \\ \vdots \\ \Delta V_N \end{bmatrix} \tag{A5}$$

The only difference between the circuits of Figs 1(c) and 1(d) is that line *i*-*j* does not exist in the former but in the latter. It can be confirmed that the matrix $\boldsymbol{Y'}$ is the admittance matrix of the circuit of Fig. 1(d) in which the buses are reordered as *i*, *j*, 1, …, *N*. Since the shunt/series elements of line *i*-*j* are only connected to buses *i* and *j*, the submatrices $\boldsymbol{B}$, $\boldsymbol{C}$, and $\boldsymbol{D}$ in $\boldsymbol{Y}$ and $\boldsymbol{Y'}$ are identical. Accounting for these elements, $\boldsymbol{A}$ needs to be replaced by $\boldsymbol{A'}$ to form the admittance matrix of the circuit of Fig. 1(d). Therefore, (A5) implies that injecting $\Delta I_i'$ and $\Delta I_j'$ in the circuit of Fig. 1(d), results in the same superimposed voltages as those in the circuit of Fig. 1(c).

The voltage response equivalence between the two circuits guarantees that the superimposed branch currents in both circuits are identical. This is because identical lines will carry the same currents if subjected to the same terminal voltages. This ends the proof. The converse of the Proposition can be proved in a similar way, as well.

TABLE B1
BIG O NOTATION REPRESENTATION FOR *SoSR* CALCULATION

Operation	Big O notation
$\boldsymbol{Y1}_{2\times N_m} = \boldsymbol{H}_{2\times N_m}{}^{*}\, \boldsymbol{R}^{-1}_{N_m\times N_m}$	$O(2{N_m}^2)$
$\boldsymbol{Y2}_{2\times 2} = (\boldsymbol{Y1}_{2\times N_m}\, \boldsymbol{H}_{N_m\times 2})^{-1}$	$O(4N_m)$
$\boldsymbol{Y3}_{N_m\times 2} = \boldsymbol{H}_{N_m\times 2}\, \boldsymbol{Y2}_{2\times 2}$	$O(4N_m)$
$\boldsymbol{S}_{N_m\times N_m} = \boldsymbol{I} - \boldsymbol{Y3}_{N_m\times 2}\, \boldsymbol{Y1}_{2\times N_m}$	$O(2{N_m}^2)$
$\boldsymbol{Y4}_{N_m\times 1} = \boldsymbol{S}_{N_m\times N_m}\boldsymbol{m}_{N_m\times 1}$	$O({N_m}^2)$
$SoSR = \boldsymbol{Y4}_{1\times N_m}{}^{*}\, \boldsymbol{Y4}_{N_m\times 1}$	$O(N_m)$

APPENDIX B: ANALYSIS OF THE COMPUTATION TIME

The computation time of WABP using the proposed technique for every candidate line includes the time needed to build the matrix $\boldsymbol{H}$ related to the candidate lines and the calculation time for the *SoSR* of the line. Let N_m denote the number of measurements. The big O notation of the computation time of the method represents the asymptotic curve that refers to the computation complexity with a very large N_m [10]. As detailed in [3], three multiplications are needed to calculate every entry of $\boldsymbol{H}$. Therefore, T_H can be represented as $\boldsymbol{O}(6N_m)$ for all $2N_m$ entries in $\boldsymbol{H}$. Big O notation for multiplication of a $n \times p$ matrix to a $p \times q$ matrix is $\boldsymbol{O}(npq)$ [10]. Accordingly, Table B1 shows the big O notation of *SoSR* calculations in detailed steps. The terms $O({N_m}^2)$ dominate the $O(N_m)$ ones, and thus, the total computation time can be represented as $\boldsymbol{O}(5{N_m}^2)$ for every candidate line. The constant scalar 5 can be dropped in big O notation for a very large N_m.

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