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# Mitigating Potential-Induced Degradation (PID) Using $SiO_2$ ARC Layer

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**Abstract:** Potential-induced degradation (PID) of photovoltaic (PV) cells is one of the most severe types of degradation, where the output power losses in solar cells may even exceed 30%. In this article, we present the development of a suitable anti-reflection coating (ARC) structure of solar cells to mitigate the PID effect using a $SiO_2$ ARC layer. Our PID testing experiments show that the proposed ARC layer can improve the durability and reliability of the solar cell, where the maximum drop in efficiency was equal to 0.69% after 96 h of PID testing using an applied voltage of 1000 V and temperature setting at 85 °C. In addition, we observed that the maximum losses in the current density are equal to 0.8 mA/cm$^2$, compared with 4.5 mA/cm$^2$ current density loss without using the $SiO_2$ ARC layer.

**Keywords:** solar cells; PID mitigation; ARC; electroluminescence imaging; current density

## 1. Introduction

Photovoltaic (PV) energy conversion based on crystalline silicon (c-Si) solar cells is one of the significant technological pillars of the tremendous success of the PV industry in the last decade. Confirmed terrestrial PV module efficiencies of c-Si are above 24%, and for multi-crystalline silicon solar cells are as close as 20% [1].

Improving the efficiency of solar cells has been a perpetually challenging task, since there is a strong interaction between the different recombination losses, including intrinsic and extrinsic recombination loss with current density at maximum power point (MPP) as a function of the surface recombination at the rear side [2]. In addition, the anti-reflection coating (ARC) structures of the solar cell play an essential role in shaping the maximum efficiency of the cell; an incorrect ARC structure can lead to a significant drop in the current density of more than 3.5 mA/cm$^2$ [3].

To keep the efficiency of solar cells at its highest levels, the reliability and stability must be carefully checked. To facilitate this inspection, potential-induced degradation (PID) testing is strongly advised [4]. The PID test measures the leak current by applying a high voltage (normally 1000 V and above, according to IEC 62804 standard) in a high-temperature and high-humidity environment. After the full duration of the test—96 h—the degradation of the PV module, or on a small scale as a standalone solar cell, can be measured by comparing the current-voltage (I-V) curve before PID testing begins and after the PID test is fully complete [5]. In addition, the electroluminescence (EL) imaging can be captured prior to and after the PID test to visualise the actual collision on the surface structure after PID testing is done. EL imaging can also facilitate the overview of the cracks and defects of the cell, which is immeasurably valuable [6].

Current research expresses significant interest in mitigating the PID problems of solar cells. This is for three main reasons. Firstly, the PID degrades the output power of the solar cells. Secondly, every solar cell affected by PID reduces the total string voltage [7]. Thirdly, it is difficult to detect this problem quickly when overall PV installations are up and running [8] because degradation of PV output power is not only due to the impact of PID but also the existence of faulty bypass diodes [9], faulty PV modules [10–12] and hotspots [13].

There are numerous ARC structures now available in the literature. However, a limited number of these structures have had PID testing to check their reliability, stability and degradation, to ensure that the reported efficiencies are accurate. N-type solar cell structures, including BiSoN, MoSon and pPERT, have been investigated by Devoto and Halm [14]. It was concluded that the above-mentioned ARC solar cell structures cannot mitigate PID testing, and after 74 h of PID testing, there is an approximately 20% drop in their efficiency. Other experiments [15,16] have shown that p-type solar cells can degrade efficiency in the range of 5% to 25%.

The investigation of bifacial PID in bifacial mono c-Si p-PERC solar cells was developed by Carolus et al. [17]. It was evident that there is more considerable reduction in the efficiency of bifacial solar cells that have glass packing renders, which tends to be extremely sensitive to PID testing. Furthermore, the front side of bifacial solar cells tends to have more degradation than the rear junction.

One solution for mitigating the PID effect on solar cells is to change the capsulation film instead of using ethylene vinyl acetate (EVA)., Wang [18] suggests using Poly Olefin (PO) material with a low water vapour through rate. This solution can potentially reduce the power losses to around 3%. In addition, this new material was proven to improve the reliability and stability of PV solar cells, as demonstrated by López-Escalante et al. [19]. They show that PO-made solar cells are resistant, to a certain degree, to the PID effect. Other research [20] suggests using a thin silicon dioxide ($SiO_2$) ARC layer in combination with p-type or n-type solar cells that can enhance the efficiency of the solar cell after applying the PID test. There are some other recognised methods for mitigating PID effect on solar cells, such as replacing the soda-lime glass with a quartz glass that guarantees the solar glass is free of the suspected PID ions [21]. Another appropriate method to mitigate the PID effect of solar cells is to attach narrow, thin, flexible glass strips on the glass surface along the inner edges of the solar cell frame [22]. The drop in output power after PID testing is equal to 8.8%, while it is equal to 15% prior to using this mitigation technique.

Experimental evidence of the PID effect on copper indium gallium selenide (CIGS) showed that CIGS PV cells suffer from PID testing [23]. The results showed that there is an almost 15% drop in the maximum output power after 120 h of PID testing. In addition, it was also evident that the back and front contact almost have the same drop in maximum power as well as short circuit current after completing the PID testing cycle.

## 2. Gap in Knowledge

Perhaps one of the most important factors in today's PV manufacturing systems and production is the reliability and stability of the used materials. We have seen a rapid increase in new ideas for how to mitigate the effect of PID on newly-developed solar cell structures. However, there is still a lack of existing ARC structures that have been proven to be effective at mitigating PID. Therefore, in this article we present the development of a suitable ARC structure created by layering $SiO_2$ at the bottom of $SiN_x$ that effectively reduces the PID affect. Results show that there is a limited drop in the maximum power of 0.01 W, and the overall drop in efficiency is limited at 0.69% after 96 h of PID testing using an applied voltage of 1000 V and temperature setting at 85 °C.

## 3. Paper Organization

The rest of the article is organised as follows: Section 4 presents PID testing experiments performed on three different solar cell ARC structures. Section 5 presents the results of PID testing on the PV cell $SiO_2$-free layer, $SiO_2$ layer placed at the top of $SiN_x$, and the $SiO_2$ layer placed at the bottom of $SiN_x$.

Lastly, Section 6 presents the overall conclusion of the results discussed in the article, followed by the acknowledgement and the reference list.

## 4. Experiment

In this study, a PID test was conducted by constructing three polycrystalline silicon solar cells with three types of ARC structures. The test was carried out using PIDcon PID-tester according to IEC 62804 standard, at 0 h and after 96 h. The working principles of the PIDcon test setup are shown in Figure 1.

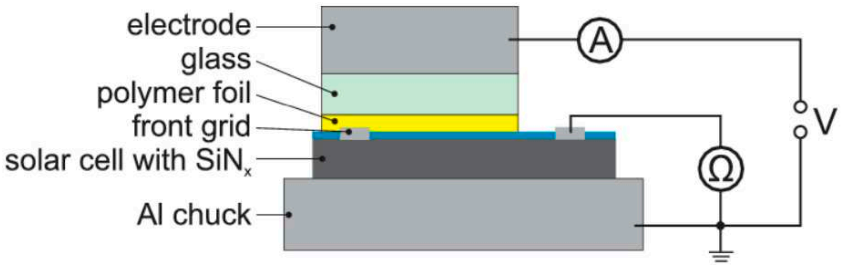


**Figure 1.** A simple schematic of the working principles of the PIDcon test setup.

The layer consists of a solar cell, polymer foil, and glass between the two metal electrodes. A positive voltage is applied at the upper electrode, while the bottom electrode is virtually grounded/heated. The shunt resistance ($R_{sh}$) as a function of time is also measured. The standard test conditions were as follows: (i) voltage 1000 V, (ii) temperature 85 °C, (iii) dry conditions, no use of water and (iv) test duration 96 h.

The solar cells' structure that has been tested in this study is shown in Figure 2. The first solar cell structure (Figure 2a) is made free of $SiO_2$ while the second solar cell structure as in Figure 2b includes the $SiO_2$ thin film placed on the top of the silicon nitride ($SiN_x$). The last solar cell is where the $SiO_2$ thin film is placed at the bottom of the $SiN_x$. For ease of referencing the solar cells, we called them the first cell #1, the second cell #2 and the third cell #3.

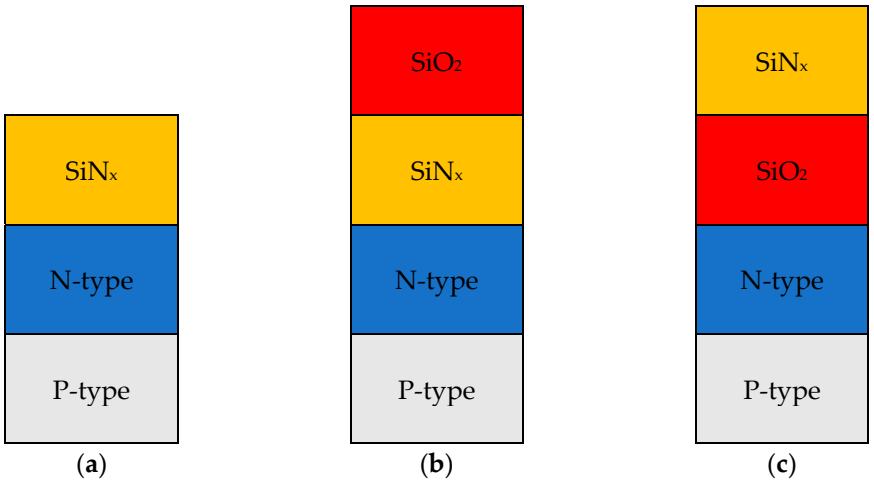


**Figure 2.** Anti-reflection coating (ARC) structure of the three examined solar cells: (**a**) $SiO_2$-free (cell #1), (**b**) $SiO_2$ layer placed at the top of $SiN_x$ (cell #2), and (**c**) $SiO_2$ layer placed at the bottom of $SiN_x$ (cell #3).

To compare the PID of the three examined solar cells, we must first identify the critical electrical parameters that have to be measured and compared. Here, we complied with the IEC 62804 standard, thus comparing the maximum power ($P_{max}$), efficiency, and short-circuit current density ($J_{sc}$). The efficiency was calculated using the following (*FF* is the fill factor, and $V_{oc}$ corresponds to the open-circuit voltage):

$$\text{Efficiency} = J_{sc} \times V_{oc} \times FF \quad (1)$$

### *4.1. $SiO_2$ Layer Preperation and Properties*

The $SiO_2$ thin film was prepared by liquidphased deposition. The deposition system contained temperature-controlled water to maintain uniformity in the deposition temperature amongst the surface and a Teflon vessel as a liquid solution. Initially, 25 g of silica powder with 99.9% purity was mixed with 500 mL of hydrofluorosilicic acid; this mixture was stirred for almost 24 h to ensure that the hydrofluorosilicic acid became saturated. The next step was to mix 32 mL of the saturated hydrofluorosilicic acid with 25 mL boric acid for the deposition of the $SiO_2$ film.

After the deposition process was complete, we rinsed a tin-doped indium oxide glass in water; this process is required to make a purified nitrogen gas. Finally, the thin film was annealed in the air for 10 min at 425 °C. The chemical reaction between oxygen and silicon to generate $SiO_2$ is usually driven by a high-heat environment; however, even at room temperature, a shallow layer of native oxide, approximately 1 nm thick, can form in an air environment.

The reasons for selecting $SiO_2$ to mitigate the PID effect of solar cells are summarised as follows:

- It is straightforward to deposit on various materials and grown thermally on silicon wafers, which makes it manageable for manufacturing purposes.
- It can block the ion diffusion implementation of many undesired contaminants, particularly when placed on the bottom of the $SiN_x$ layer.
- The interface between silicon and silicon dioxide has relatively few mechanical and electrical defects.
- It has high dielectric strength and a relatively wide bandgap, making it an excellent insulator.
- It has high-temperature stability of up to 1600 °C, making it a useful material for process and device integration [24].
- The $SiO_2$ layer causes the silicon-silicon dioxide interface to move into the wafer while the oxide grows. This would typically mean that while the oxide grows, it consumes the silicon atoms at the surface of the wafer, making it a more reliable structural layer.

### *4.2. Experiment Setup (Tools and Equipment)*

To perform the PID test on the solar cell samples, PIDcon PID-tester has been used. The main characteristics of this tester are that no climate chamber is necessary during the PID test and no lamination of the solar cells is required [25]. The leakage current, output power and I-V curve also can be measured using this device. After the completion of PID testing, the solar cells were subjected to EL imaging. This procedure used a high-resolution Keland EL tester. This device also allows the inspection of the current density of the solar cells. Therefore, by the end of each experiment, the I-V curve, EL and current density images were analysed and compared.

The circuit diagram of the double diode model used for the analysis of the I-V curve measurements is shown in Figure 3. The junction recombination is modeled by adding a second diode ($D_2$) in parallel with the first ($D_1$) and setting the ideality factor typically to two.

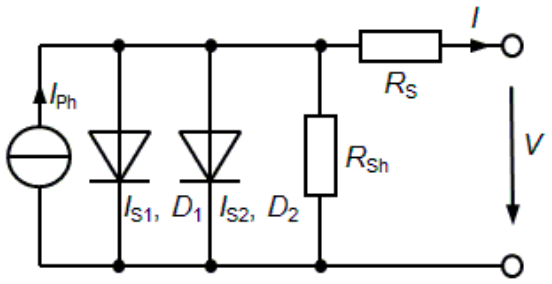


**Figure 3.** Circuit diagram of the double diode model including the series ($R_s$) and parallel ($R_{sh}$) resistances.

### *4.3. Performance of the Examined Solar Cell Samples Before PID Testing*

The EL, current density and I-V curves of the three solar cell samples before the PID test are shown in Figure 4. The critical parameters before the PID test began are summarised in Table 1: the efficiency of cell #3 is equal to 19.24% (the lowest) and 20.32% for cell #2 (the highest). In addition, the value of the current density, open-circuit voltage and the fill factor are almost identical for the three solar cell samples.

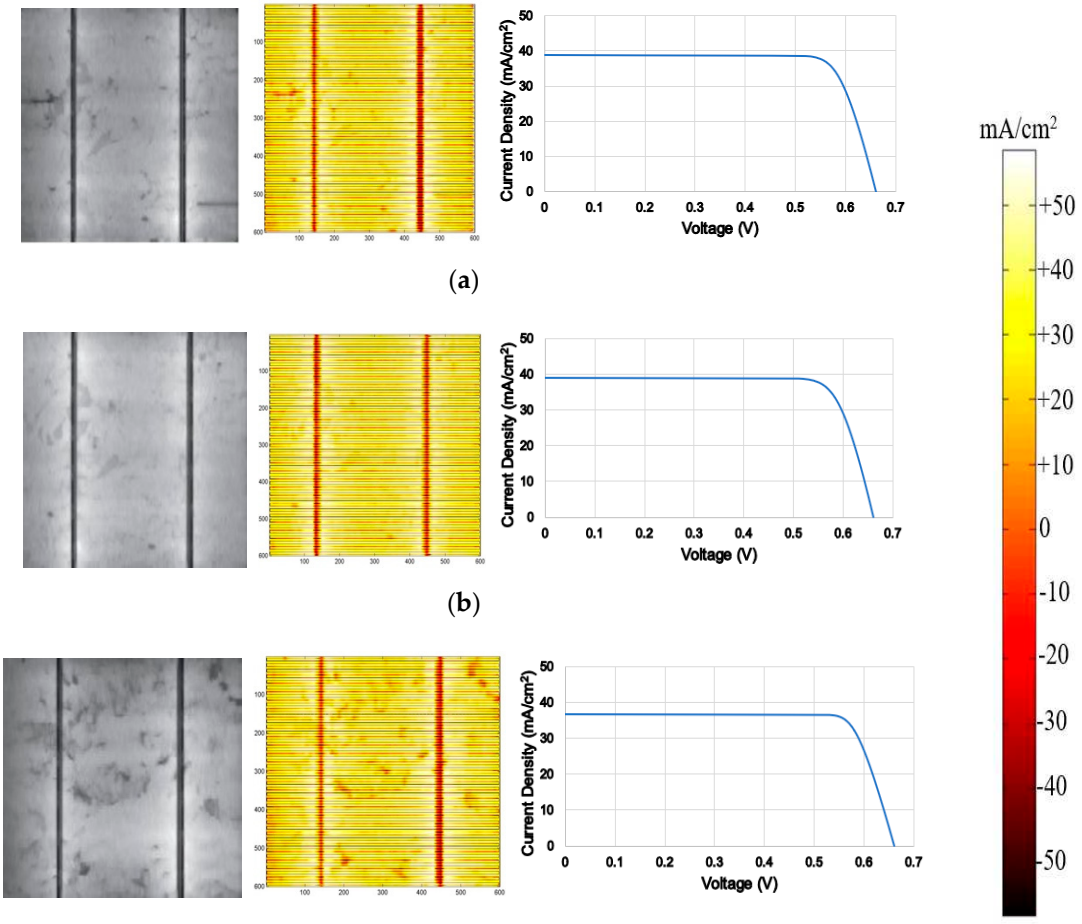


**Figure 4.** Electroluminescence (EL), current density and the current-voltage (I-V) curve of the three examined solar cells before the potential-induced degradation (PID) test: (**a**) cell #1, (**b**) cell #2 and (**c**) cell #3.

**Table 1.** Summary of the critical parameters for the examined solar cells before the PID test.

| Sample | $J_{sc}$ (mA/cm$^2$) | $V_{oc}$ (V) | *FF* (%) | $P_{max}$ (W) | $R_{sh}$ (Ω) | Efficiency (%) |
|---|---|---|---|---|---|---|
| Cell #1 | 37.77 | 0.68 | 77.1 | 0.48 | 87.7 | 19.80 |
| Cell #2 | 38.91 | 0.68 | 76.8 | 0.49 | 84.4 | 20.32 |
| Cell #3 | 37.72 | 0.66 | 77.3 | 0.46 | 89.2 | 19.24 |

According to Figure 4, the EL image showed no cracks or significant defects in the examined solar cells before the PID test began. The current density images also show a uniform distribution of the current for all samples, meaning no defects or leakage current is present. Seeing that the negative value of current density represents a reverse current following from the solar cell, zero current density

represents no flow of current at a particular area of the cell, whereas the positive value of the current density shows a direct DC current generated by the cell.

## 5. Results

### *5.1. $SiO_2$-Free (Cell #1)*

After the completion of the PID test over 96 h, the EL and current density images were taken, as shown in Figure 5. It is evident that the solar cell had a considerable amount of degradation. As exhibited by the current density image, after PID testing there is a significant part of the solar cell that produces even negative current density, which typically results in a decrease in the efficiency of the cell.

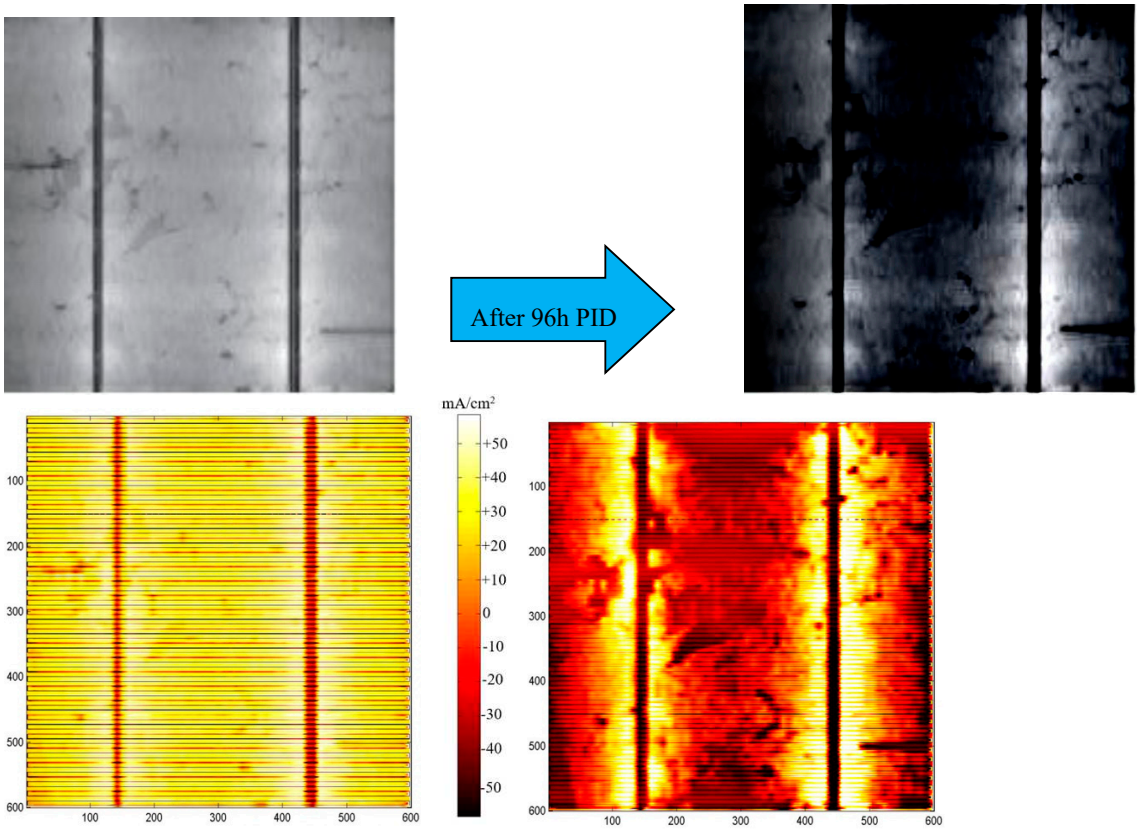


**Figure 5.** EL and the current density image of the first solar cell sample, $SiO_2$-free.

Figure 6 shows the actual I-V curve of the solar cell before vs. after PID testing. The summary of the comparison between all relevant parameters is presented in Table 2. As can be seen, after PID testing, all related parameters of the solar cell significantly dropped. Remarkably, the efficiency of the solar cell became 13.96%, compared with 19.80% before PID testing (loss = 5.84%). Therefore, without the $SiO_2$ coating, the solar cell would potentially keep degrading over time.

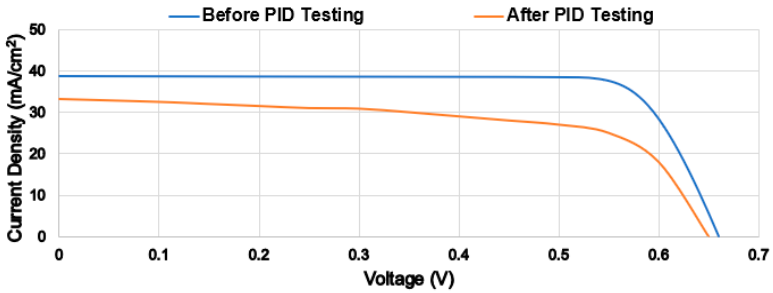


**Figure 6.** I-V curve characteristics before and after PID testing of the first solar cell sample, $SiO_2$-free.

**Table 2.** Before vs. after PID testing of the first solar cell sample (cell #1).

| Solar Cell #1 | $J_{sc}$ (mA/cm$^2$) | $V_{oc}$ (V) | *FF* (%) | $P_{max}$ (W) | $R_{sh}$ (Ω) | Efficiency (%) |
|---|---|---|---|---|---|---|
| Before PID | 37.77 | 0.68 | 77.1 | 0.48 | 87.7 | 19.80 |
| After PID | 33.2 | 0.66 | 63.7 | 0.37 | 9.12 | 13.96 |

The leakage current of this cell is generated continuously. Therefore, PV modules made of $SiO_2$-free ARC structure would typically suffer from PID phenomena, leading to poor stability and significant decay of the output power production, and hence continuous degradation at higher rates.

### *5.2. $SiO_2$ Thin Film Placed on the Top of the $SiN_x$ (Cell #2)*

The I-V curve results of PID testing of the second solar cell, which has a top-layer $SiO_2$ ARC structure, are shown in Figure 7. This result reveals that placing the $SiO_2$ layer on the top of the $SiN_x$ does not have a significant impact on the stability of the solar cell. In fact, the experiment shows that the efficiency dropped by 7.03% (i.e., before PID it was 20.32%, and after PID it was 13.29%). Other relevant parameters are presented in Table 3.

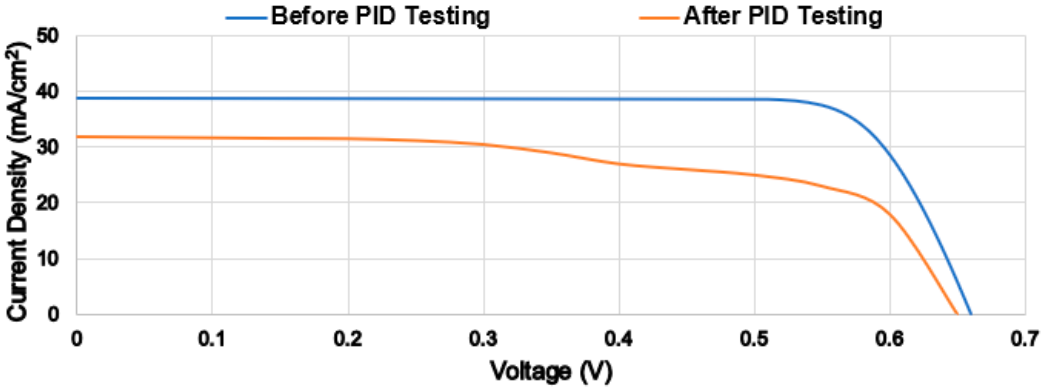


**Figure 7.** I-V curve characteristics before and after PID testing of the second solar cell sample, with $SiO_2$ layer placed on the top of the $SiN_x$.

**Table 3.** Before vs. after PID testing of the first solar cell sample (cell #2).

| Solar Cell #1 | $J_{sc}$ (mA/cm$^2$) | $V_{oc}$ (V) | *FF* (%) | $P_{max}$ (W) | $R_{sh}$ (Ω) | Efficiency (%) |
|---|---|---|---|---|---|---|
| Before PID | 38.91 | 0.68 | 76.8 | 0.49 | 84.4 | 20.32 |
| After PID | 31.90 | 0.66 | 63.1 | 0.35 | 7.51 | 13.29 |

The EL and current density images of the cell are shown in Figure 8. According to the $J_{sc}$, after completing PID testing, the solar cell dropped from 38.91 mA/cm$^2$ to 31.90 mA/cm$^2$, approximately 18%. This result illustrates the negative impact of layering $SiO_2$ on the top of the $SiN_x$. In addition,

the results of this experiment are almost identical to cell #1 results in terms of the drop in the shunt resistance from 84 Ω to below 10 Ω and the drop in the fill factor from almost 75% to 63%. Thus, it is possible to assume that placing a layer of $SiO_2$ on the top of the $SiN_x$ leads to lowering $J_{sc}$ and $P_{max}$ and, consequently, the cell efficiency.

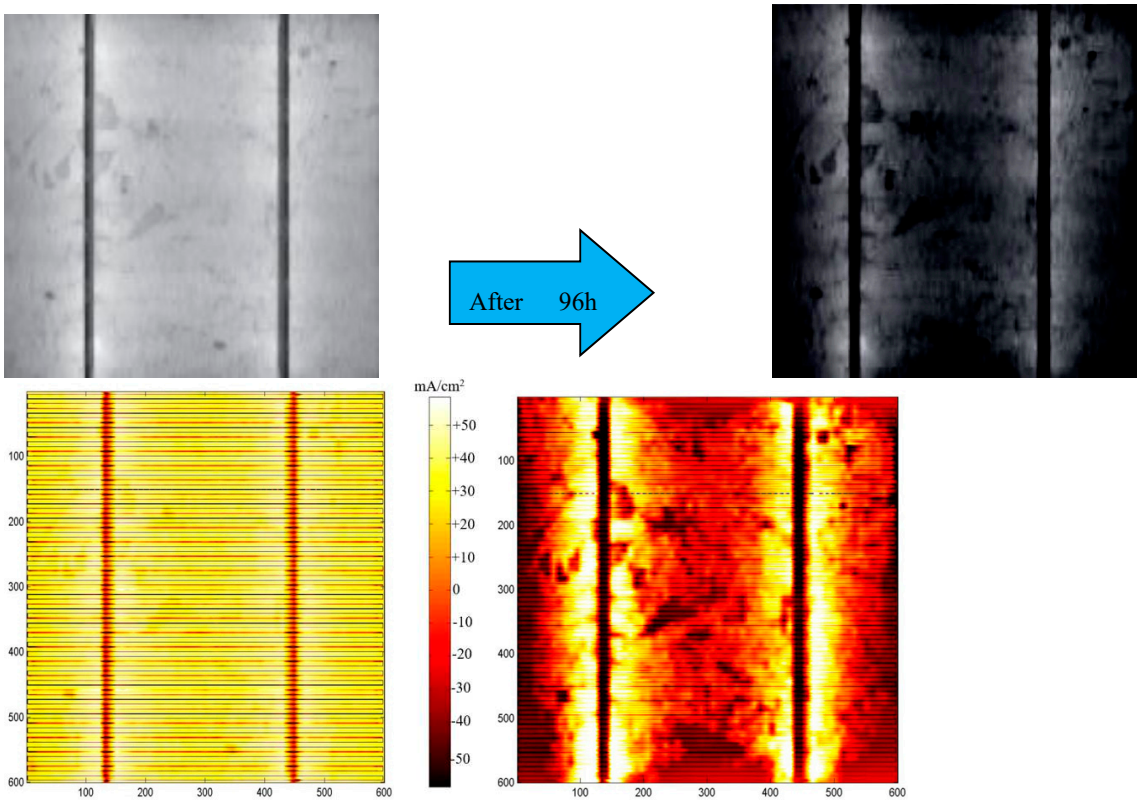


**Figure 8.** EL and the current density image of the second solar cell sample, with SiO2 on the top of the SiNx.

In summary, both solar cell samples with an $SiO_2$ layer on the top of the $SiN_x$ and $SiO_2$-free samples had significant leakage of the current after PID testing. Therefore, this leads us to another experiment, which will be discussed in the next subsection.

### *5.3. $SiO_2$ Thin Film Placed on the Bottom of the $SiN_x$ (Cell #3)*

In this subsection, the results of PID testing of the third solar cell will be discussed. This solar cell has a $SiO_2$ layer placed on the bottom of the $SiN_x$. Placing this layer on the bottom of the $SiN_x$ will reasonably achieve the following:

- Enhance the stability of the solar cell structure, because there will be a limited leakage of the current at the top layer ($SiN_x$), preventing mismatched conditions of the solar cell, particularly during the PID test [26].
- As there will be a limited leakage of the current, the expected drop in efficiency will also be at a minimum level. In addition, a drop in the shunt resistance is expected during PID testing [27]. However, it will be a limited drop as the current density will remain at its highest.

Figure 9 shows the measured I-V curves before and after PID testing for cell #3. There is a limited drop in the maximum power of 0.01 W (approximately 2.2%); the efficiency also dropped by 0.69% (before PID 19.24% and after PID 18.55%). The shunt resistance dropped by 3.5 Ω, representing a decrease of 3.92%. All interpretive parameters before and after PID testing are presented in Table 4.

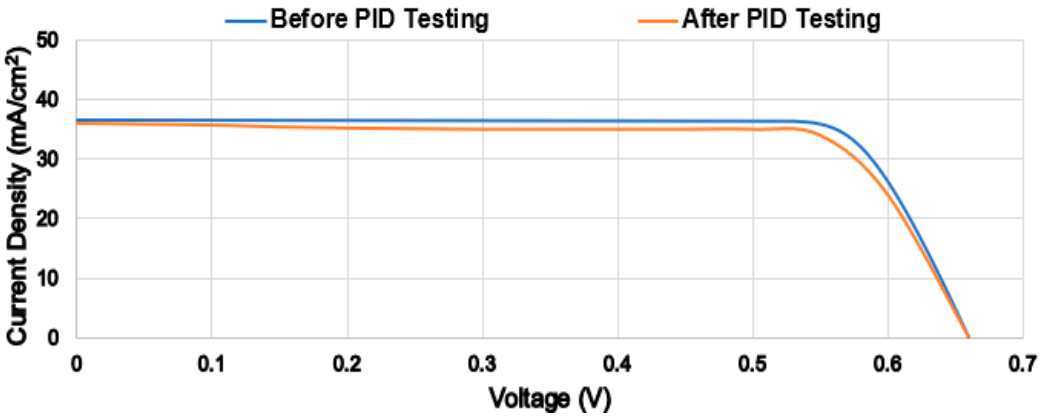


**Figure 9.** I-V curve characteristics before and after PID testing of the second solar cell sample, with $SiO_2$ layer placed on the bottom of the $SiN_x$.

**Table 4.** Before vs. after PID testing of the first solar cell sample (cell #3).

| Solar Cell #1 | $J_{sc}$ (mA/cm$^2$) | $V_{oc}$ (V) | $FF$ (%) | $P_{max}$ (W) | $R_{sh}$ (Ω) | Efficiency (%) |
|---|---|---|---|---|---|---|
| Before PID | 37.72 | 0.66 | 77.3 | 0.46 | 89.2 | 19.24 |
| After PID | 36.88 | 0.66 | 76.2 | 0.45 | 85.7 | 18.55 |

The EL and current density images of the solar cell are shown in Figure 10. As can be noticed, there is a limited loss of approximately 2.2% in the current density after completing the PID test, before PID 37.72 mA/cm$^2$ and after PID 36.88 mA/cm$^2$; therefore, there is a total loss of 0.84 mA/cm$^2$.

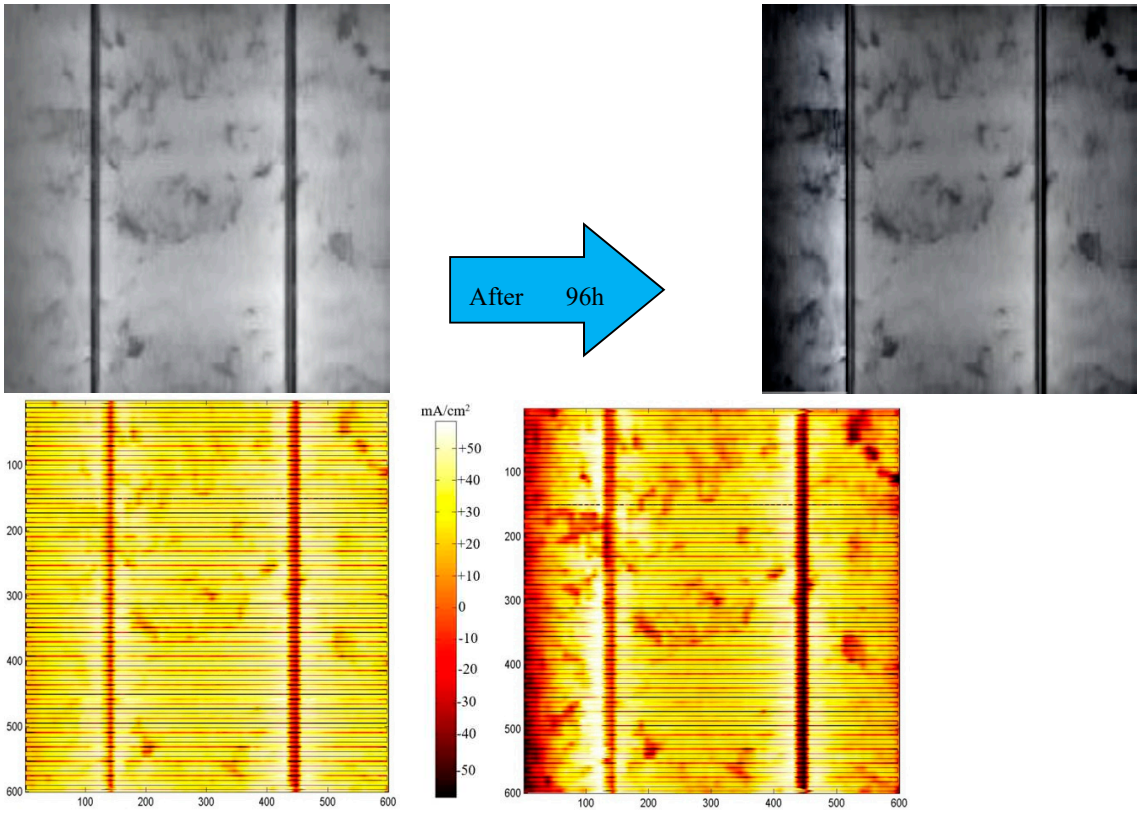


**Figure 10.** EL and the current density image of the third solar cell sample, with $SiO_2$ on the bottom of the SiNx.

Table 5 summarises the percentage drop from before and after PID testing of each critical parameters analysed. Cell #3 shows lower drops for all parameters, reaffirming the effectiveness of using the $SiO_2$ ARC layer for PID mitigation.

**Table 5.** Percentage drops of each critical parameter after PID testing.

| Solar Cell Parameter | Cell #1 | Cell #2 | Cell #3 |
|---|---|---|---|
| $J_{sc}$ | 12.10% | 18.00% | 2.23% |
| $V_{oc}$ | 2.94% | 2.94% | 0% |
| $FF$ | 13.40% | 13.70% | 1.1% |
| $P_{max}$ | 22.92% | 28.57% | 2.17% |
| $R_{sh}$ | 89.60% | 91.10% | 3.92% |
| Efficiency | 5.84% | 7.03% | 0.69% |

In contrast with the above results, one of the decisive successes of mitigating for PID testing when layering $SiO_2$ on the bottom of the $SiN_x$ is that the dark leakage current ($J_0$) is extremely low due to the effective hydrogenation process; this would characteristically reduce the trapped charge density of the solar cell structures, thereby improving the stability and reliability of the cell. In addition, PV modules consist of a series of those cells that can also produce a resolute output power with a limited degradation over time.

## 6. Conclusions

In this article, we discussed the potential of preventing PID by modifying the ARC structure in polycrystalline silicon solar cells. Three types of ARC structures were subjected to the PID test for a period of 96 h under 1000 V and 85 °C conditions, according to IEC 62804 standard. It is possible to conclude that the ARC structure containing $SiO_2$-free or $SiO_2$ layer on the top of the $SiN_x$ has a significant drop in the efficiency, always higher than 5%, after the PID test. A considerable value also decreases all other relevant parameters, including the shunt resistance ($R_{sh}$), short-circuit current density ($J_{sc}$) and maximum output power ($P_{max}$).

We found that when the $SiO_2$ layer is placed on the bottom of the $SiN_x$, there is a limited leakage of the current of the solar cell after the completion of the PID test. Consequently, there was a limited drop in the maximum output power of 0.01 W, which represents approximately 2.2%, and the efficiency also dropped by 0.69%. Therefore, this ARC structure was confirmed to be an effective PID mitigation, preventing PV module degradation as well as increasing its reliability.

For future research, it would be interesting to perform PID testing on a humidity environment since it is common that PV modules are subject to these conditions.

**Author Contributions:** M.D.: formal analysis, methodology, software, writing—original draft, writing—review and editing. Y.H.: methodology, investigation, writing—review and editing. N.S.: formal analysis, supervision and proofreading, visualization, writing—review and editing. R.G.V.: methodology, writing—original draft, writing—review and editing. All authors have read and agreed to the submitted version of the manuscript.

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